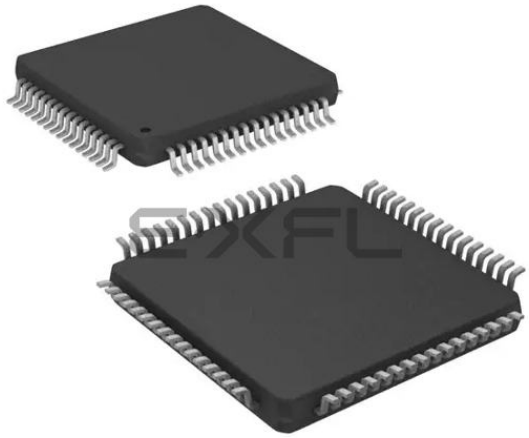

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192a3u-au

7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read and DMA controller write, etc.) can access different memory sections at the same time.

7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.11 JTAG Disable

It is possible to disable the JTAG interface from the application software. This will prevent all external JTAG access to the device until the next device reset or until JTAG is enabled again from the application software. As long as JTAG is disabled, the I/O pins required for JTAG can be used as normal I/O pins.

7.12 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.13 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-4 on page 17 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-4. Number of words and pages in the flash.

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega64A3U	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128A3U	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192A3U	17	192K + 8K	256	Z[8:1]	Z[17:9]	192K	384	8K	16
ATxmega256A3U	18	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16

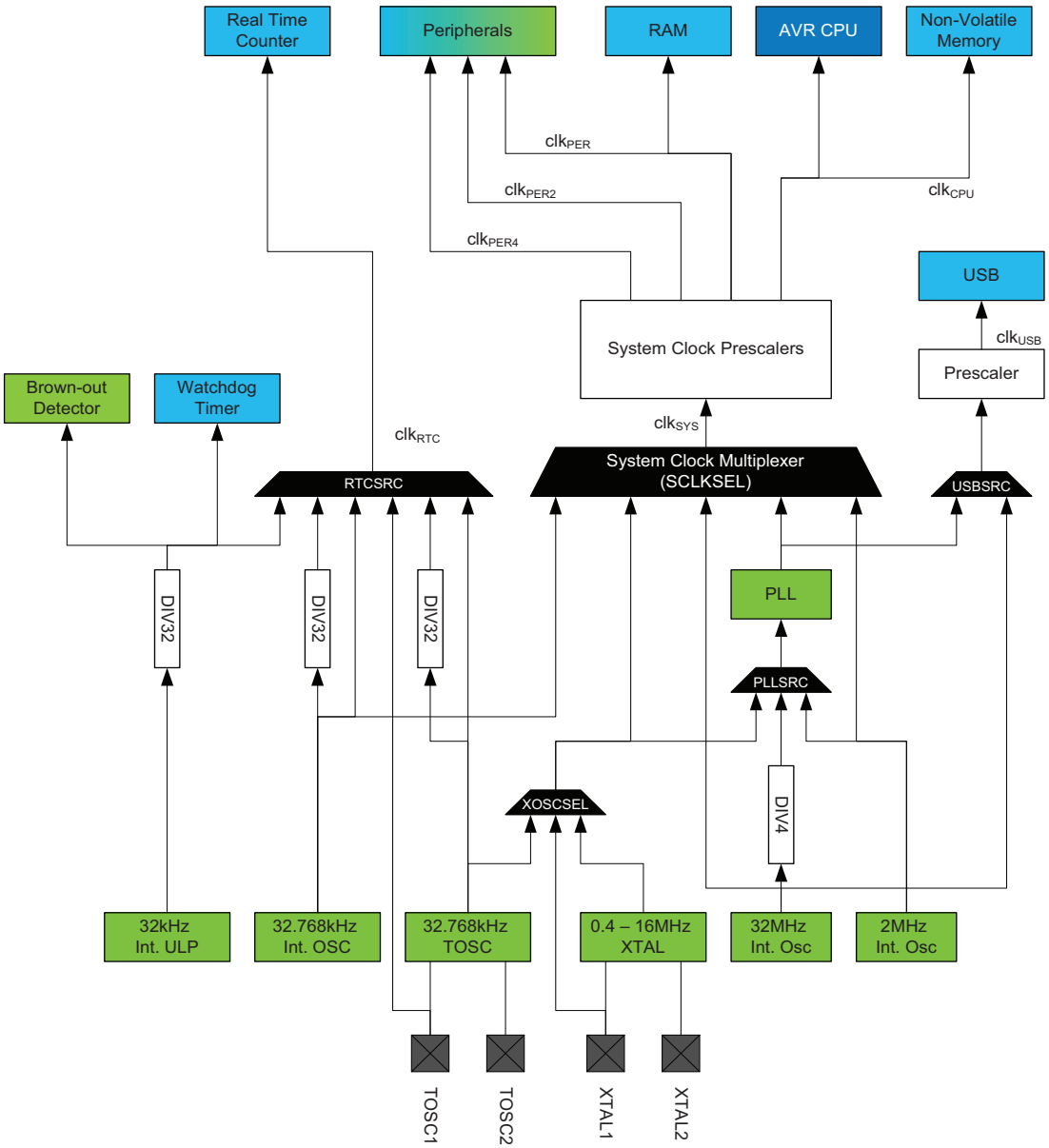
Table 7-5 on page 18 shows EEPROM memory organization for the Atmel AVR XMEGA A3U devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for

addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-5. Number of bytes and pages in the EEPROM.

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No of Pages
	Size	bytes			
ATxmega64A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega192A3U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega256A3U	4K	32	ADDR[4:0]	ADDR[11:5]	128

Figure 10-1. The clock system, clock sources and clock distribution.



10.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

10.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU or DMA controller can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

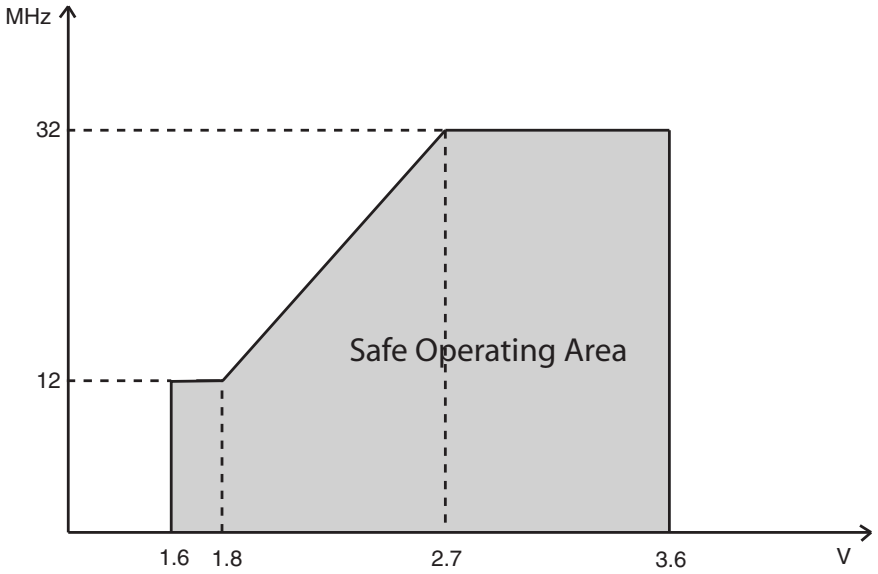
PORTD has one USB. Notation of this is USB.

Table 36-3. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 36-1. Maximum Frequency vs. V_{CC}.



36.1.11 External Reset Characteristics

Table 36-18. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			95	1000	ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V		0.60*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.70*V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V		0.40*V_{CC}		
		V_{CC} = 1.6 - 2.7V		0.30*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

36.1.12 Power-on Reset Characteristics

Table 36-19. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	V

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

36.1.13 Flash and EEPROM Memory Characteristics

Table 36-20. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

36.2.6 ADC characteristics

Table 36-40. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		5.0		kΩ
C_{sample}	Input capacitance	Switched		5.0		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-41. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling Time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

Symbol	Parameter	Condition			Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		2.4k			Ω
			1MHz crystal, CL=20pF		8.7k			
			2MHz crystal, CL=20pF		2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		4.2k			
			8MHz crystal		250			
			9MHz crystal		195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		360			
			9MHz crystal		285			
			12MHz crystal		155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		365			
			12MHz crystal		200			
			16MHz crystal		105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		435			
			12MHz crystal		235			
			16MHz crystal		125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		495			
			12MHz crystal		270			
			16MHz crystal		145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		305			
			16MHz crystal		160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		380			
			16MHz crystal		205			
	ESR	SF = Safety factor					$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin					5.2		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin					6.8		pF
C_{LOAD}	Parasitic capacitance load					2.95		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

36.4.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-120. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.4.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-121. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

36.4.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-122. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.4.16 Two-Wire Interface Characteristics

Table 36-32 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7.

Figure 36-28. Two-wire interface bus timing.

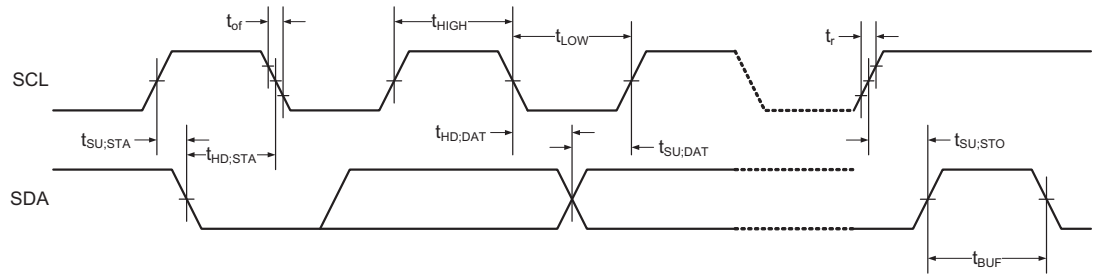
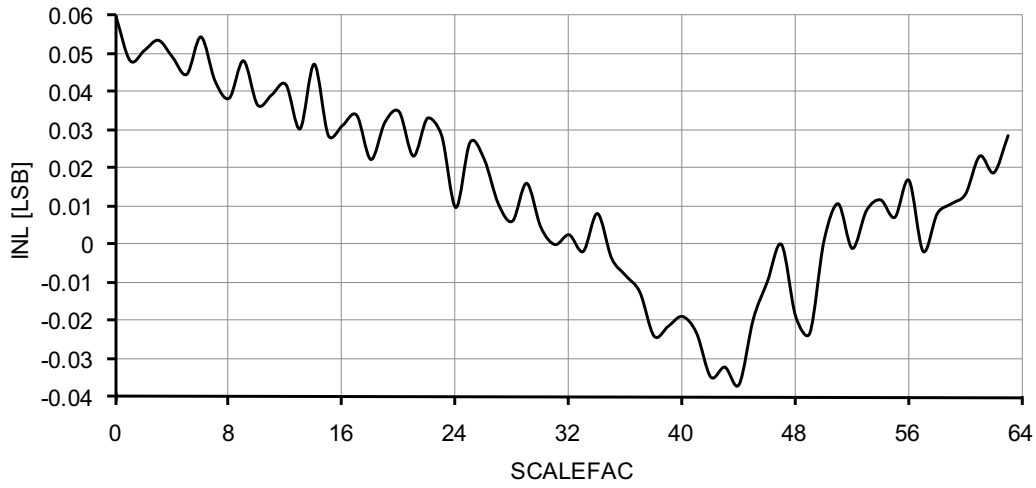


Table 36-128. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		-0.5		0.3*V_{CC}	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs		0.05*V_{CC} (1)			V
V_{OL}	Output Low Voltage	3mA, sink current	0		0.4	V
t_r	Rise Time for both SDA and SCL		20+0.1C_b (1)(2)		300	ns
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF (2)	20+0.1C_b (1)(2)		250	ns
t_{SP}	Spikes Suppressed by Input Filter		0		50	ns
I_I	Input Current for each I/O Pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL Clock Frequency	f_{PER} (3)>max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of Pull-up resistor	$f_{SCL} \leq$ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		f_{SCL} > 100kHz			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold Time (repeated) START condition	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low Period of SCL Clock	$f_{SCL} \leq$ 100kHz	4.7			µs
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High Period of SCL Clock	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			

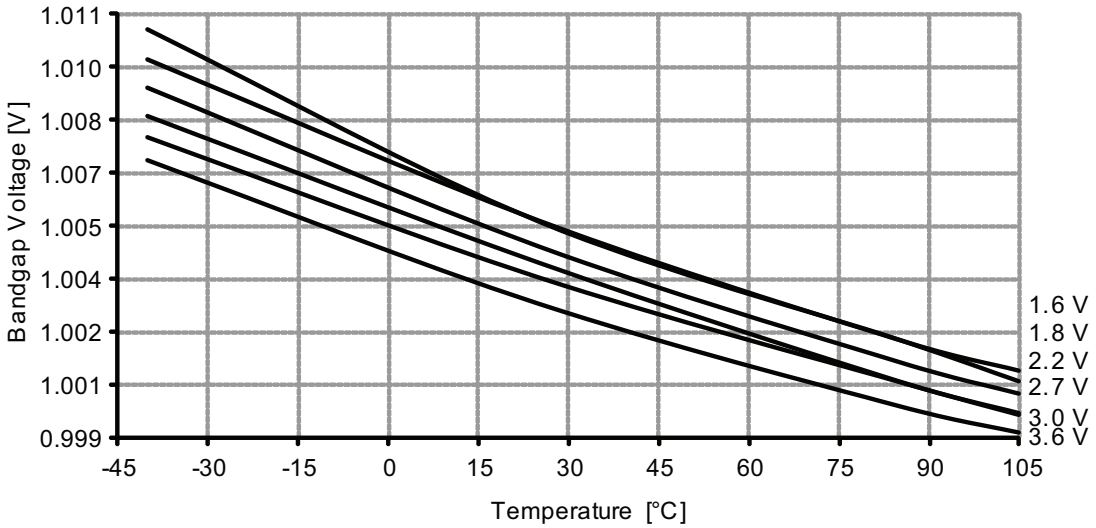
Figure 37-57. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



37.1.6 Internal 1.0V reference Characteristics

Figure 37-58. ADC/DAC Internal 1.0V reference vs. temperature.



37.1.8 External Reset Characteristics

Figure 37-61. Minimum Reset pin pulse width vs. V_{CC}.

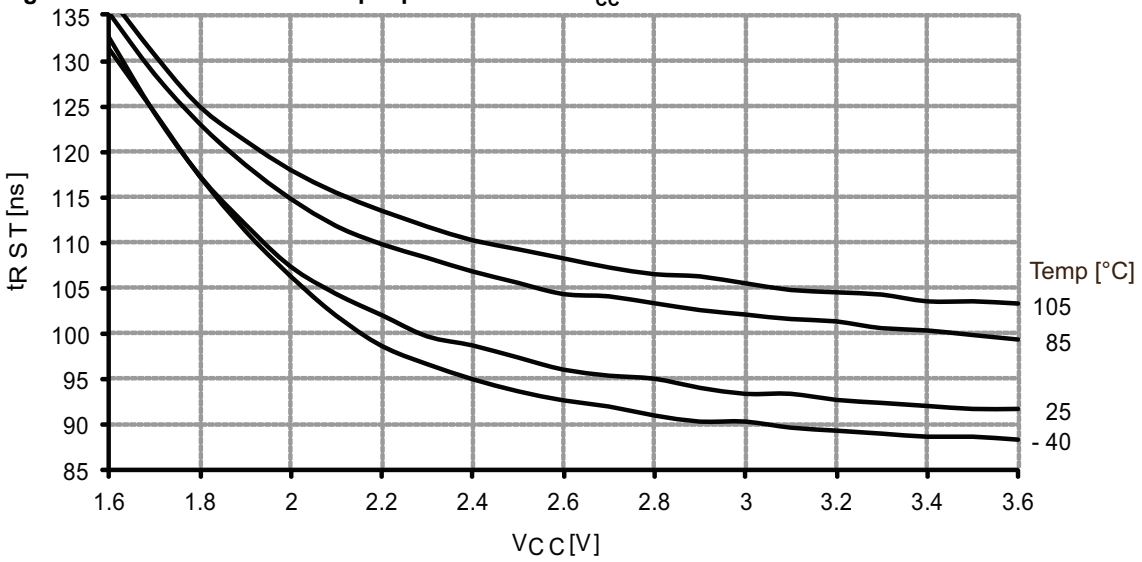
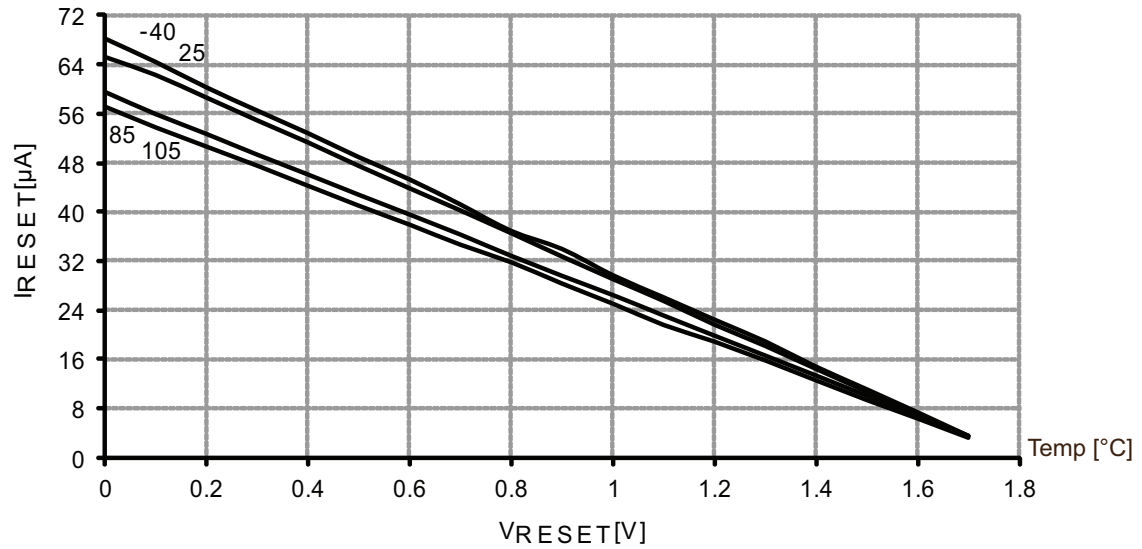


Figure 37-62. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 1.8V.



37.2.7 BOD Characteristics

Figure 37-142. BOD thresholds vs. temperature.

BOD level = 1.6V.

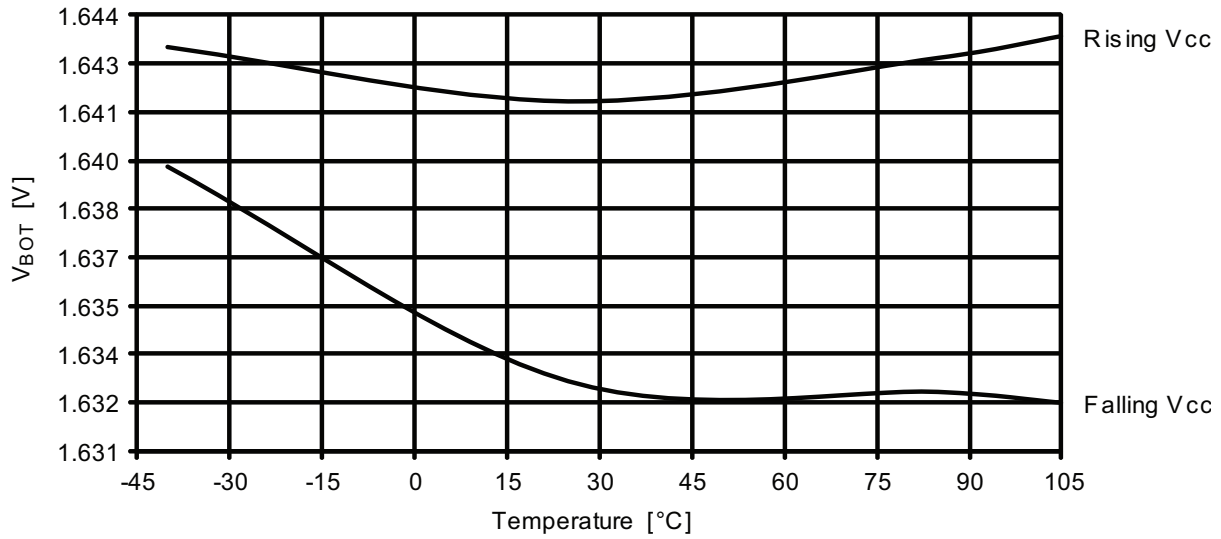


Figure 37-143. BOD thresholds vs. temperature.

BOD level = 3.0V.

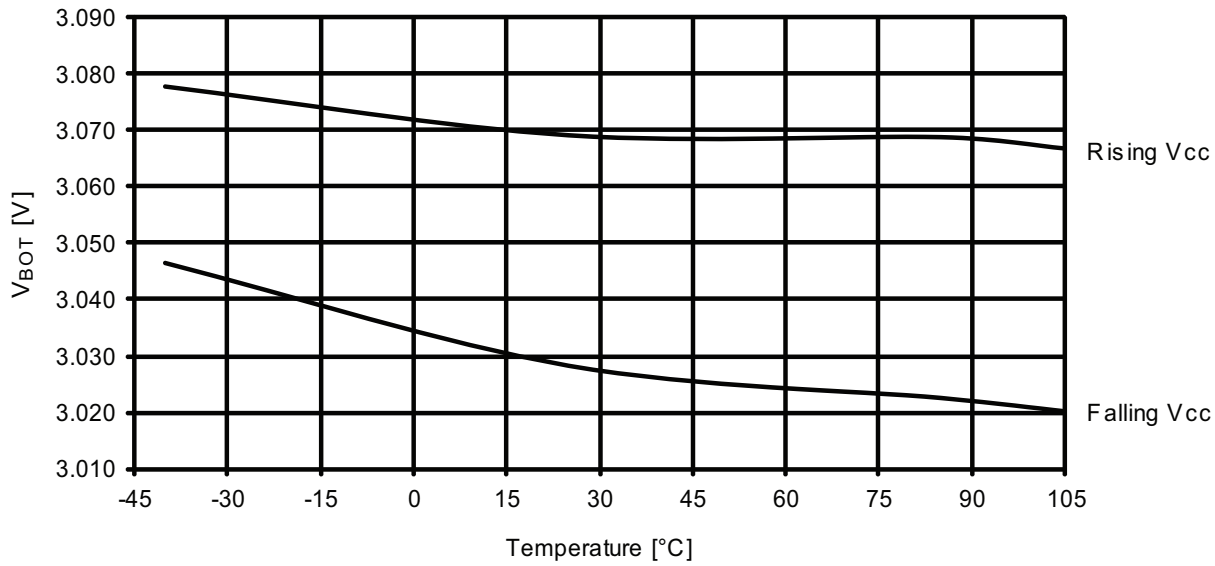


Figure 37-146. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

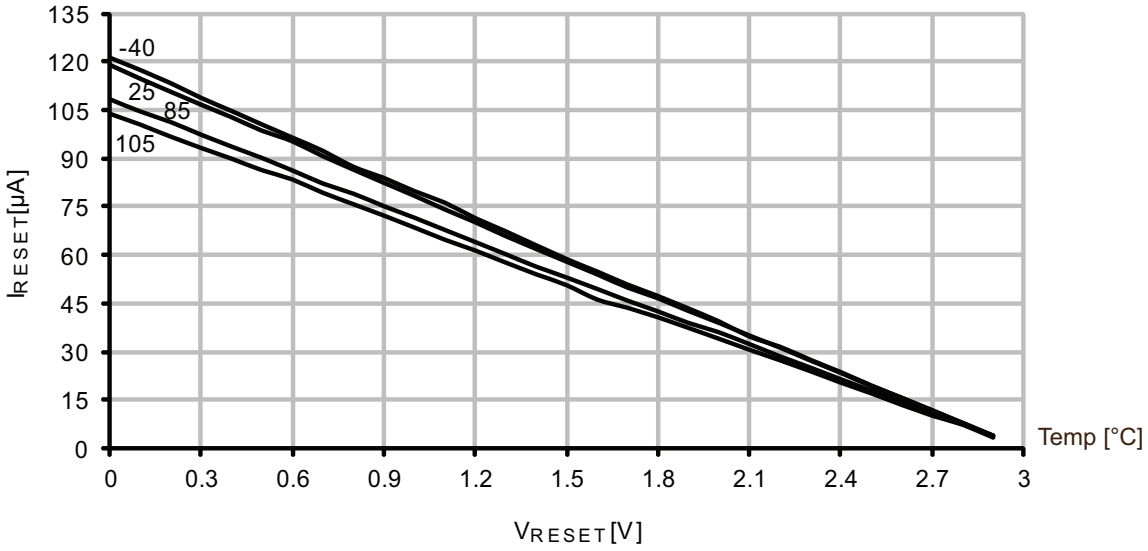


Figure 37-147. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

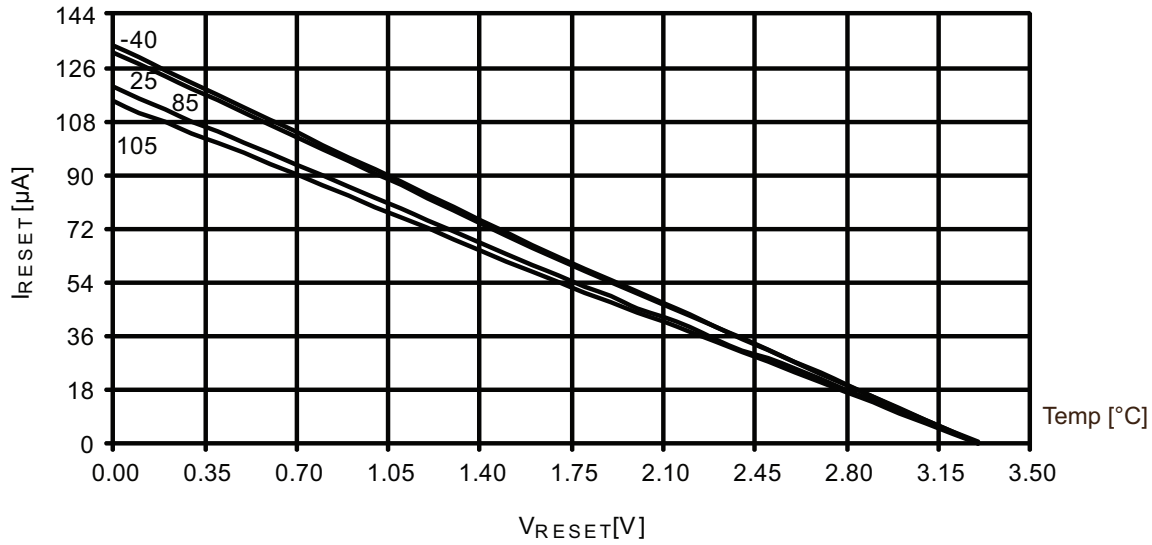


Figure 37-177. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

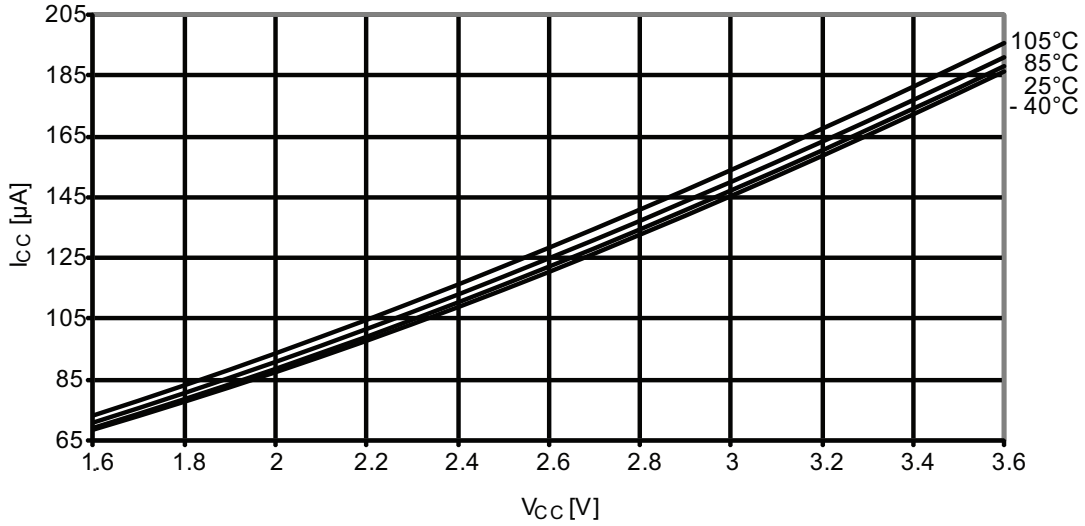
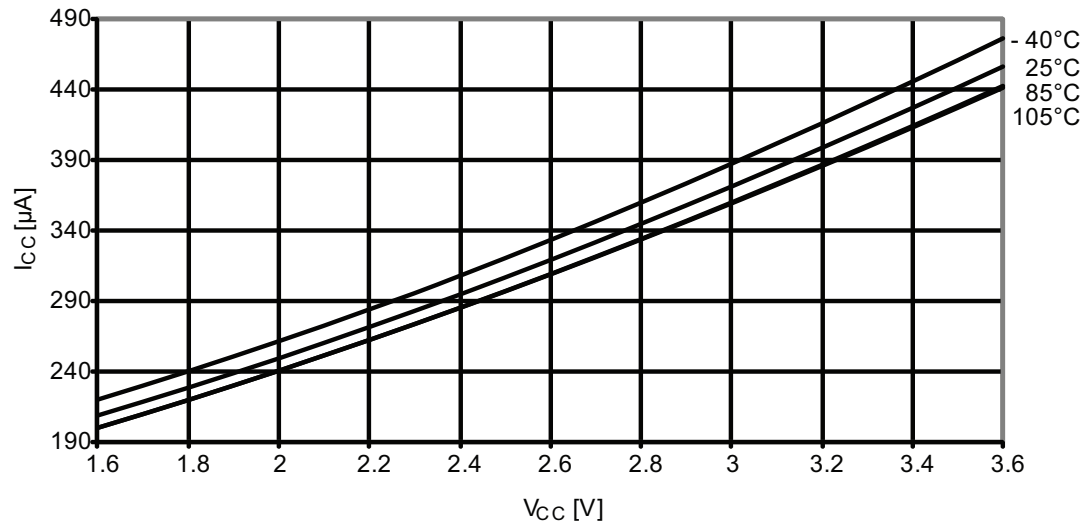


Figure 37-178. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.



37.3.8 External Reset Characteristics

Figure 37-227. Minimum Reset pin pulse width vs. V_{CC}.

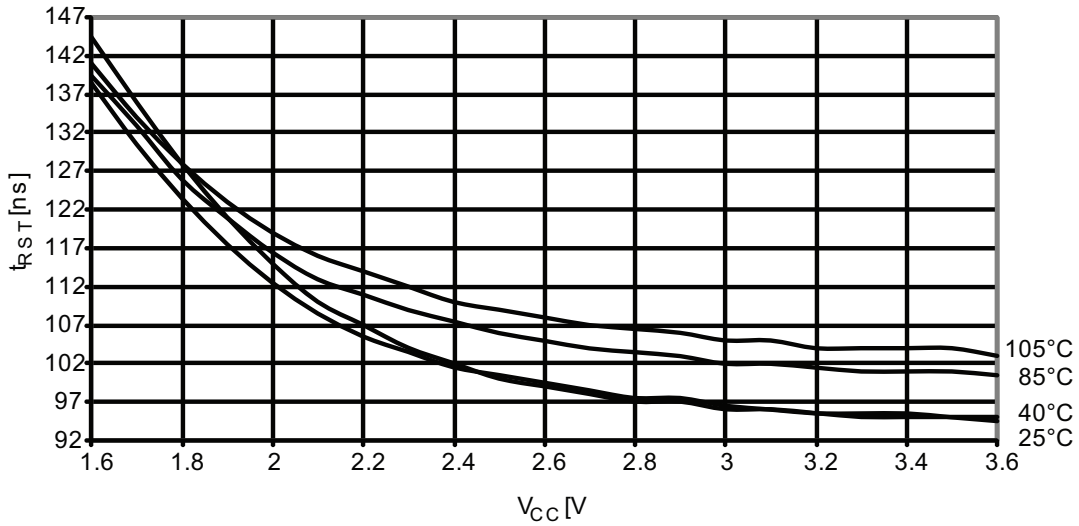


Figure 37-228. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

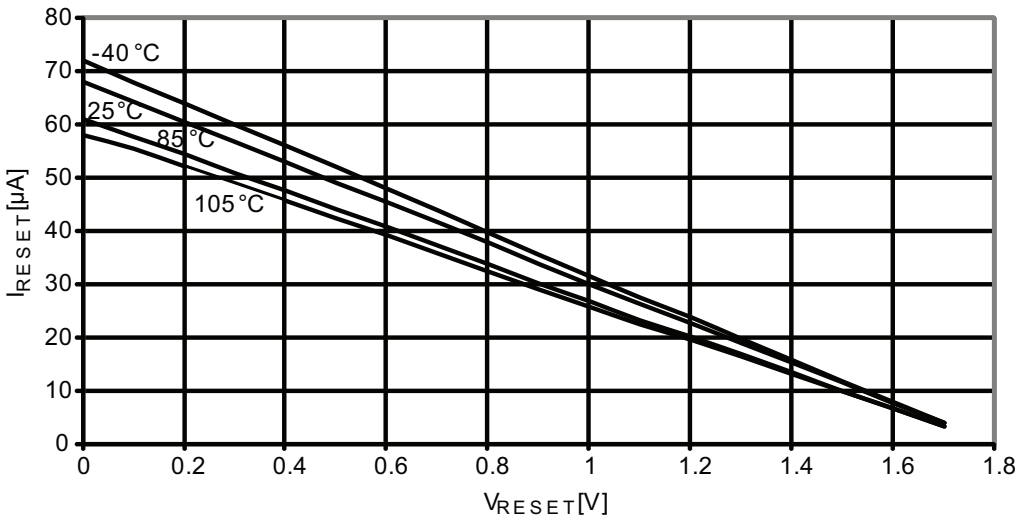


Figure 37-290. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

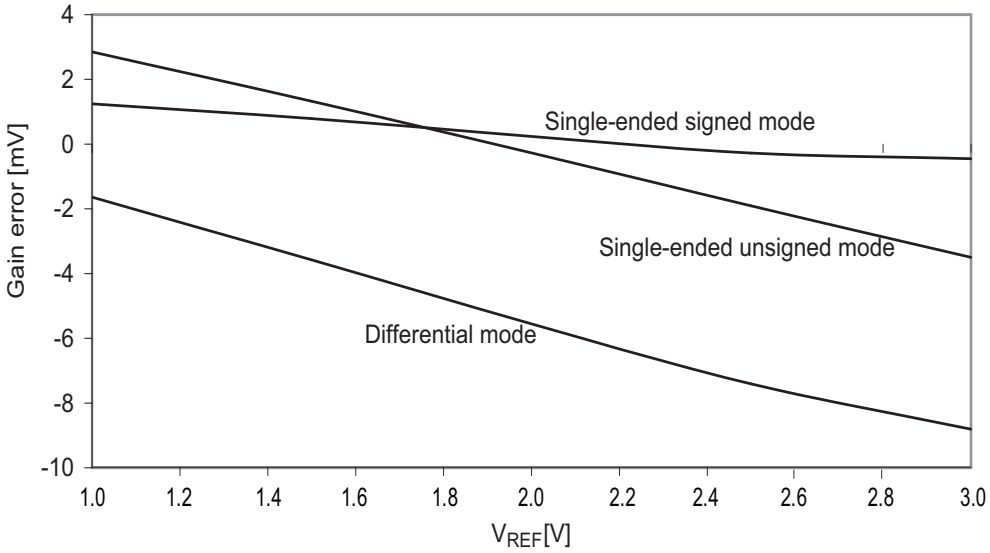


Figure 37-291. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

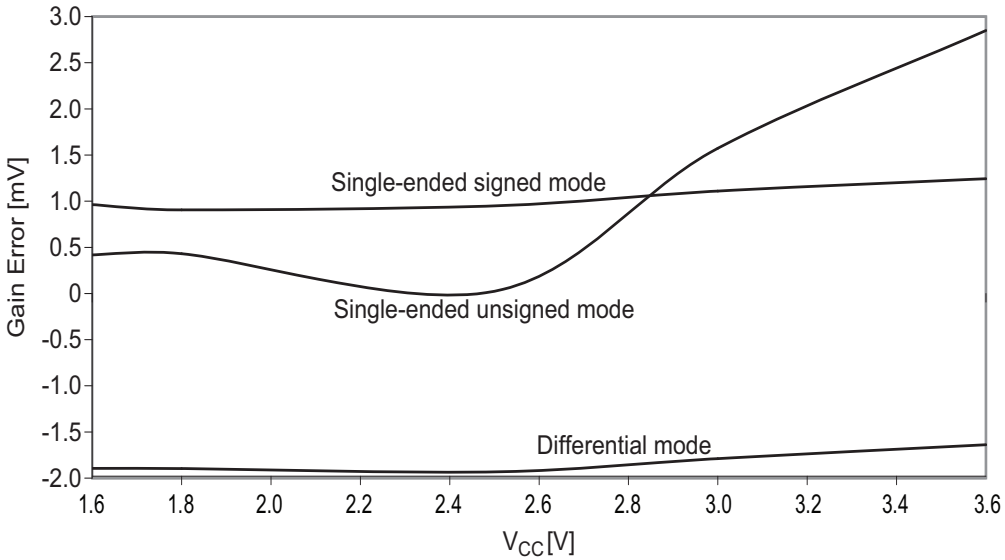
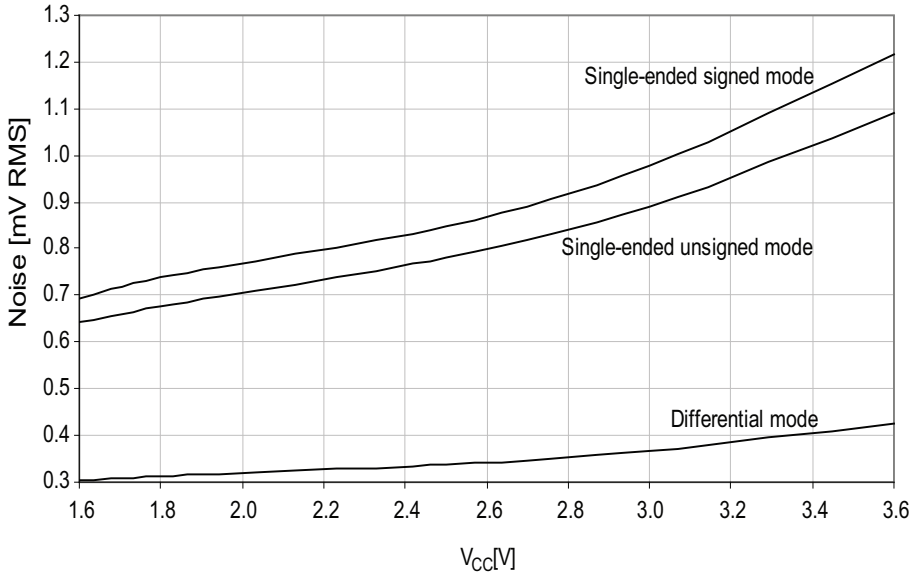


Figure 37-296. Noise vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.4.4 DAC Characteristics

Figure 37-297. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.

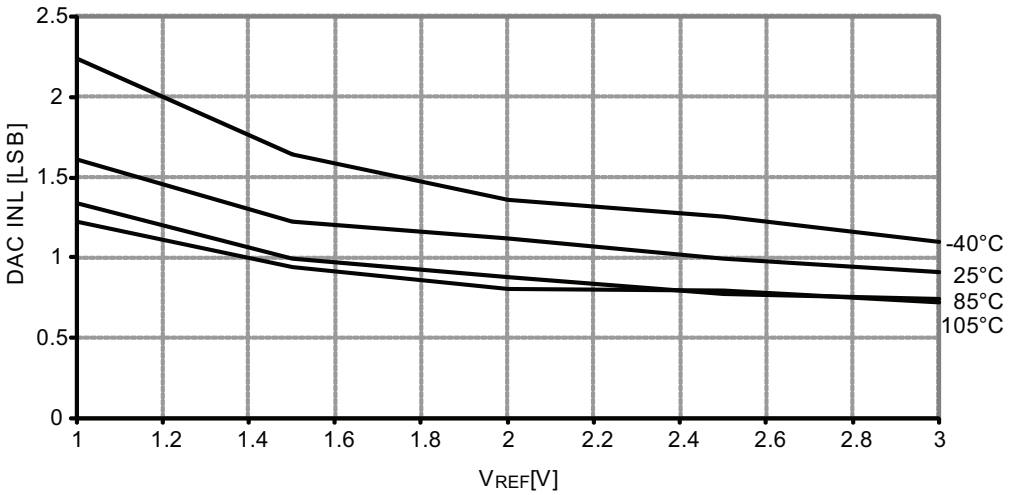
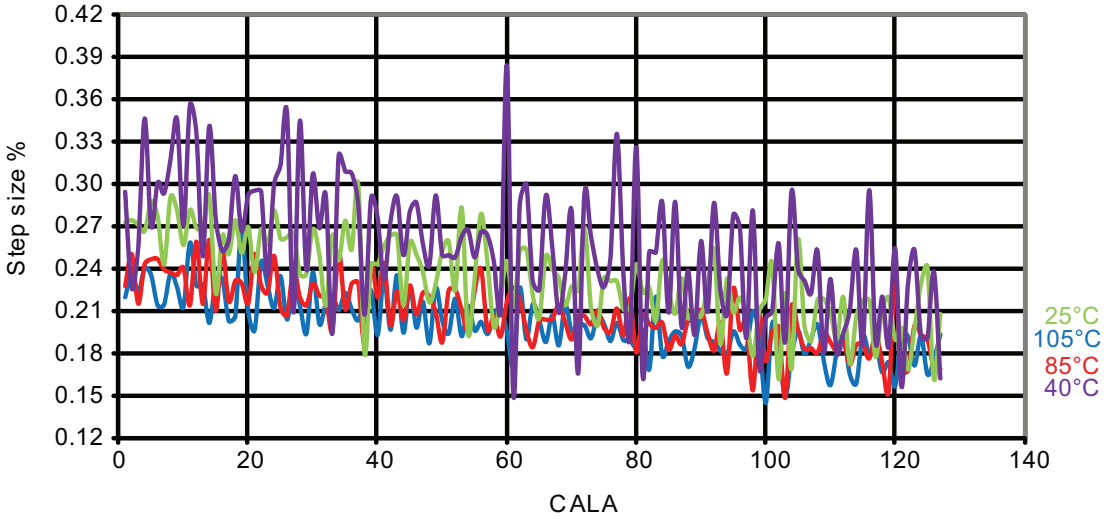


Figure 37-329. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.4.11 Two-Wire Interface characteristics

Figure 37-330. SDA hold time vs. V_{CC}.