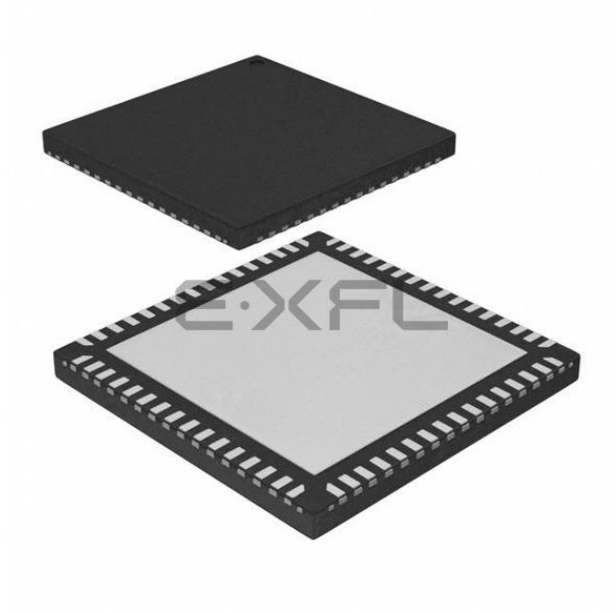

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192a3u-m7r

3. For packaging information, see “Packaging information” on page 71.
4. Tape and Reel.

Package Type	
64A	64-lead, 14 x 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
64M2	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

13. WDT – Watchdog Timer

13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

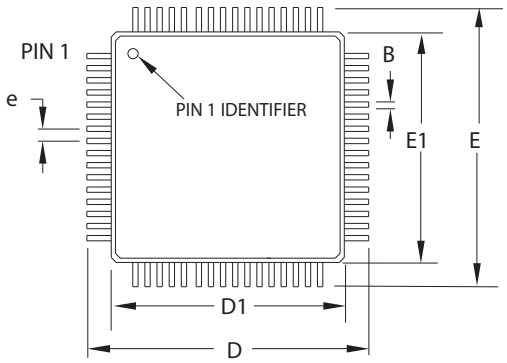
The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

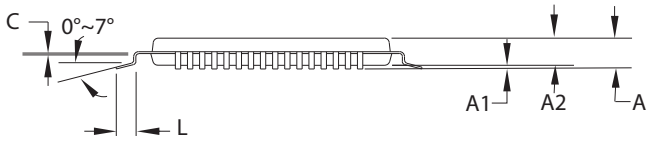
The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

35. Packaging information

35.1 64A





COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30–	0.45		
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	64A, 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	C

Table 36-14. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL (1)	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4	
			V_{CC} = 3.6V		±1.5	±4	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL (1)	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3	lsb
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4		lsb
	Gain calibration step size				4		lsb
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

36.1.8 Analog Comparator Characteristics

Table 36-15. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input Offset Voltage			<±10		mV
I_{lk}	Input Leakage Current			<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, None			0		mV
V_{hys2}	Hysteresis, Small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, Large	mode = HS		30		mV
		mode = LP		60		

36.1.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-24. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.1.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-25. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

36.1.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-26. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

Table 36-37. Current consumption for modules and peripherals.

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				27		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		µA
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			220		µA
	Watchdog Timer				1		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				100		µA
	Temperature sensor				95		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low Power mode		1.1		
	AC	High Speed Mode			330		µA
		Low Power Mode			130		
	DMA	615KBps between I/O registers and SRAM			115		µA
	Timer/Counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are givenAll parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

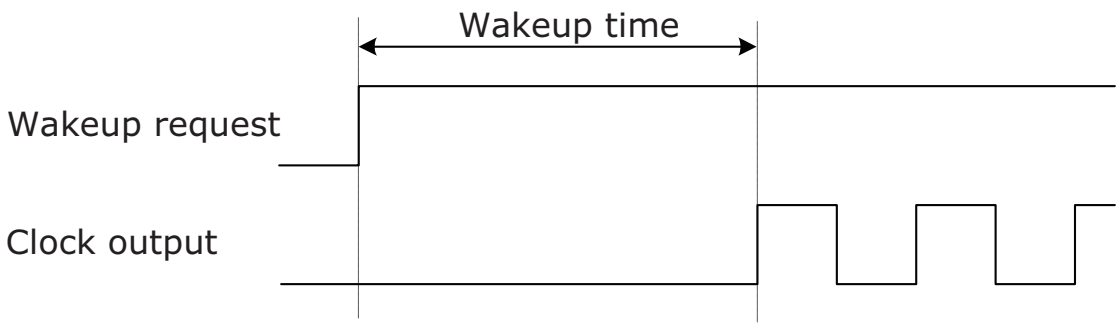
36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.



36.3.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 36-71. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} [1]/ I_{OL} [2]	I/O pin source/sink current			-20		20	mA
V_{IH}	High Level Input Voltage	V_{CC} = 2.7 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.0 - 2.7V		0.7*V_{CC}		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.0V		0.8*V_{CC}		V_{CC}+0.3	
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7- 3.6V		-0.3		0.8	V
		V_{CC} = 2.0 - 2.7V		-0.3		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.0V		-0.3		0.2*V_{CC}	
V_{OH}	High Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	0.94*V_{CC}		V
		V_{CC} = 2.3 - 2.7V	I_{OH} = -1mA	2.0	0.96*V_{CC}		
			I_{OH} = -2mA	1.7	0.92*V_{CC}		
		V_{CC} = 3.3V	I_{OH} = -8mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -6mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -2mA	1.4	1.6		
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		0.05*V_{CC}	0.4	V
		V_{CC} = 2.3 - 2.7V	I_{OL} = 1mA		0.03*V_{CC}	0.4	
			I_{OL} = 2mA		0.06*V_{CC}	0.7	
		V_{CC} = 3.3V	I_{OL} = 15mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 10mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 5mA		0.3	0.46	
I_{IN}	Input Leakage Current	T = 25°C			<0.001	0.1	µA
R_P	Pull/Buss keeper Resistor				27		kΩ
t_r	Rise time	No load			4		ns
			slew rate limitation		7		

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

36.4.6 ADC characteristics

Table 36-104. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-105. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling Time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

37.1.1.3 Power-down mode supply current

Figure 37-15. Power-down mode supply current vs. V_{CC}.
All functions disabled.

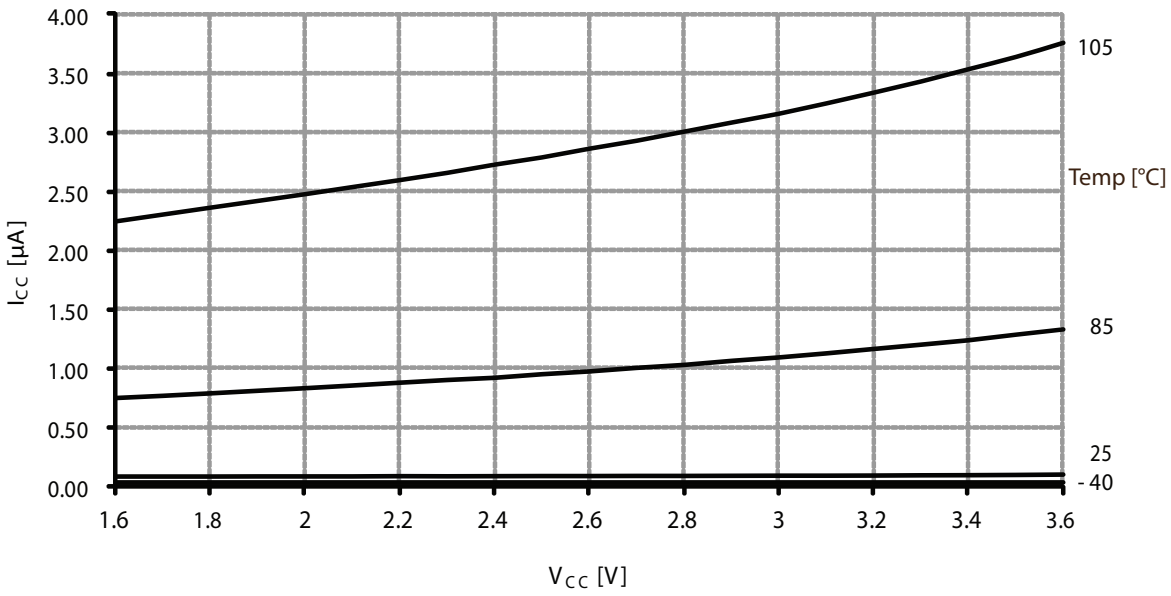
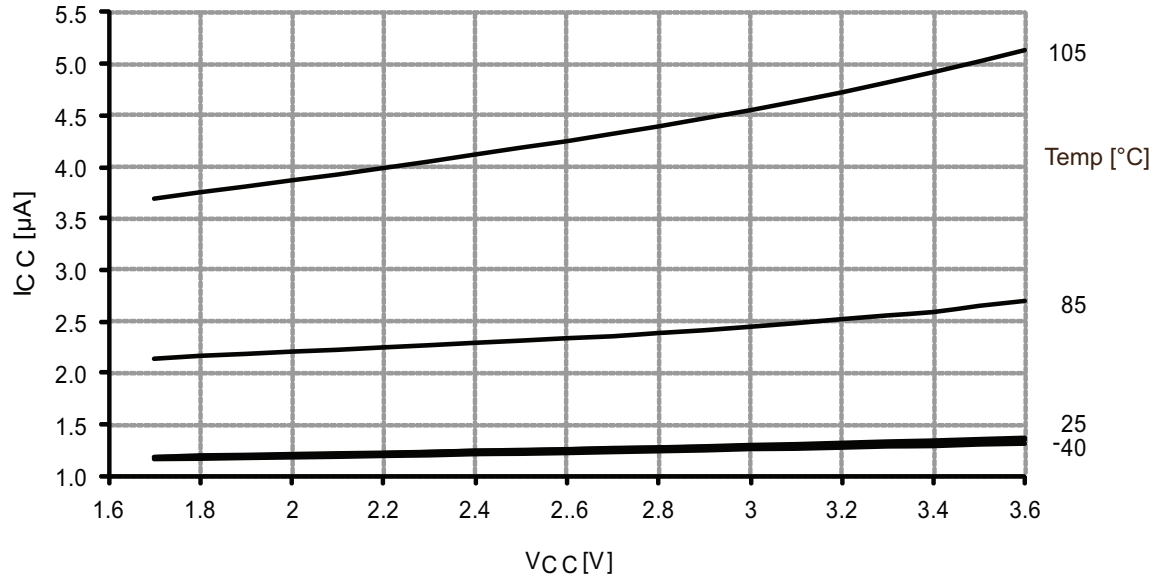


Figure 37-16. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.



37.1.7 BOD Characteristics

Figure 37-59. BOD thresholds vs. temperature.

BOD level = 1.6V.

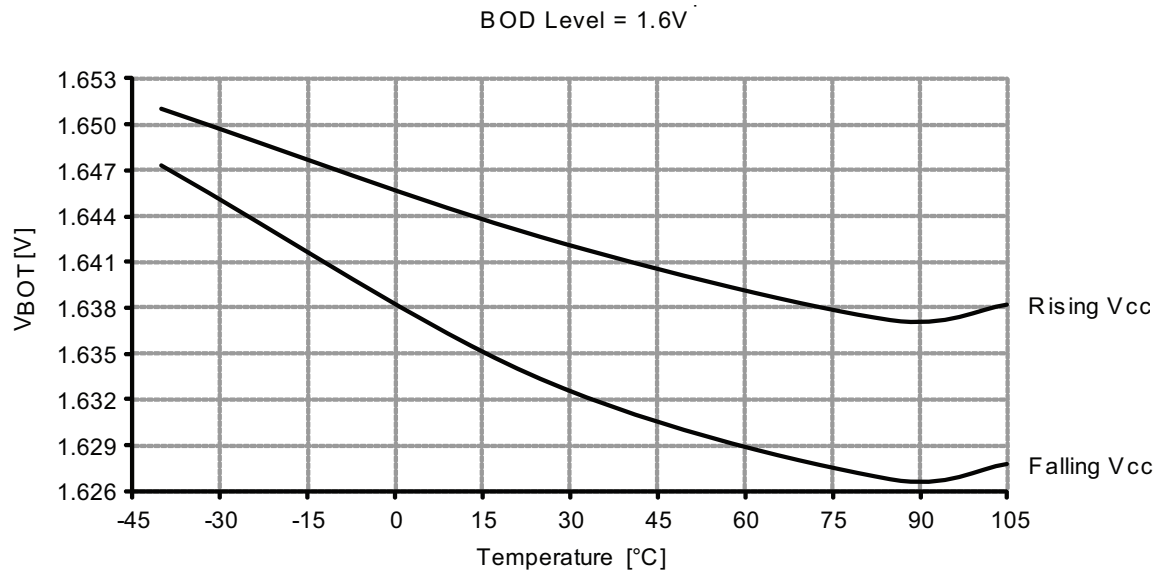


Figure 37-60. BOD thresholds vs. temperature.

BOD level = 3.0V.

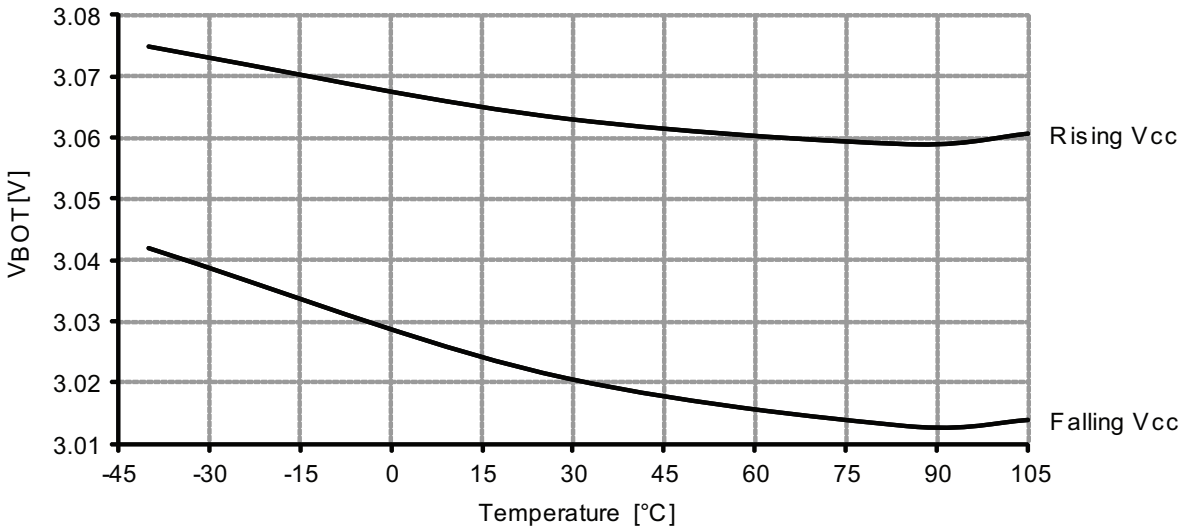


Figure 37-108. I/O pin output voltage vs. source current.

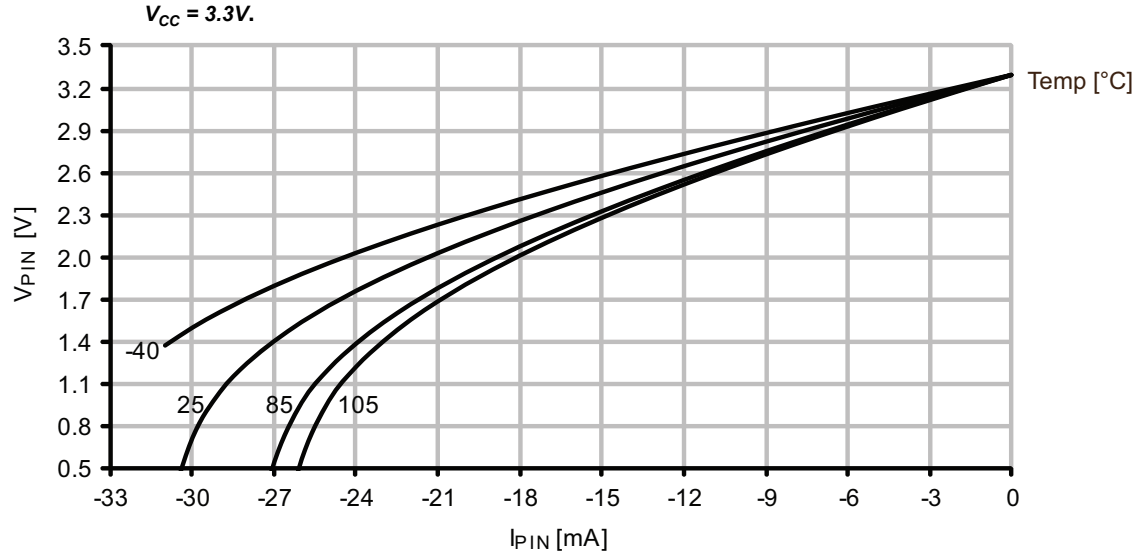
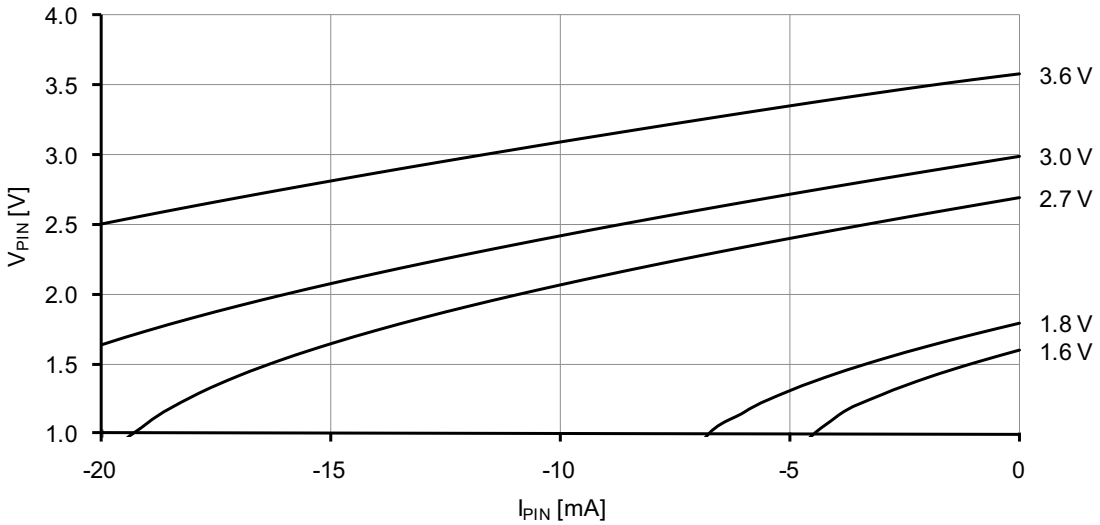


Figure 37-109. I/O pin output voltage vs. source current.



37.2.5 Analog Comparator Characteristics

Figure 37-134. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis.

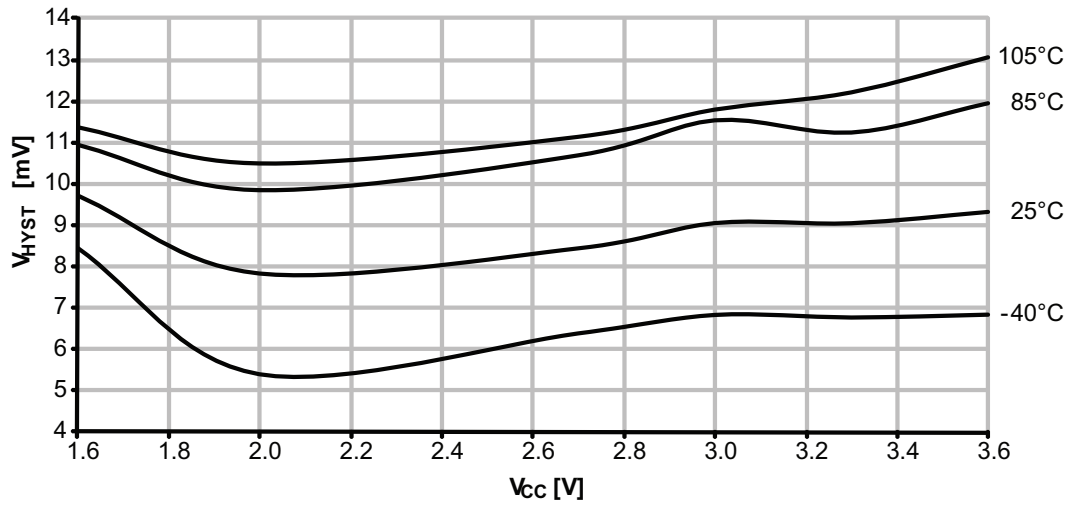
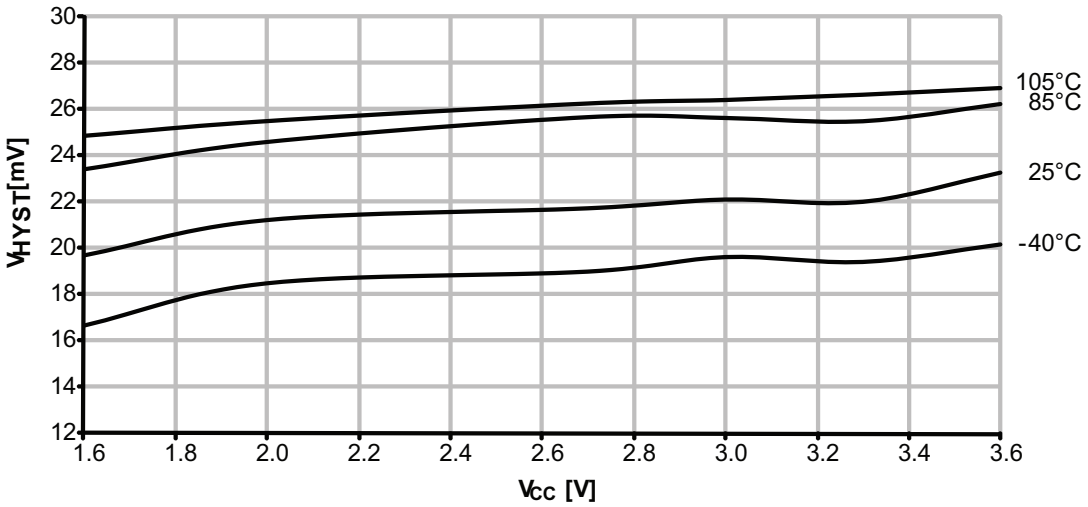


Figure 37-135. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis.



37.2.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-161. 48MHz internal oscillator frequency vs. temperature.

DFLL disabled.

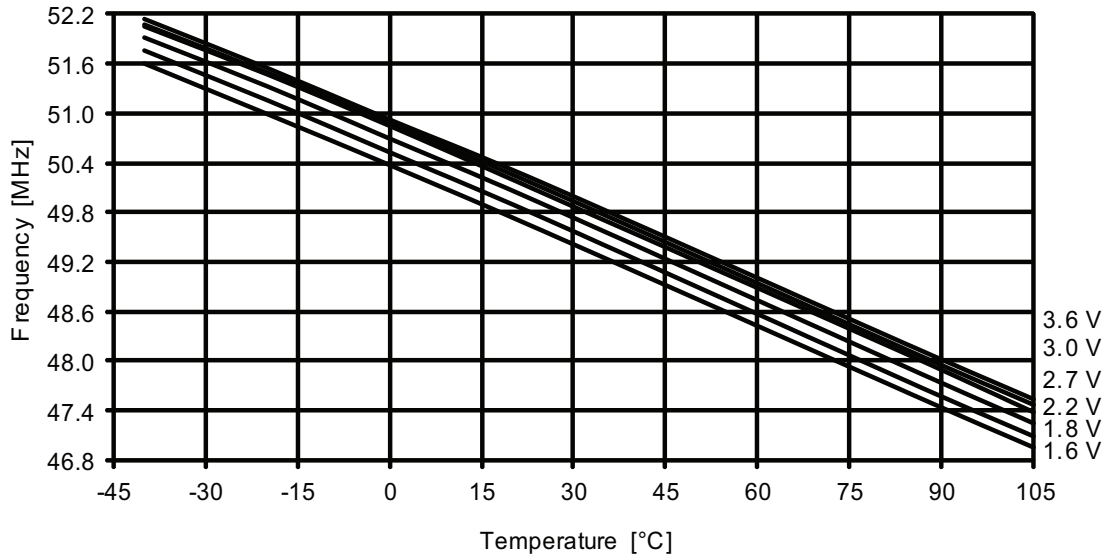


Figure 37-162. 48MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

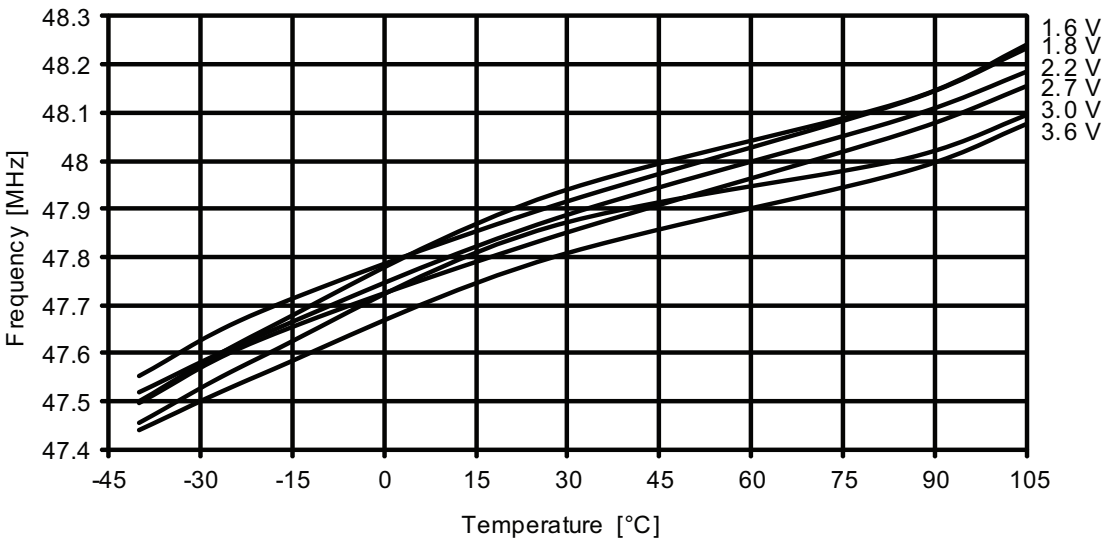


Figure 37-199. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

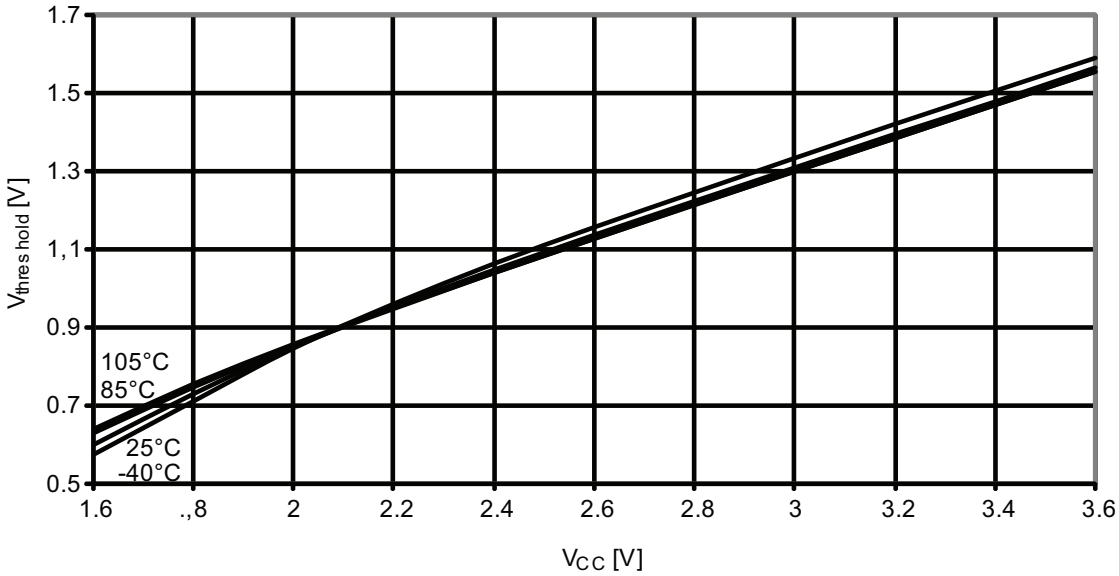


Figure 37-200. I/O pin input hysteresis vs. V_{CC} .

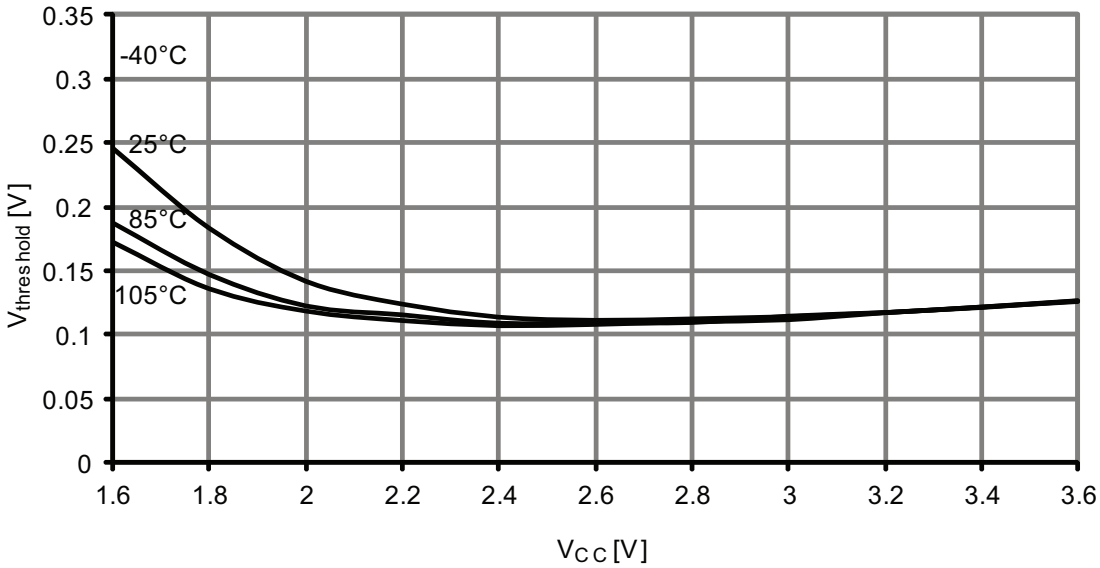


Figure 37-282. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

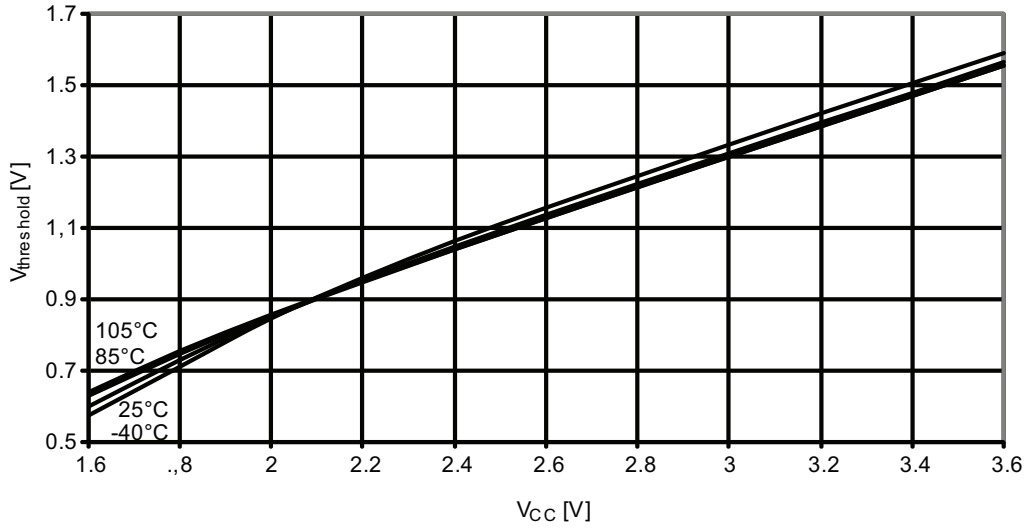


Figure 37-283. I/O pin input hysteresis vs. V_{CC}.

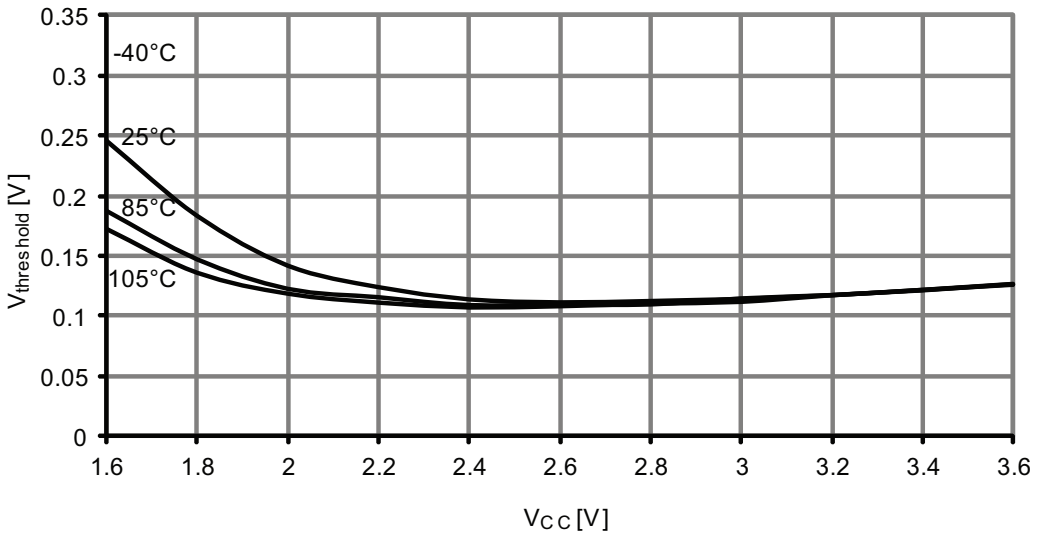


Figure 37-321. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

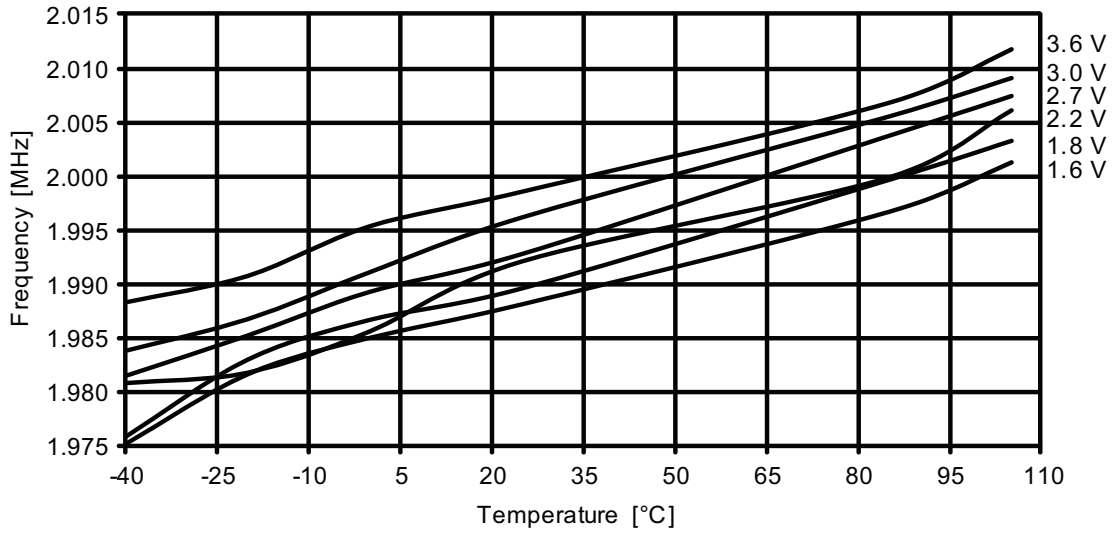


Figure 37-322. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

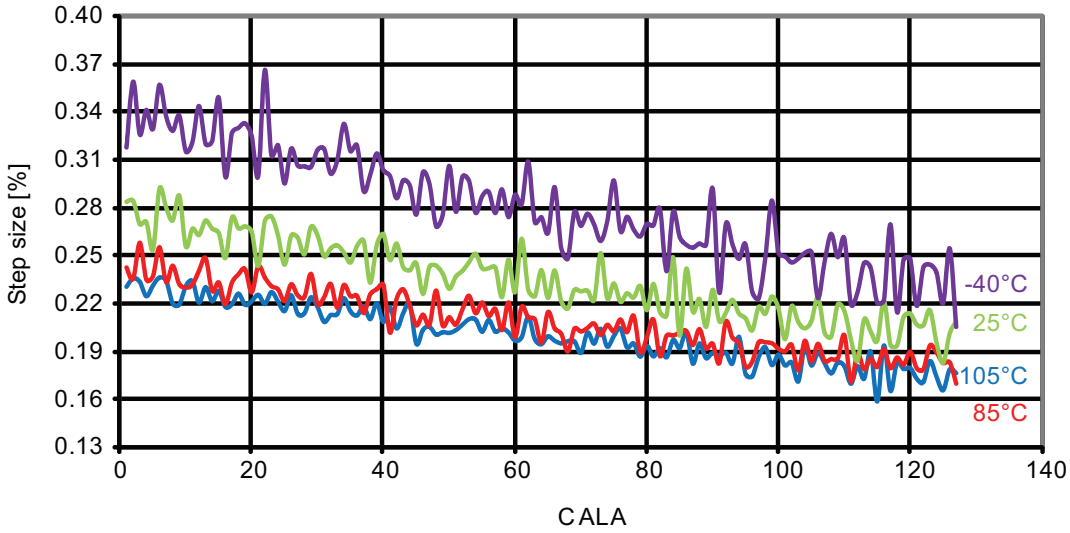


Figure 37-325. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

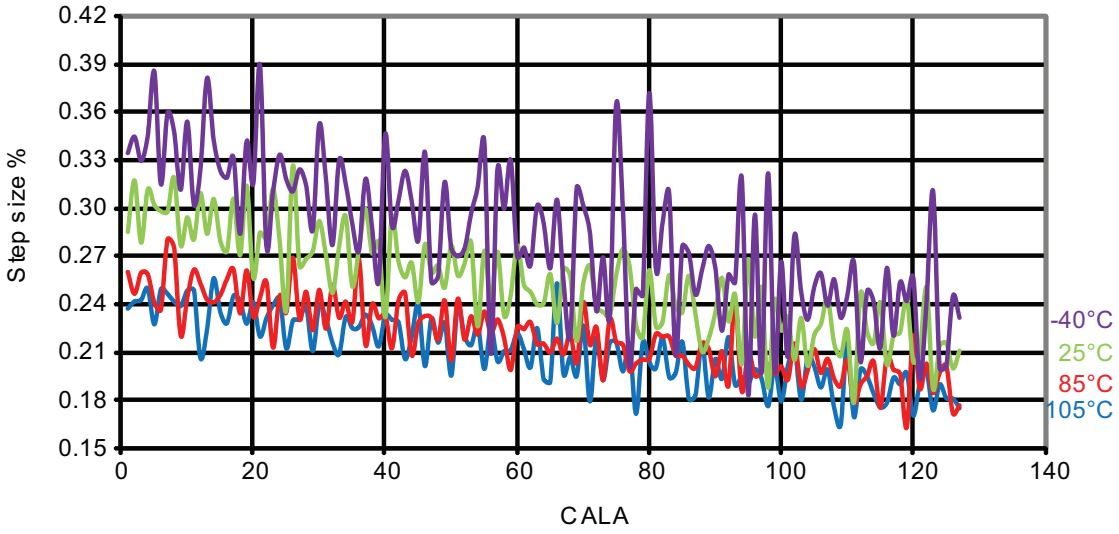


Figure 37-326. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.

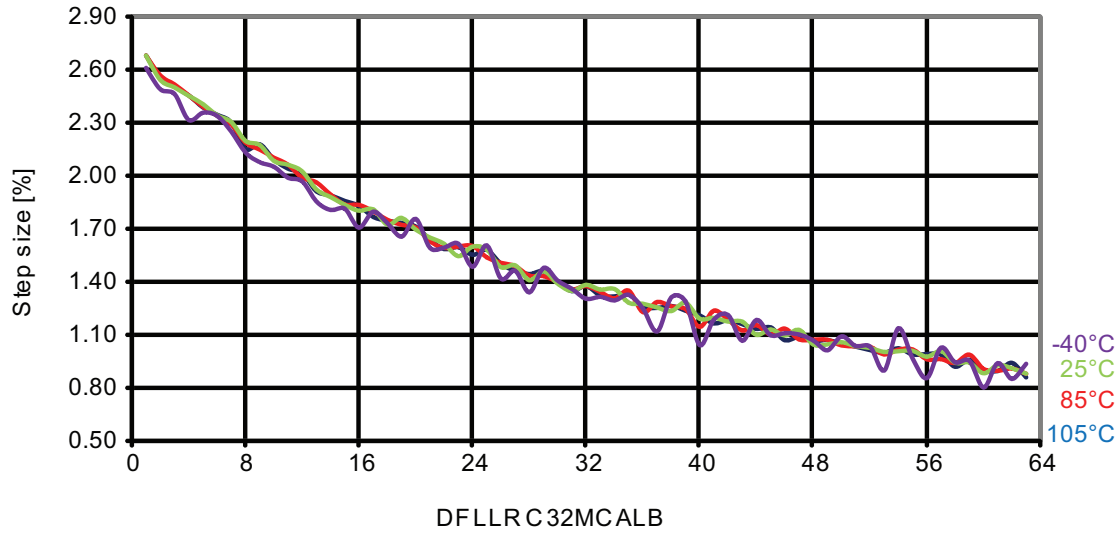
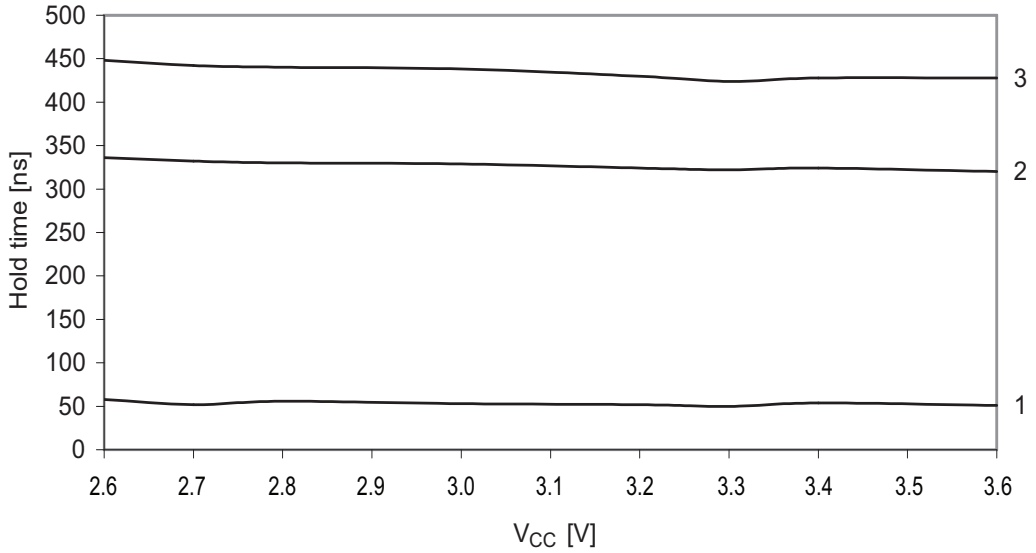


Figure 37-331. SDA hold time vs. supply voltage.



37.4.12 PDI characteristics

Figure 37-332. Maximum PDI frequency vs. V_{CC}.