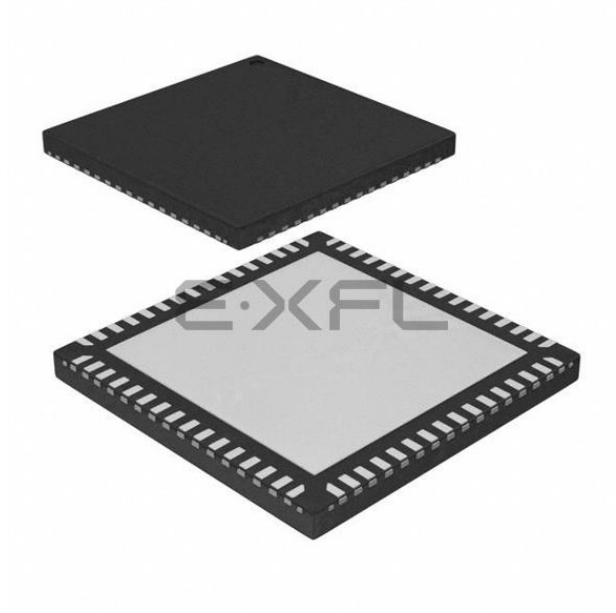
Microchip Technology - ATXMEGA192A3U-MNR Datasheet



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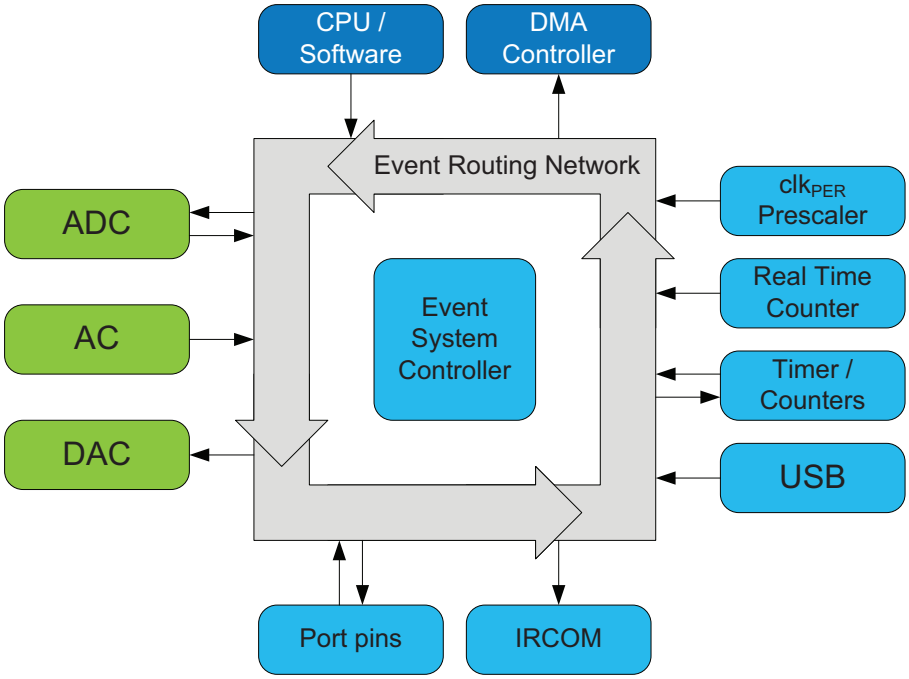
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192a3u-mnr

Figure 9-1. Event system overview and connected peripherals.



The event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to eight parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

17. TC2 - Timer/Counter Type 2

17.1 Features

- Eight eight-bit timer/counters
  - Four Low-byte timer/counter
  - Four High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

17.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2), TCD2, TCE2 and TCF2, respectively.

27. CRC – Cyclic Redundancy Check Generator

27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, DMA controller and CPU
  - Continuous CRC on data going through a DMA channel
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

Polynomial:	$x^{16}+x^{12}+x^5+1$
Hex value:	0x1021

- **CRC-32:**

Polynomial:	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Hex value:	0x04C11DB7

36.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-56. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.2.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-57. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

36.2.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-58. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.2.14.6 External clock characteristics

Figure 36-10. External clock drive waveform

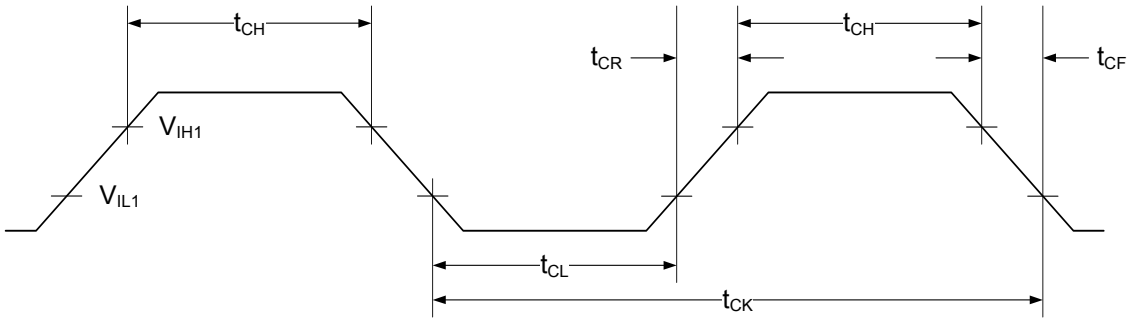


Table 36-59. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Figure 37-33. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

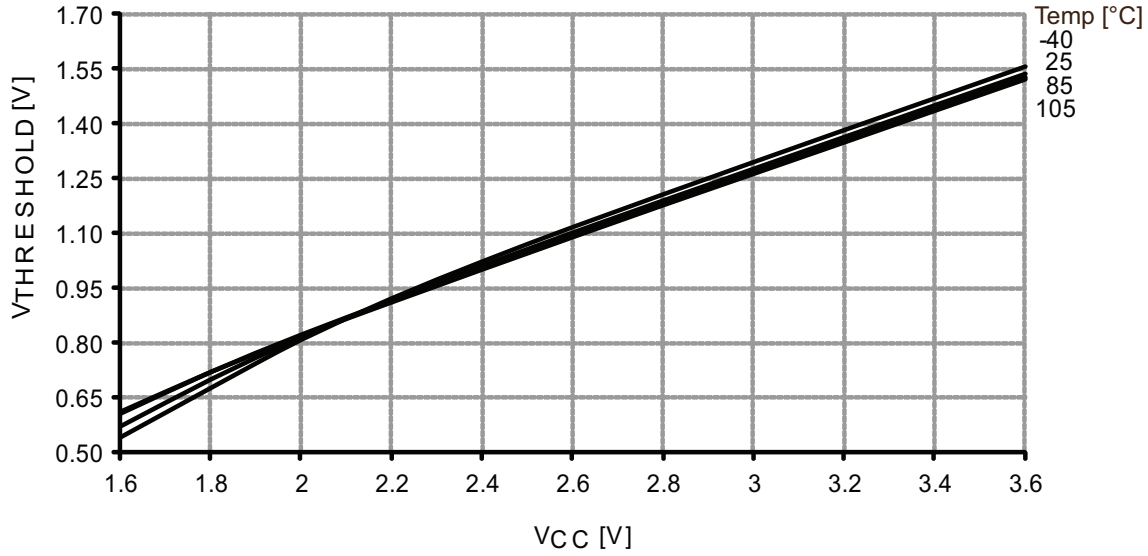


Figure 37-34. I/O pin input hysteresis vs. V_{CC}.

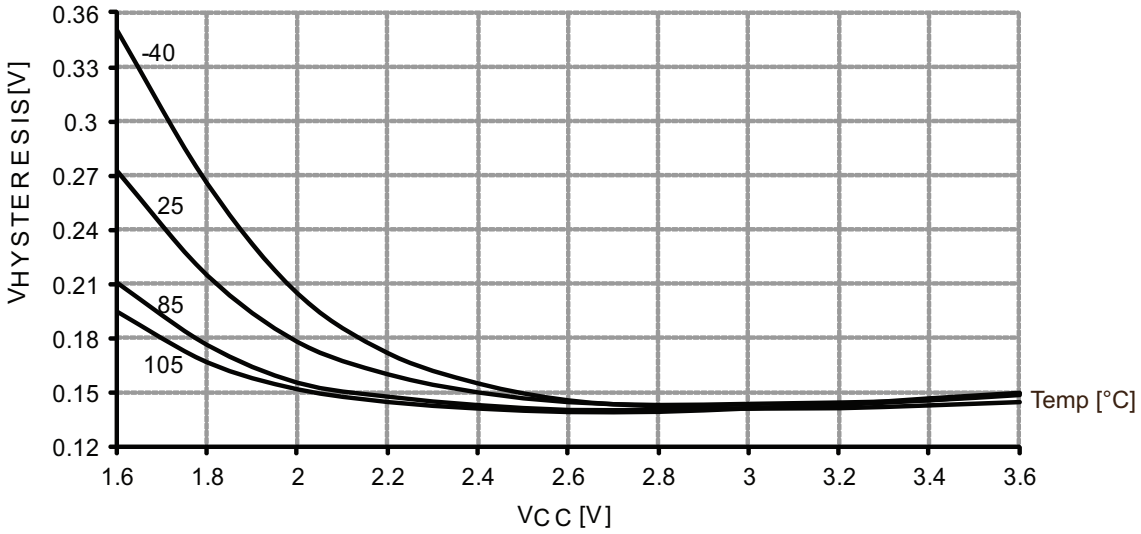


Figure 37-65. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

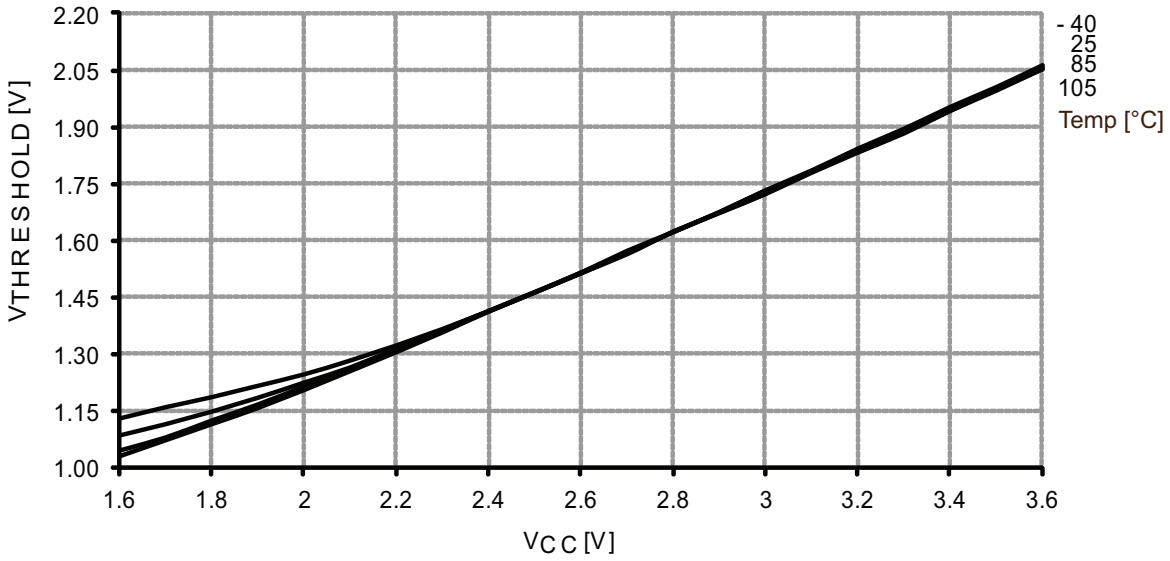


Figure 37-66. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".

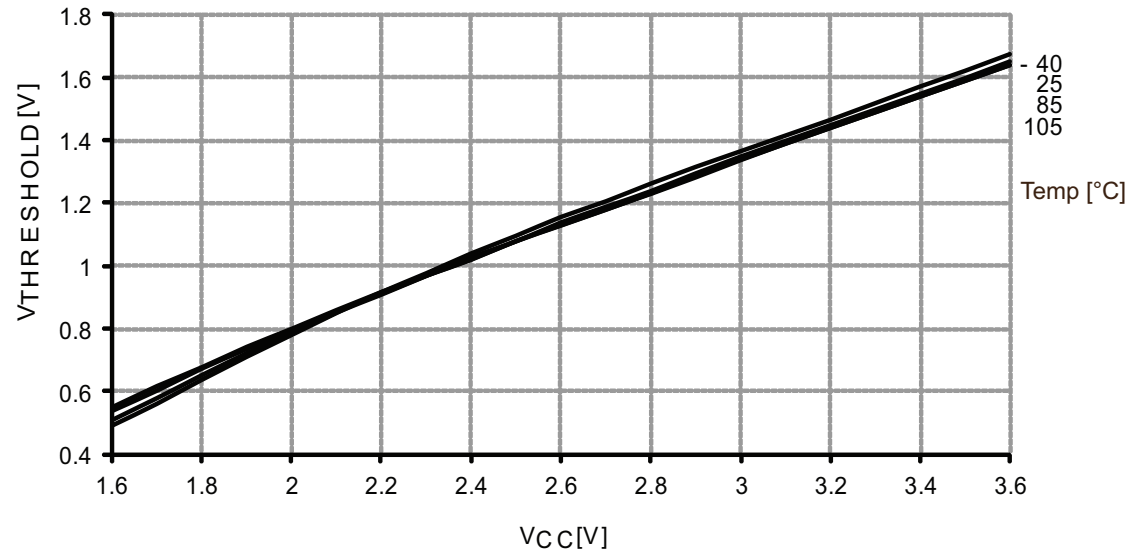
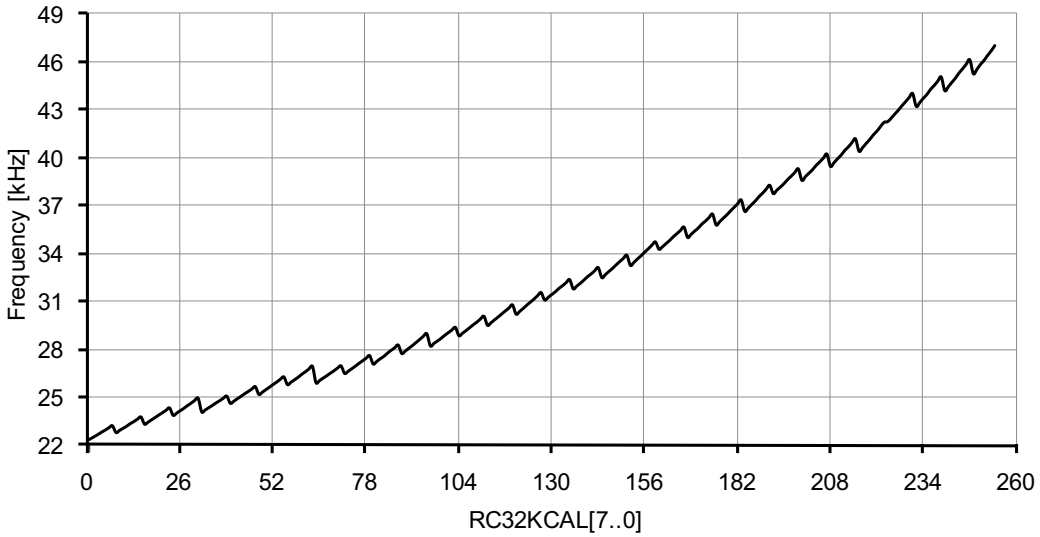


Figure 37-70. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.1.10.3 2MHz Internal Oscillator

Figure 37-71. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

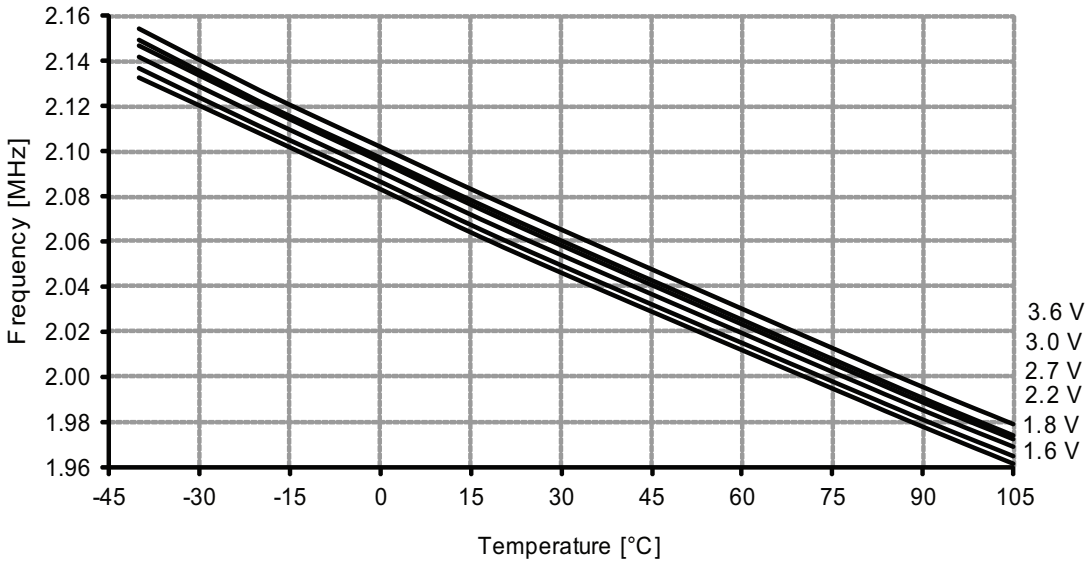


Figure 37-88. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

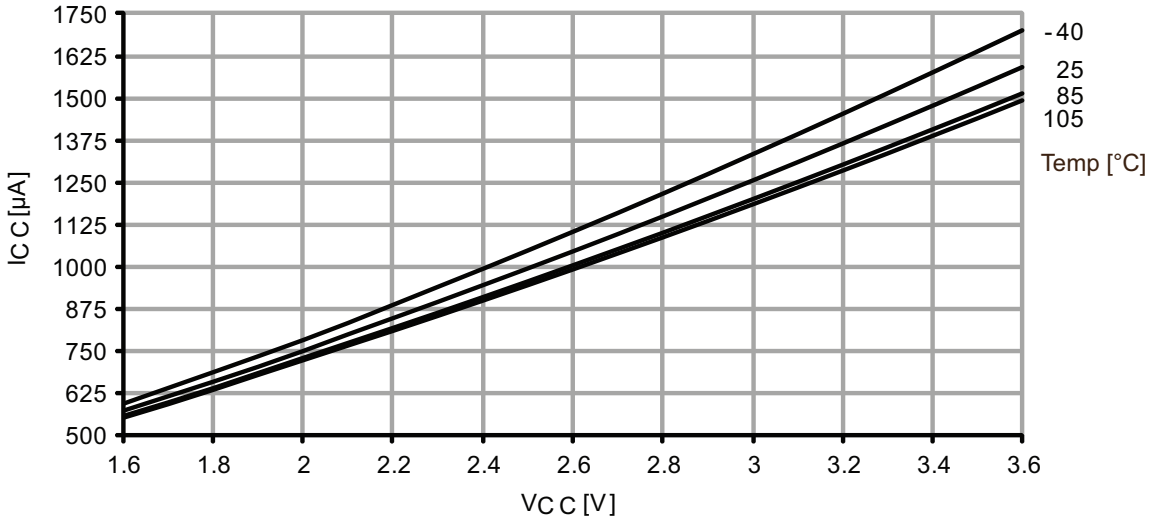
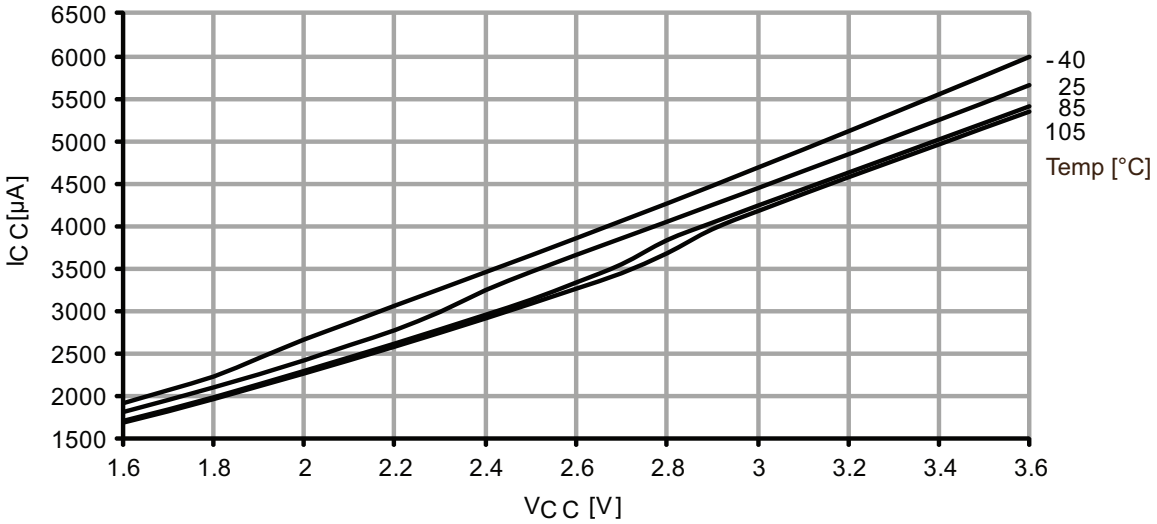


Figure 37-89. Active mode supply current vs. V_{CC}.

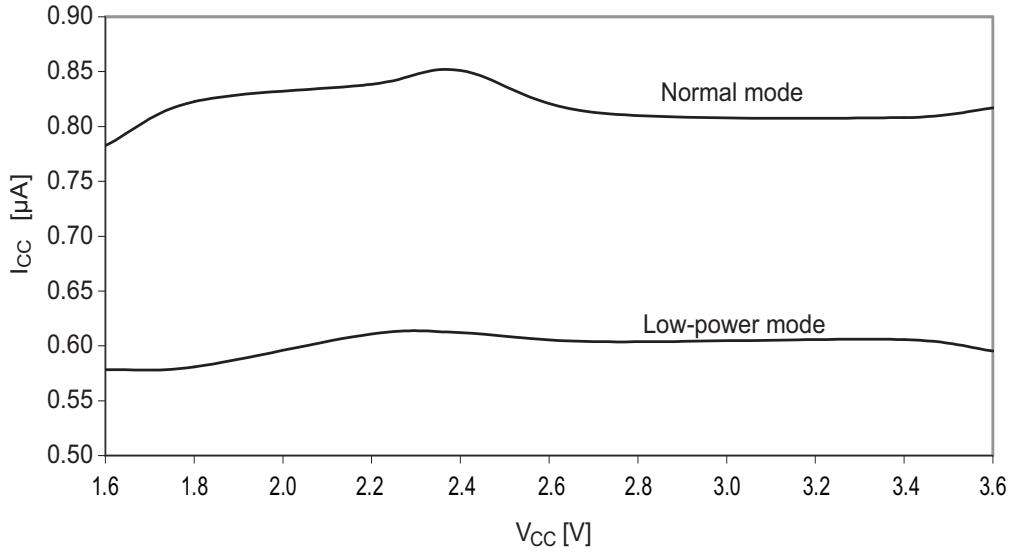
f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.



37.2.1.4 Power-save mode supply current

Figure 37-100. Power-save mode supply current vs. V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.2.1.5 Standby mode supply current

Figure 37-101. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

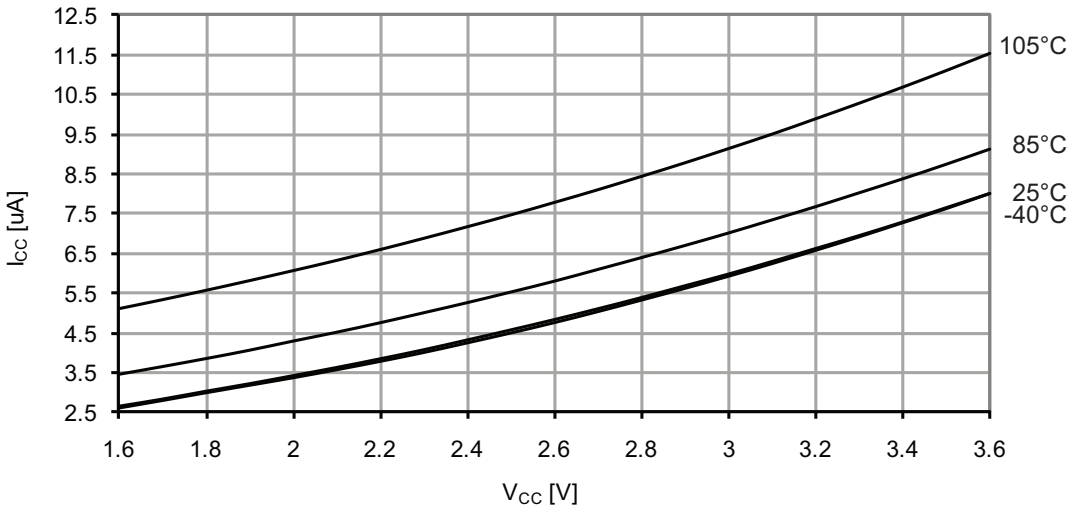


Figure 37-104. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

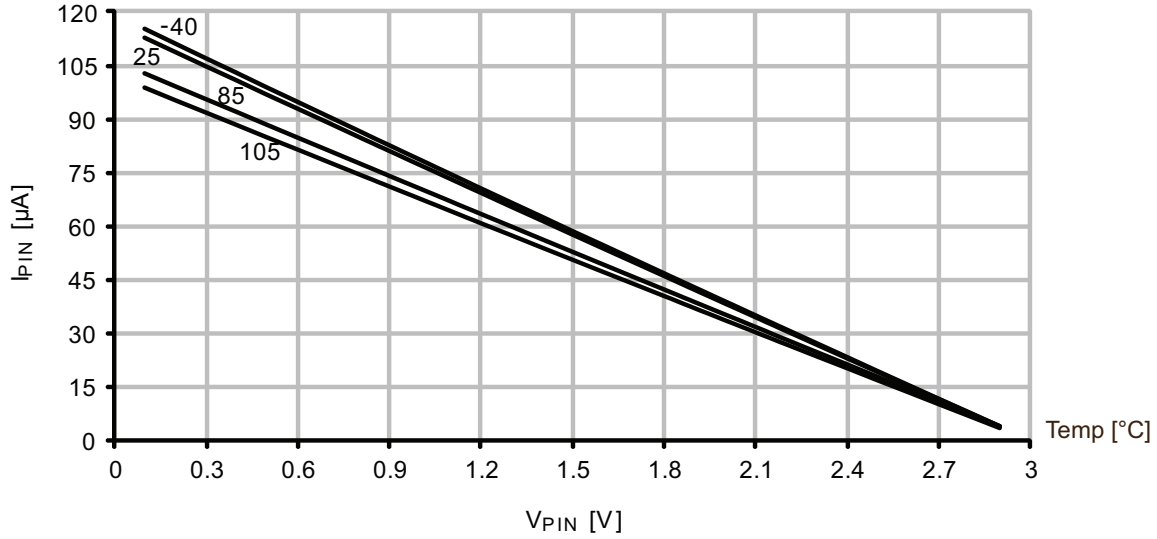


Figure 37-105. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.

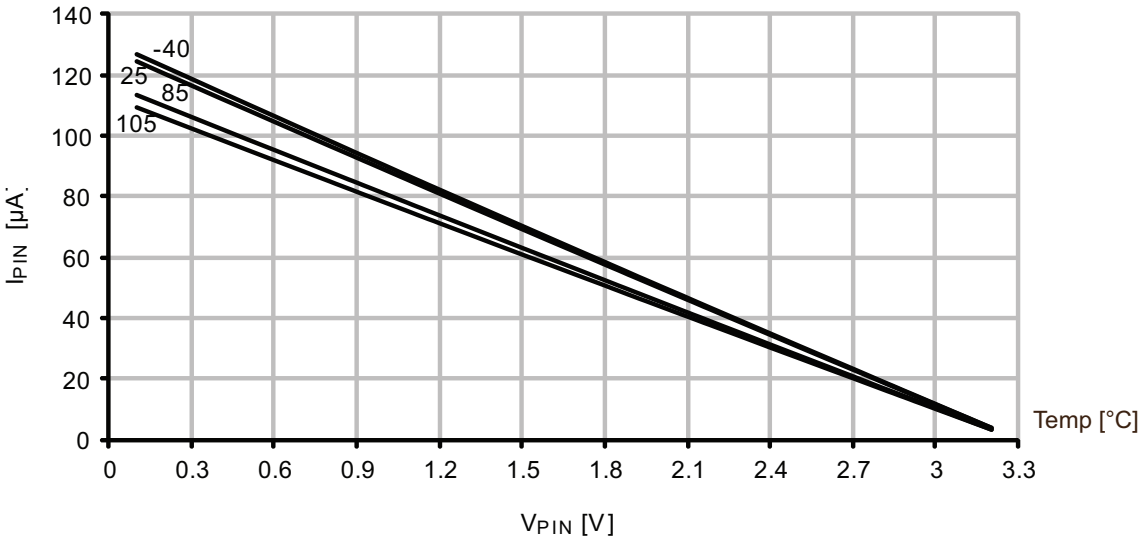
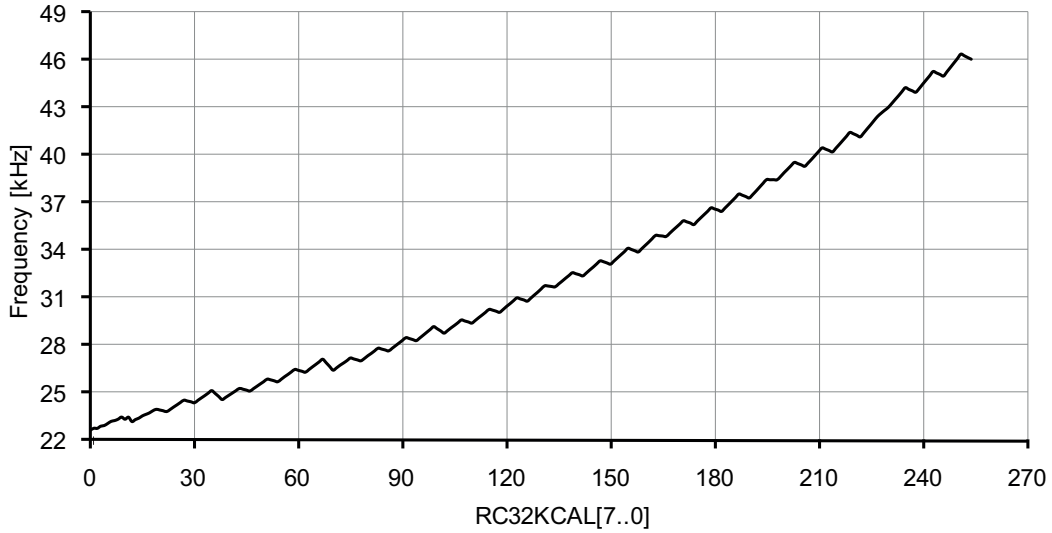


Figure 37-153. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.2.10.3 2MHz Internal Oscillator

Figure 37-154. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

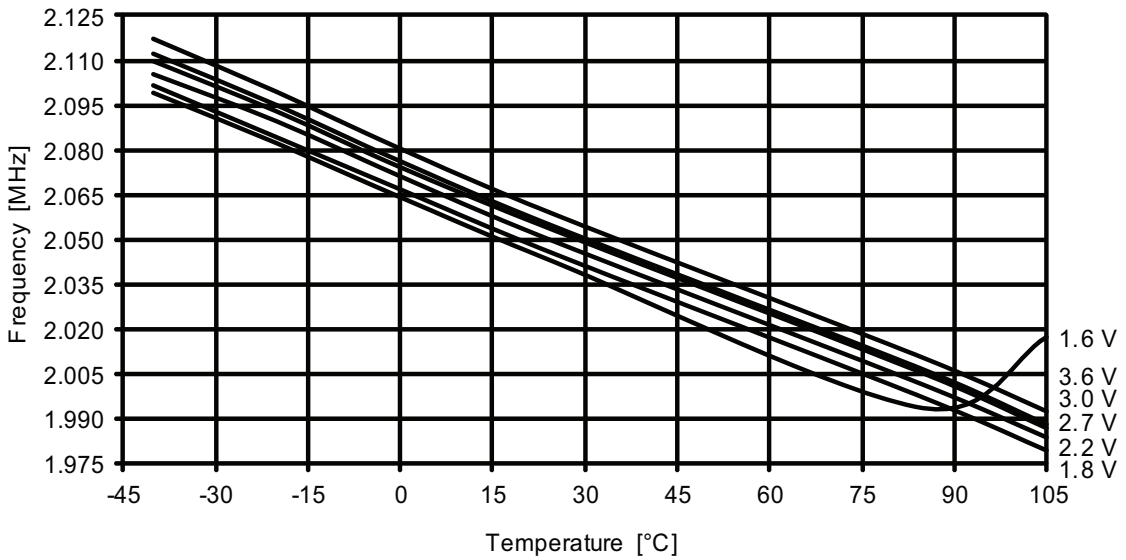


Figure 37-155. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

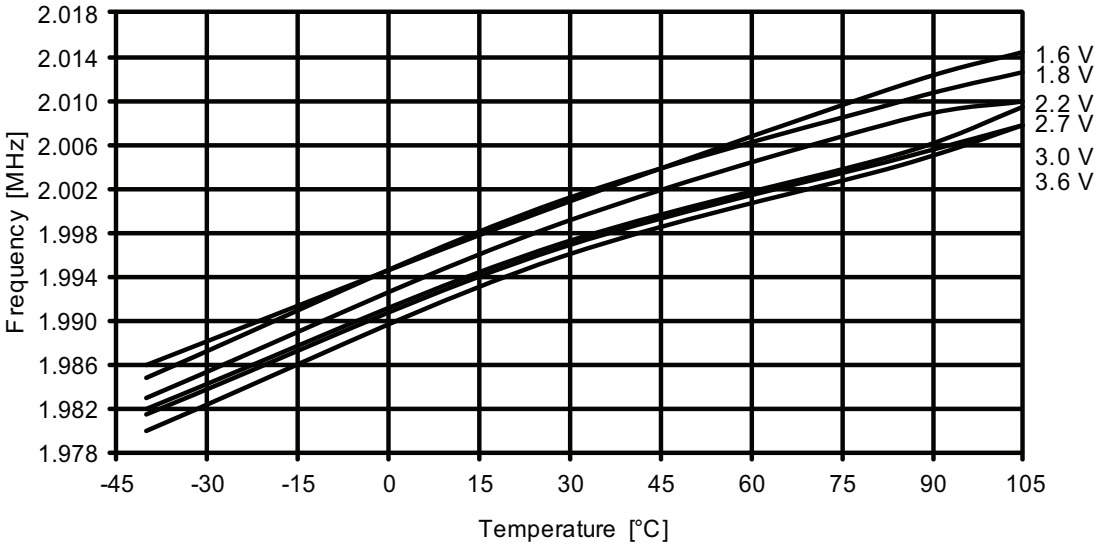
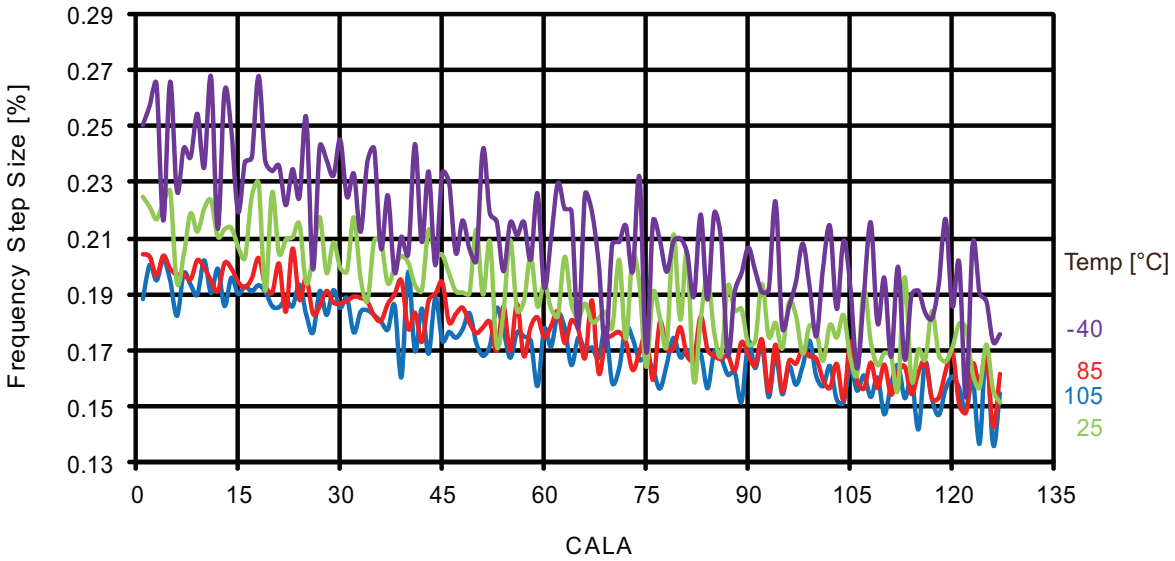


Figure 37-156. 2MHz internal oscillator CALA calibration step size.

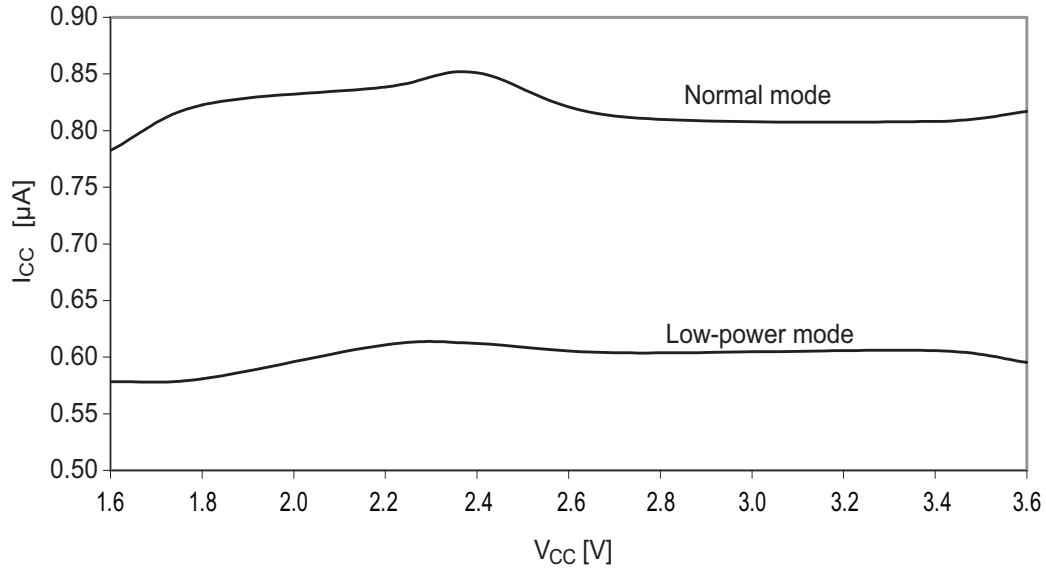
V_{CC} = 3V.



37.3.1.4 Power-save mode supply current

Figure 37-183. Power-save mode supply current vs. V_{CC}.

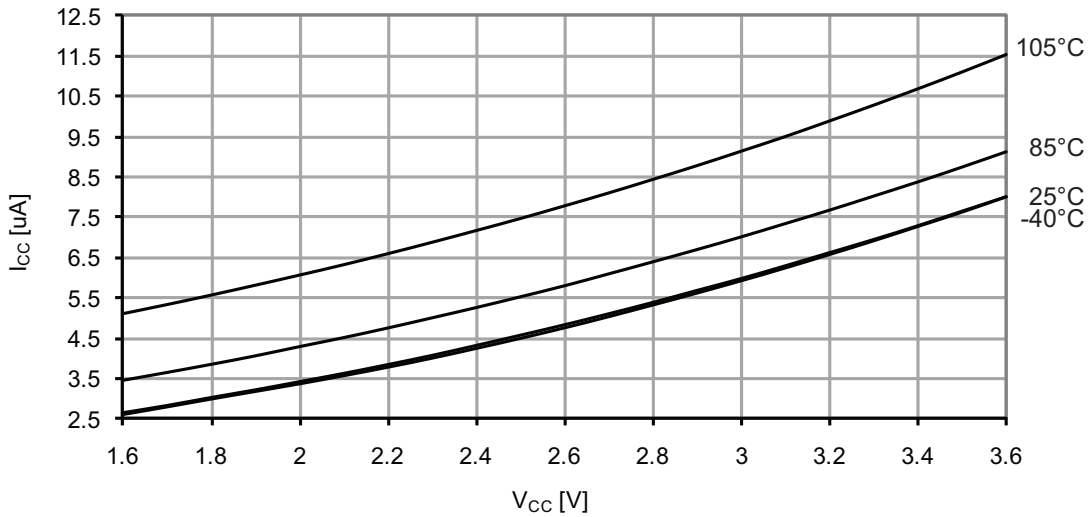
Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.3.1.5 Standby mode supply current

Figure 37-184. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.



37.3.2.3 Thresholds and Hysteresis

Figure 37-197. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

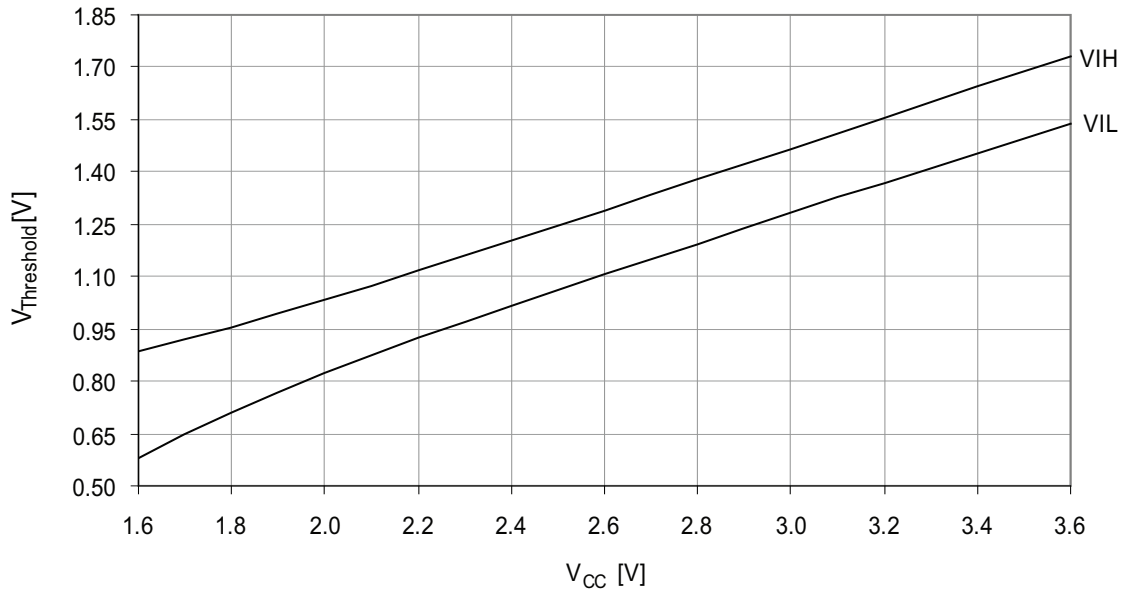


Figure 37-198. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

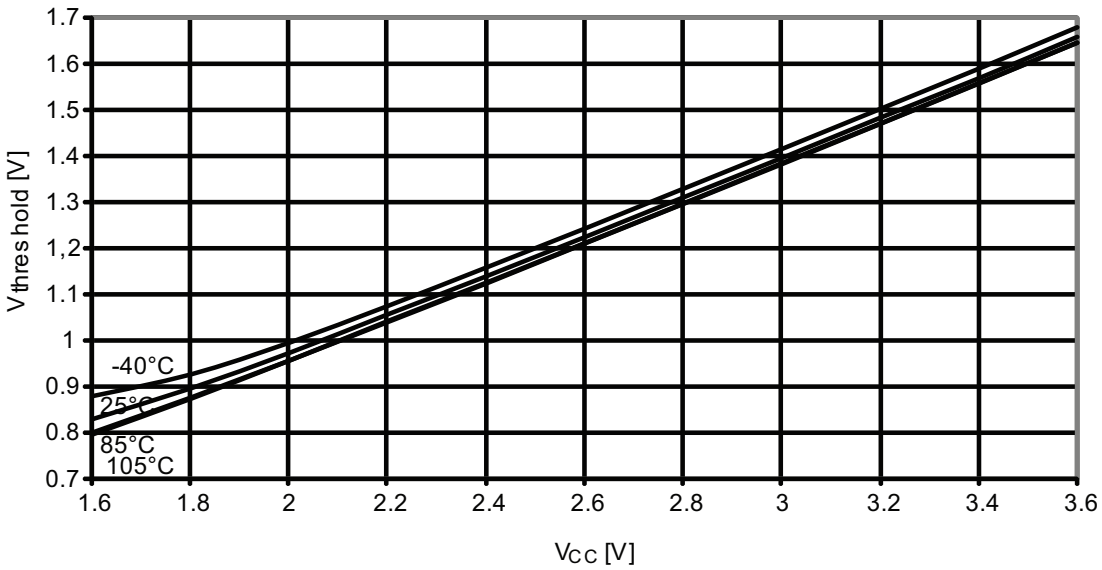
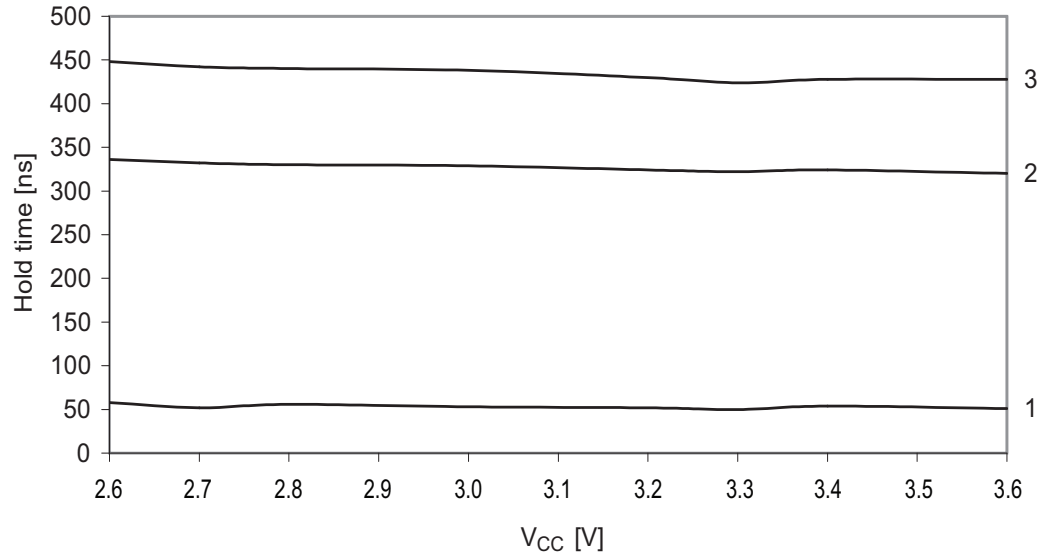


Figure 37-248. SDA hold time vs. supply voltage.



37.3.12 PDI characteristics

Figure 37-249. Maximum PDI frequency vs. V_{CC}.

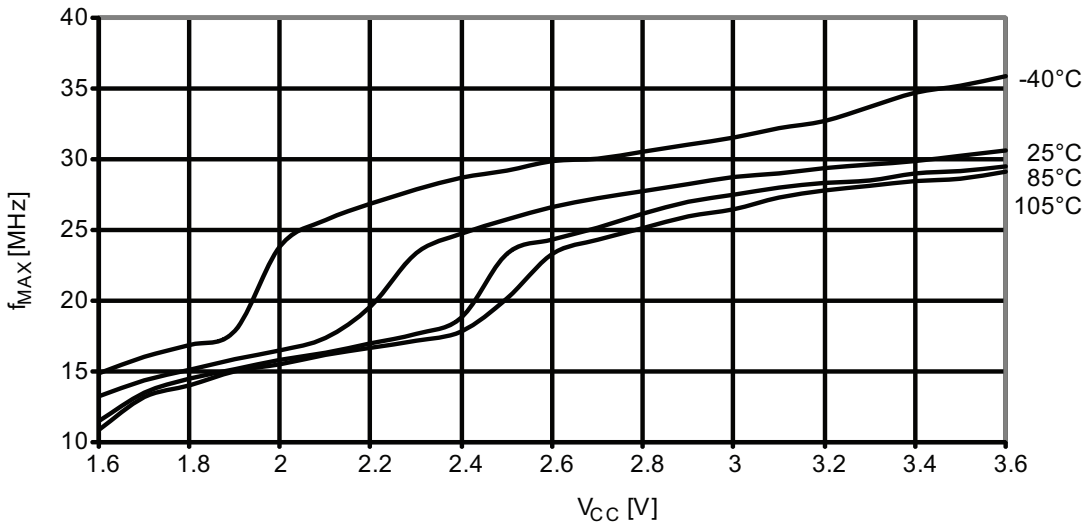
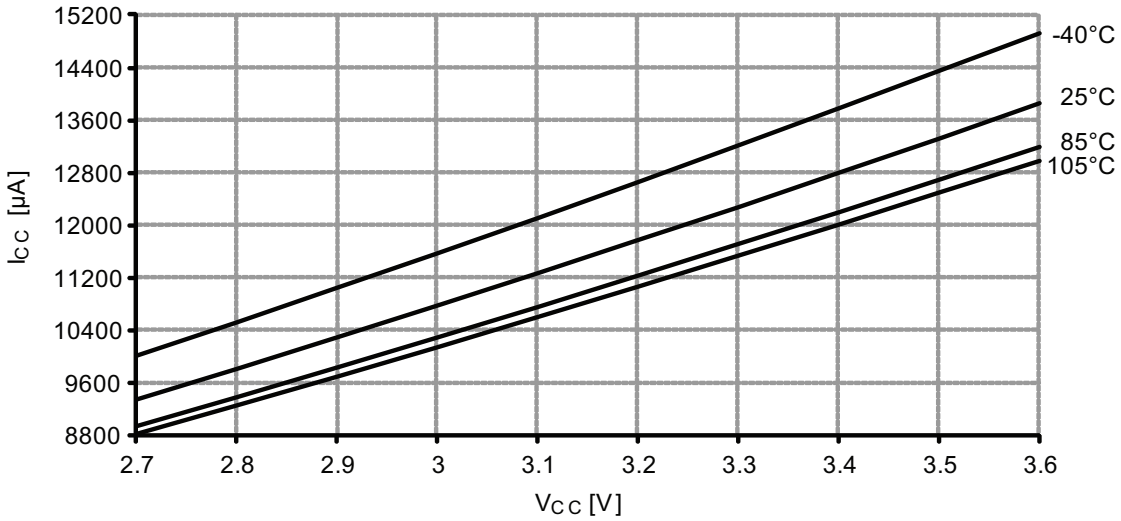


Figure 37-256. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.2 Idle mode supply current

Figure 37-257. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

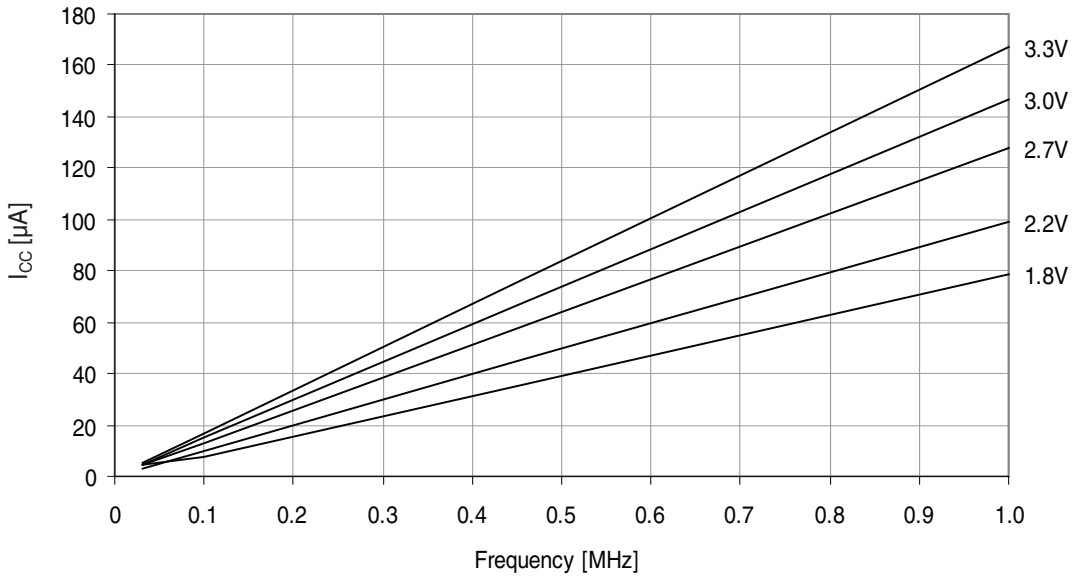


Figure 37-276. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

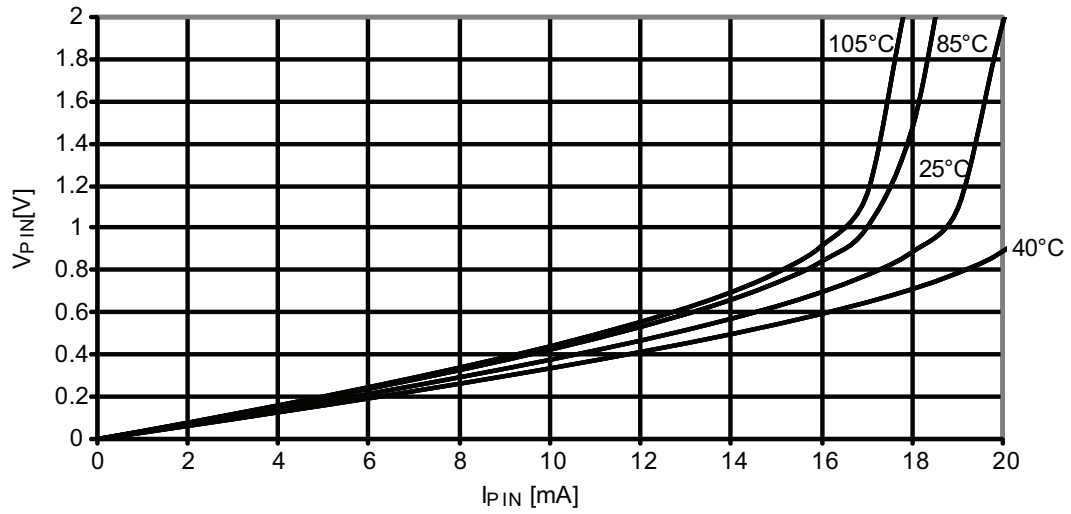
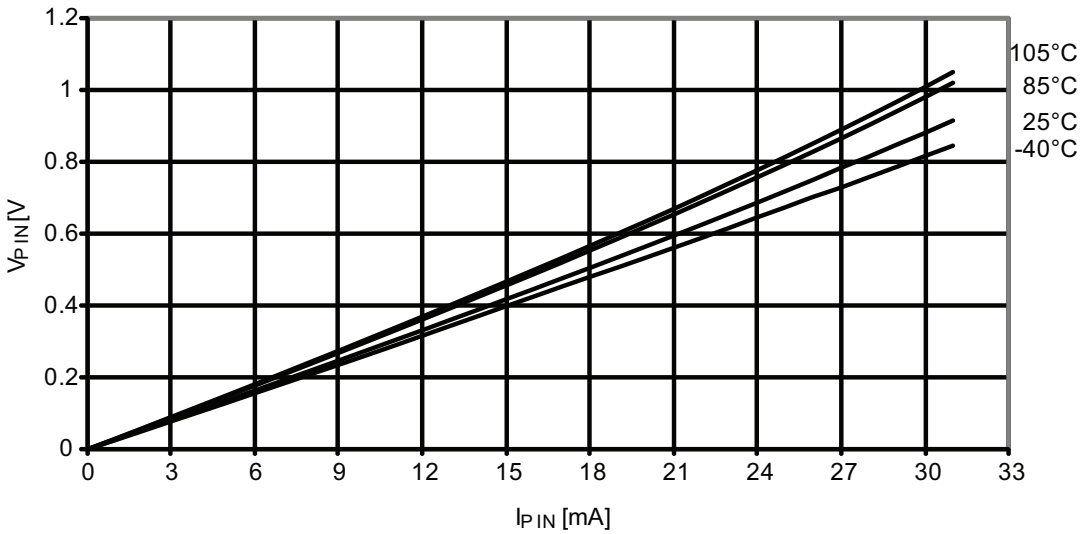


Figure 37-277. I/O pin output voltage vs. sink current.

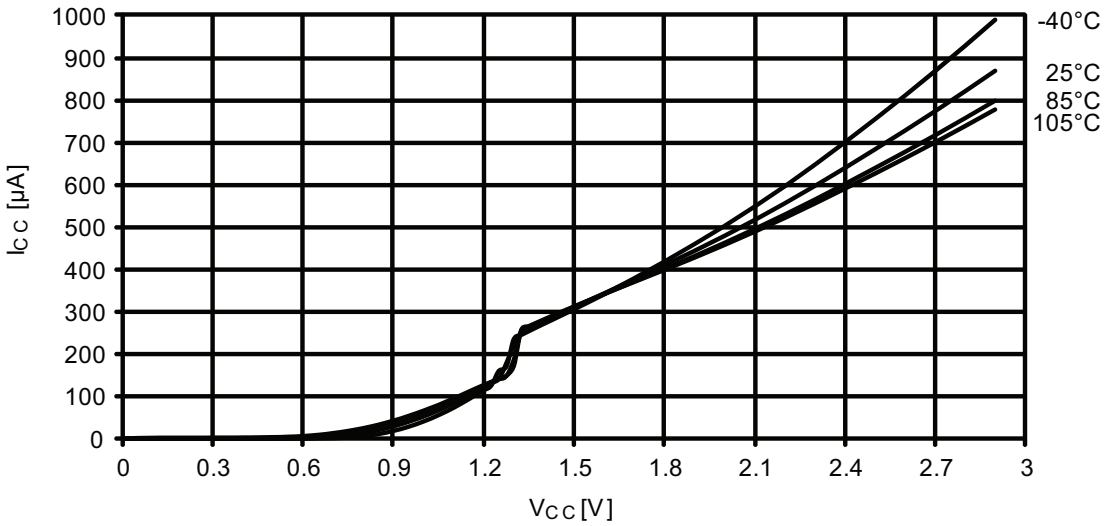
V_{CC} = 3.0V.



37.4.9 Power-on Reset Characteristics

Figure 37-316. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.



37.4.10.4 32MHz Internal Oscillator

Figure 37-323. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

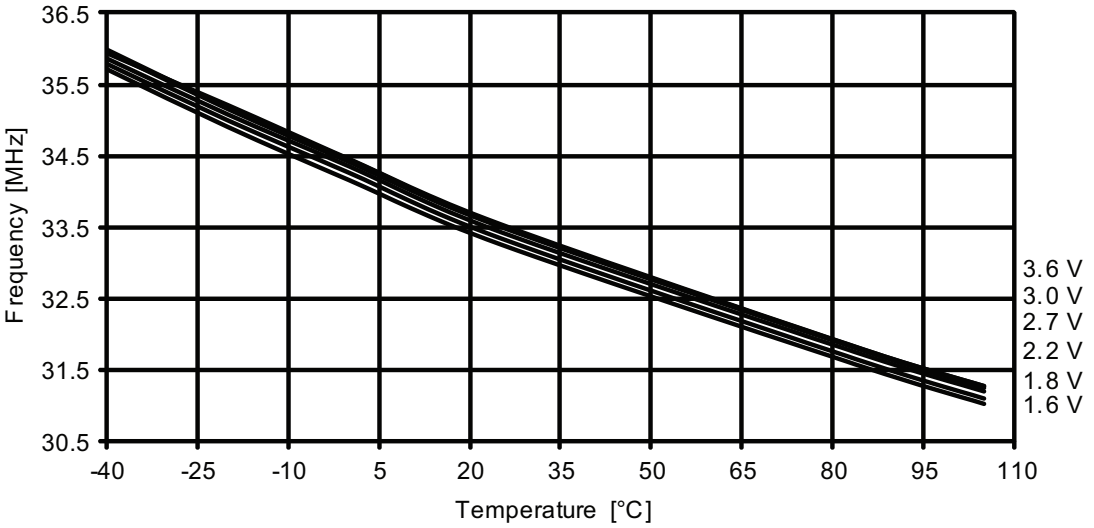


Figure 37-324. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.