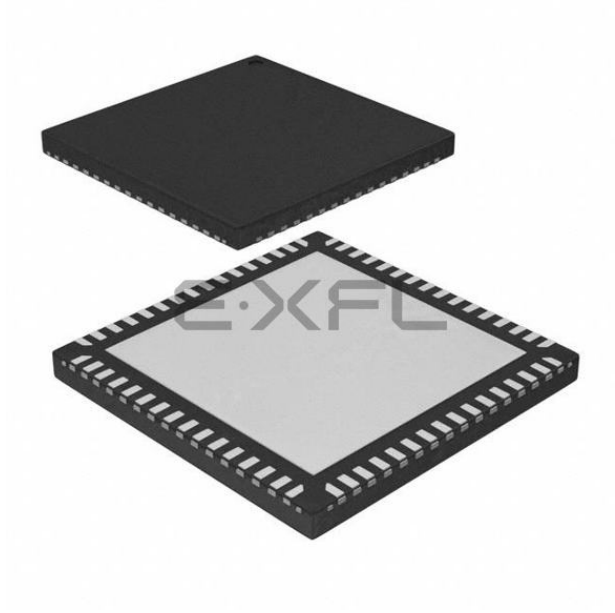

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3u-m7r

6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The stack pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded after reset, and the initial value is the highest address of the internal SRAM. If the SP is changed, it must be set to point above address 0x2000, and it must be defined before any subroutine calls are executed or before interrupts are enabled.

During interrupts or subroutine calls, the return address is automatically pushed on the stack. The return address can be two or three bytes, depending on program memory size of the device. For devices with 128KB or less of program memory, the return address is two bytes, and hence the stack pointer is decremented/incremented by two. For devices with more than 128KB of program memory, the return address is three bytes, and hence the SP is decremented/incremented by three. The return address is popped off the stack when returning from interrupts using the RETI instruction, and from subroutine calls using the RET instruction.

The SP is decremented by one when data are pushed on the stack with the PUSH instruction, and incremented by one when data is popped off the stack using the POP instruction.

To prevent corruption when updating the stack pointer from software, a write to SPL will automatically disable interrupts for up to four instructions or until the next I/O memory write.

After reset the stack pointer is initialized to the highest address of the SRAM. See Figure 7-3 on page 16.

6.8 Register File

The register file consists of 32 x 8-bit general purpose working registers with single clock cycle access time. The register file supports the following input/output schemes:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

Table 36-21. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip Erase	64KB Flash, EEPROM (2) and SRAM Erase		55		ms
	Application Erase	Section erase		6		ms
	Flash	Page Erase		4		ms
		Page Write		4		
		Atomic Page Erase and Write		8		
	EEPROM	Page Erase		4		ms
		Page Write		4		
		Atomic Page Erase and Write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

36.1.14 Clock and Oscillator Characteristics

36.1.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-22. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.1.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-23. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.22		%

36.1.15 SPI Characteristics

Figure 36-5. SPI timing requirements in master mode.

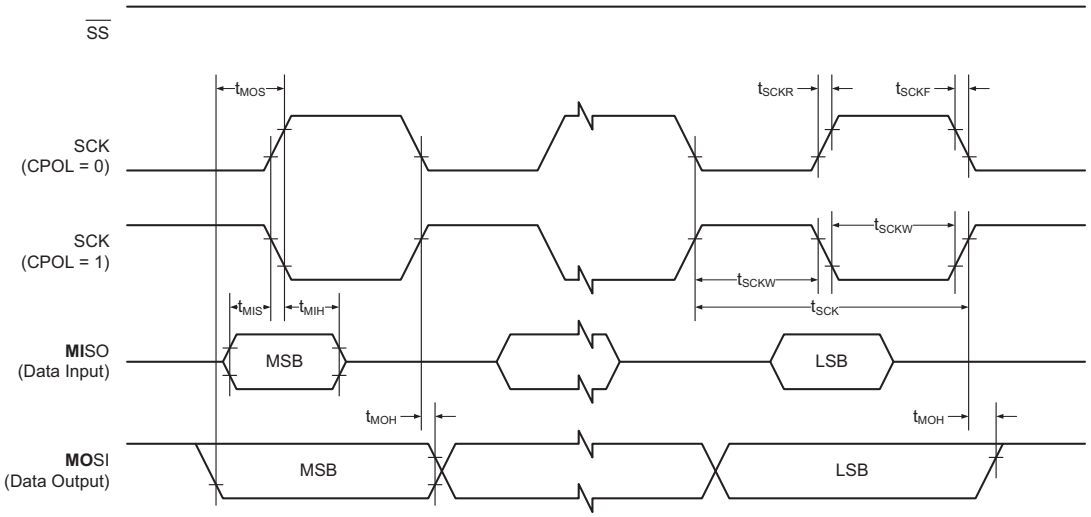
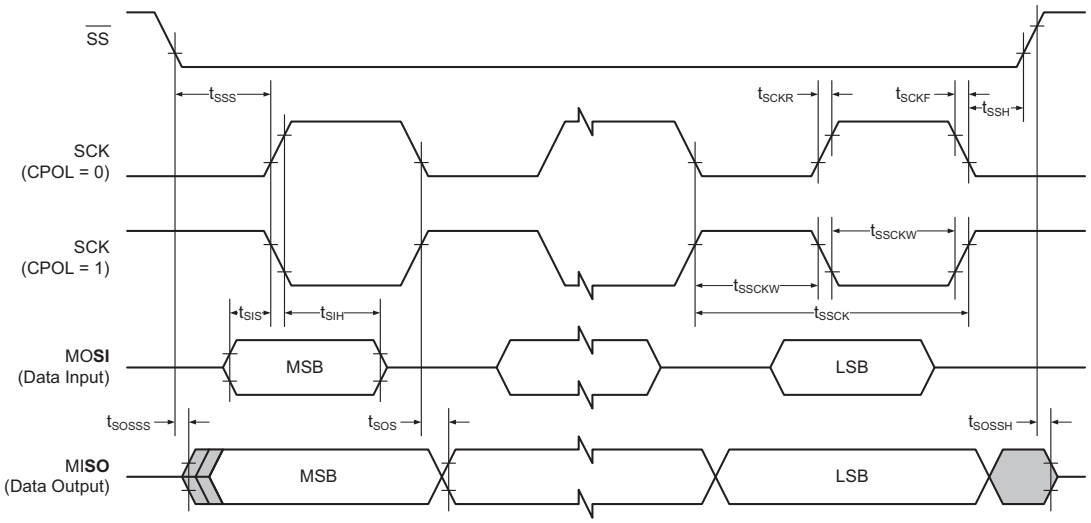
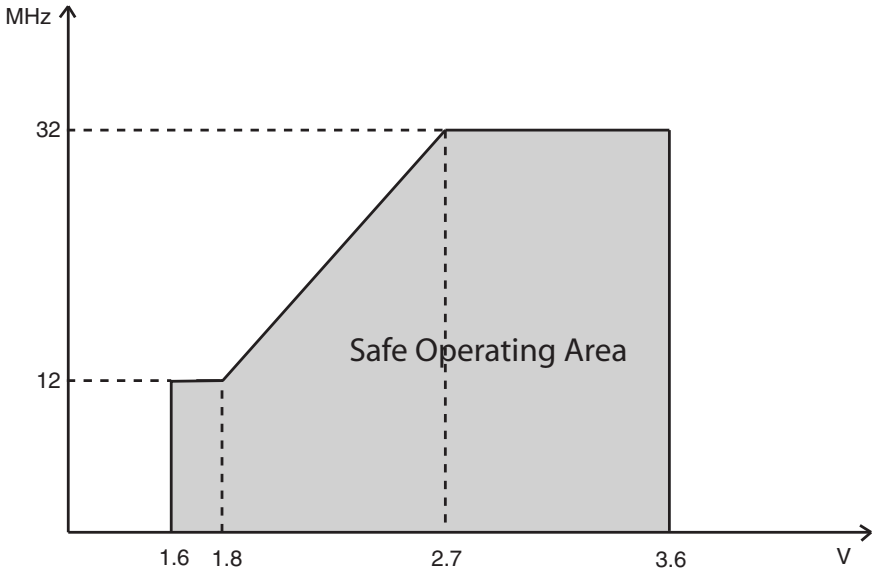


Figure 36-6. SPI timing requirements in slave mode.



The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 36-22. Maximum Frequency vs. V_{CC}.

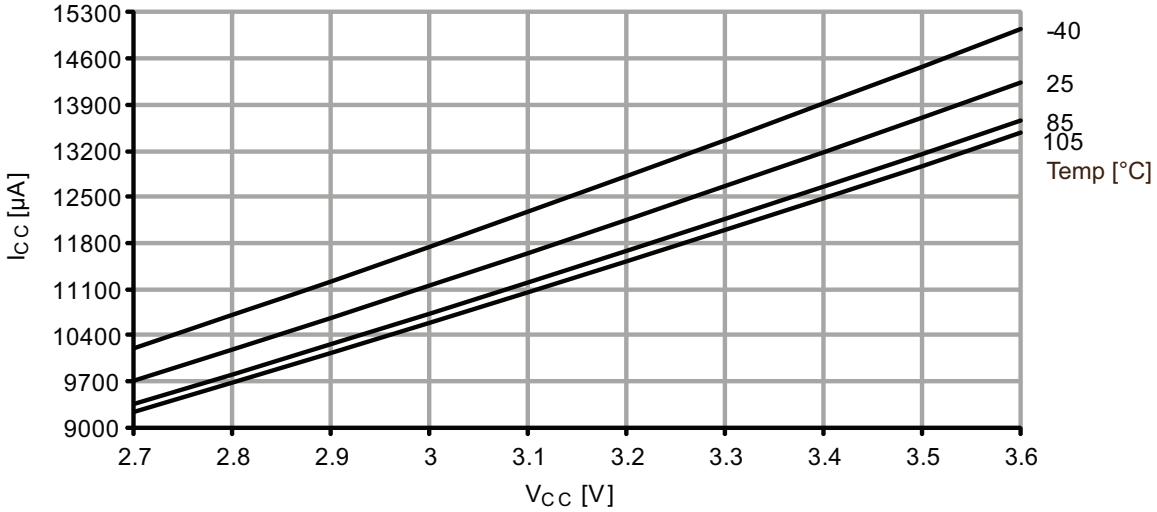


Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Figure 37-90. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.2.1.2 Idle mode supply current

Figure 37-91. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

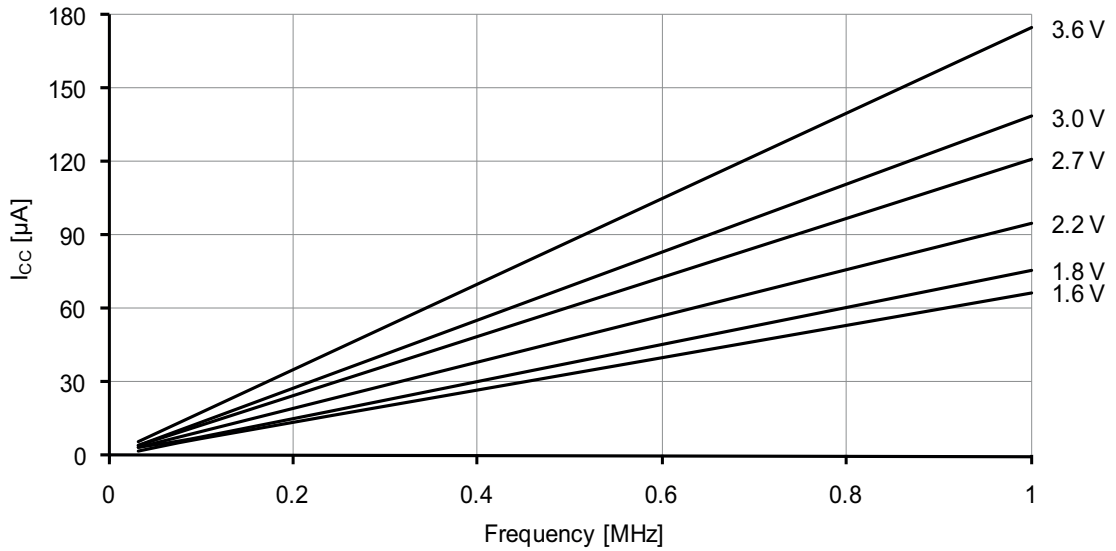


Figure 37-104. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

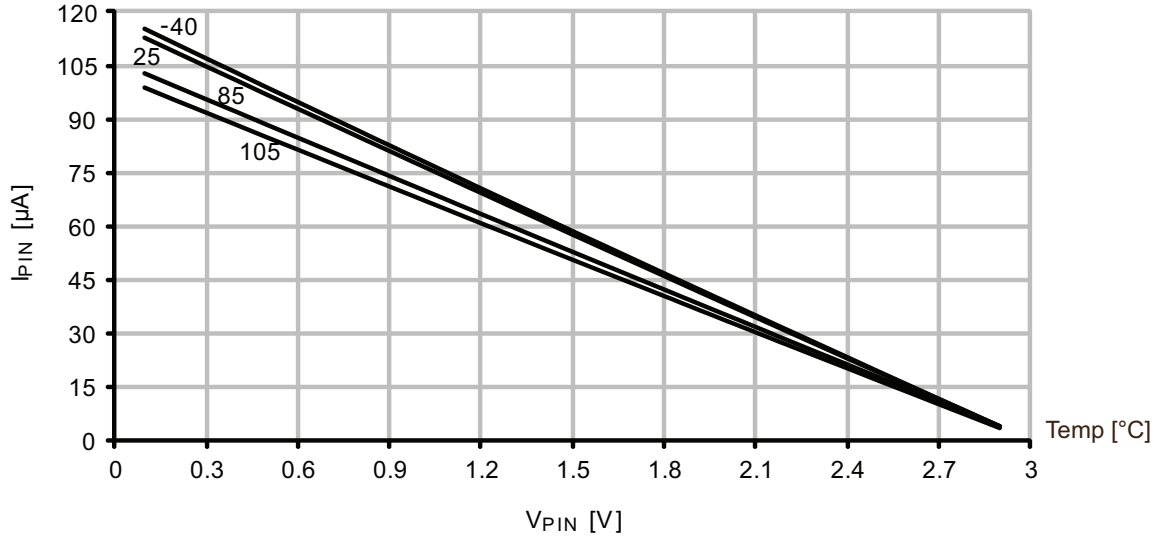


Figure 37-105. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.

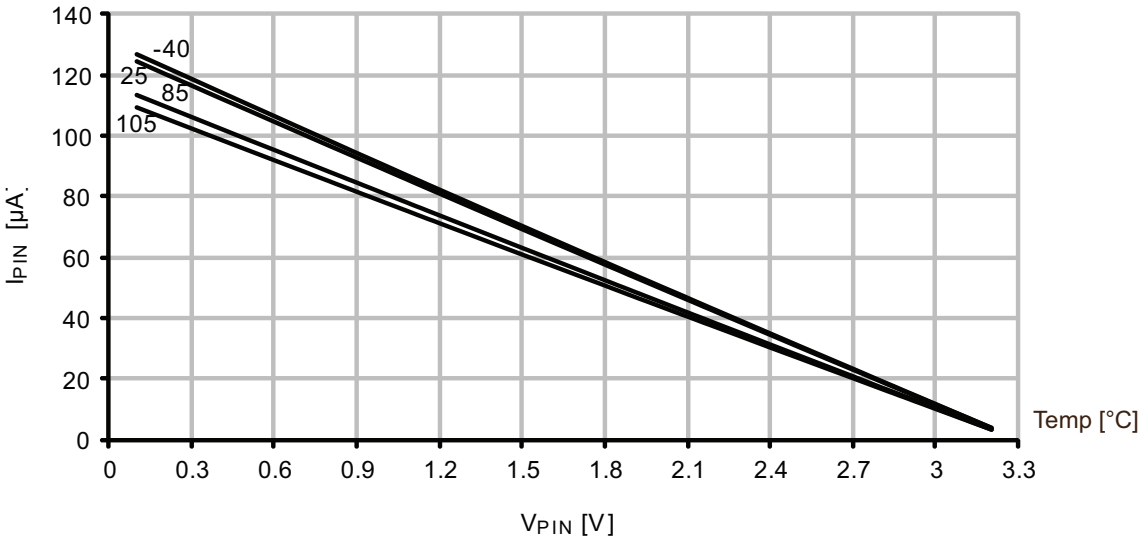


Figure 37-116. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

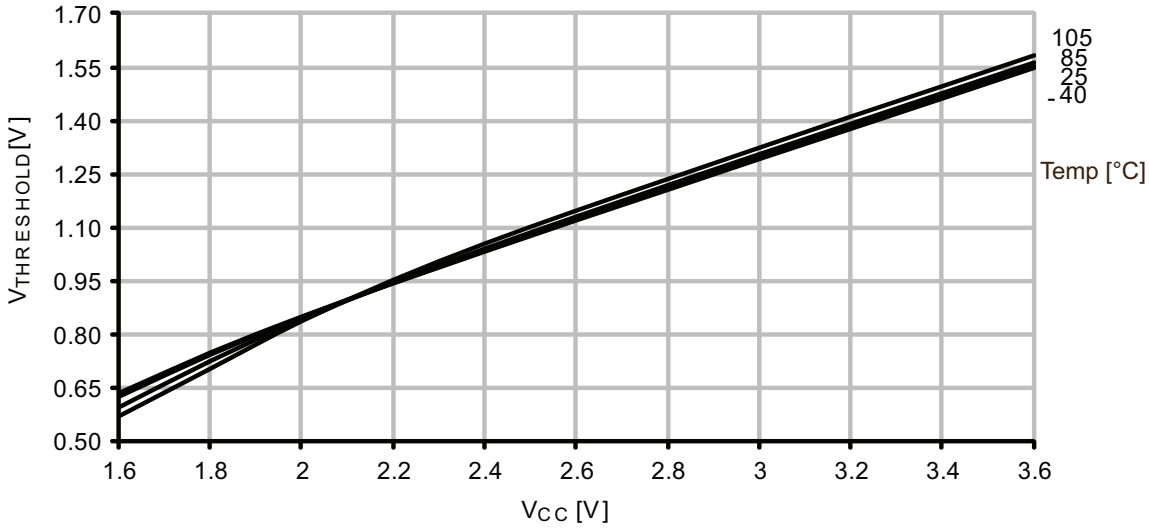
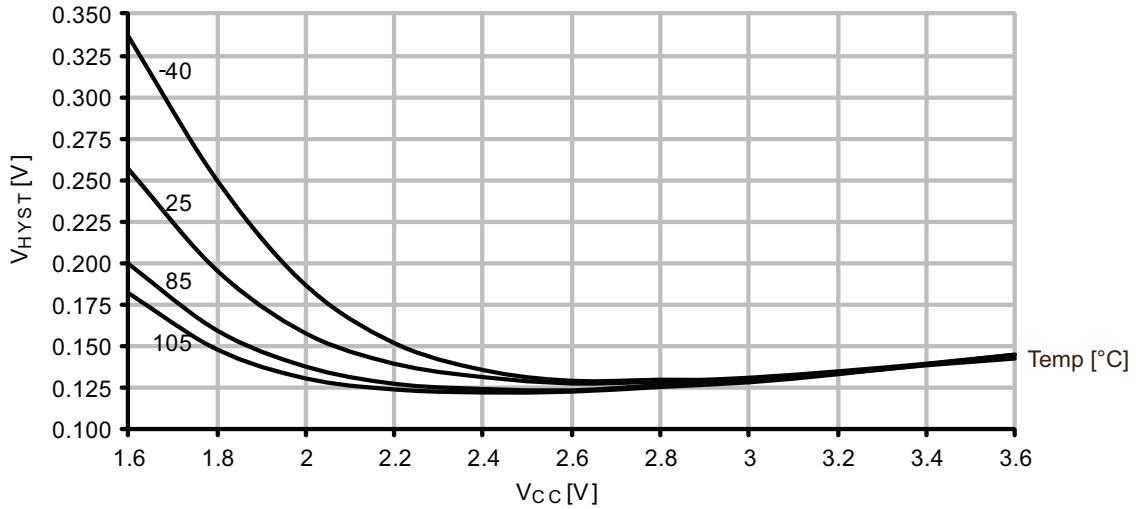


Figure 37-117. I/O pin input hysteresis vs. V_{CC}.



37.3 ATxmega192A3U

37.3.1 Current consumption

37.3.1.1 Active mode supply current

Figure 37-167. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

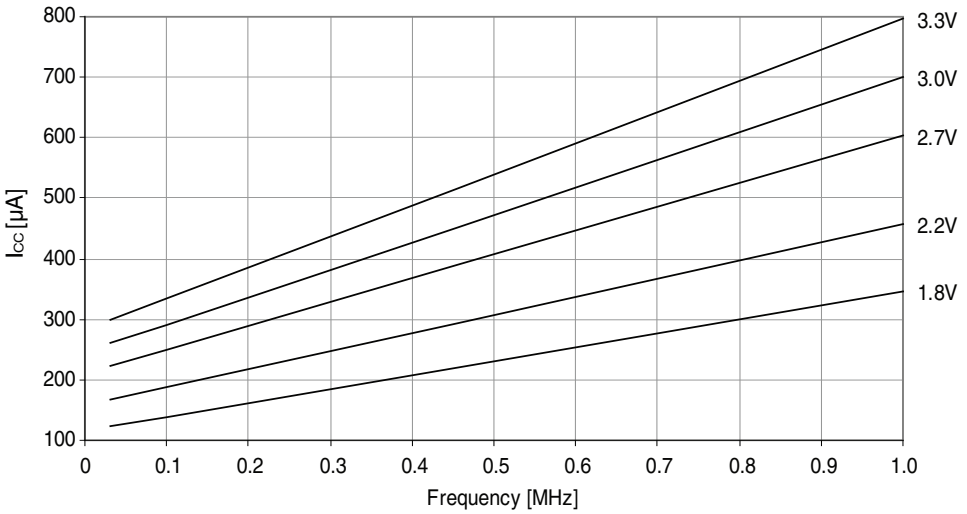


Figure 37-168. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

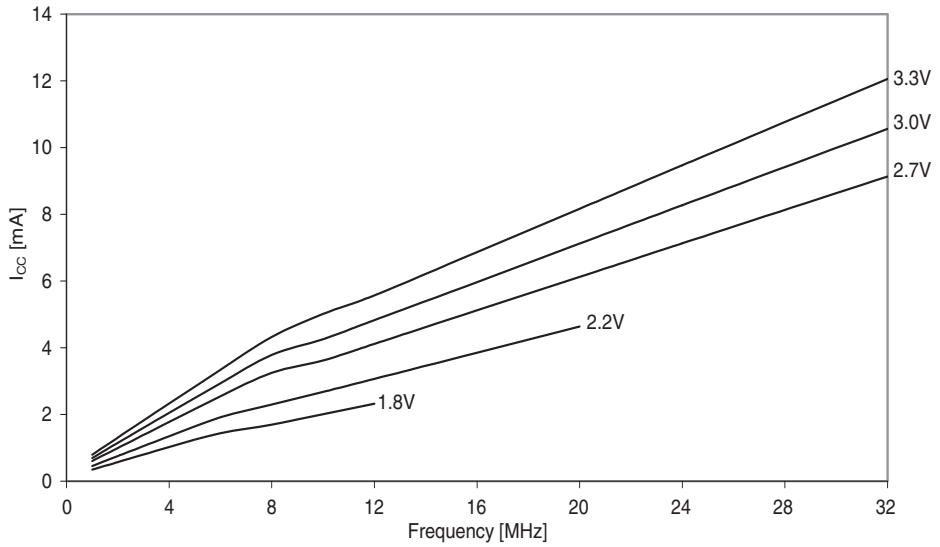


Figure 37-177. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

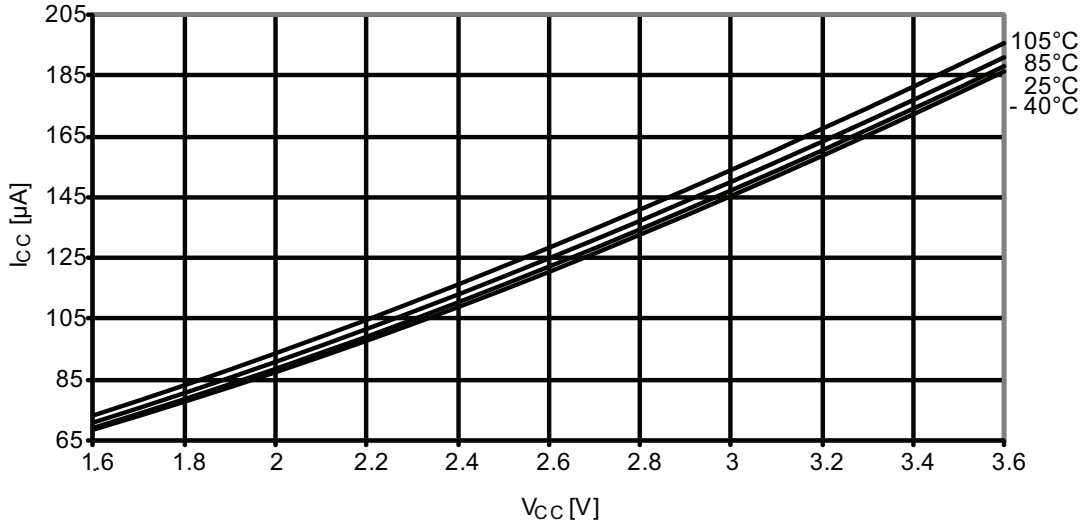


Figure 37-178. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

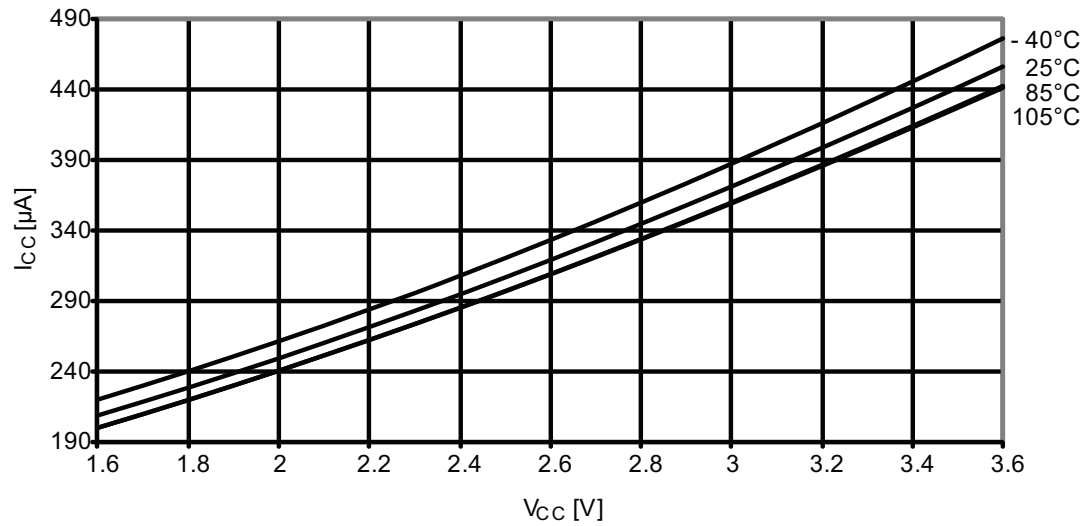


Figure 37-199. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

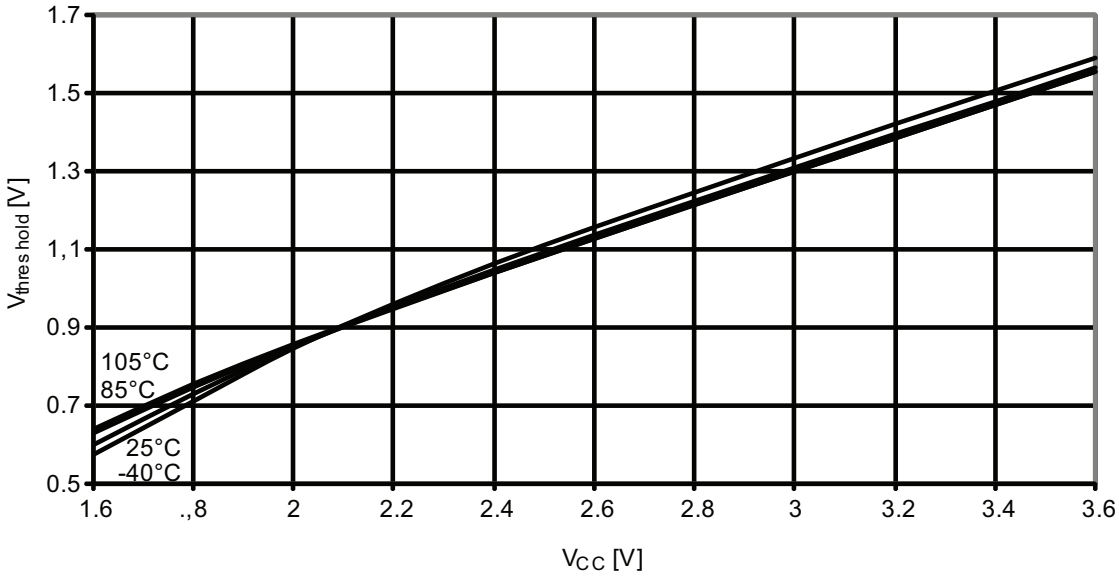


Figure 37-200. I/O pin input hysteresis vs. V_{CC} .

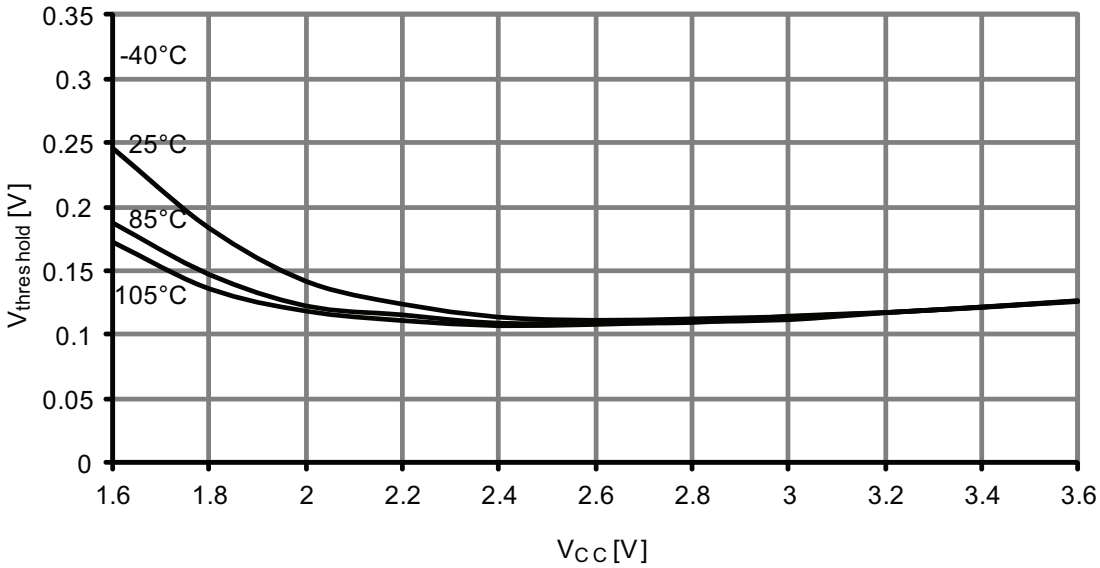


Figure 37-229. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

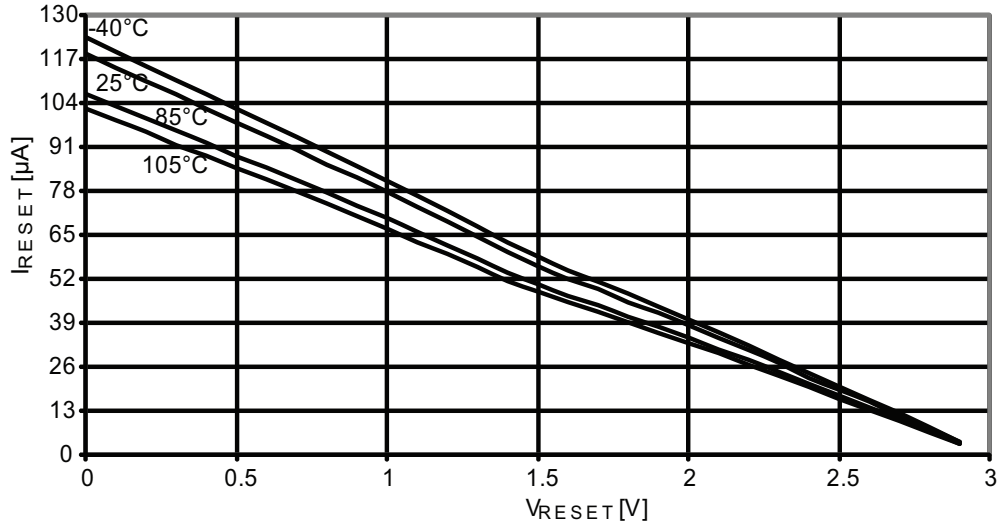


Figure 37-230. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

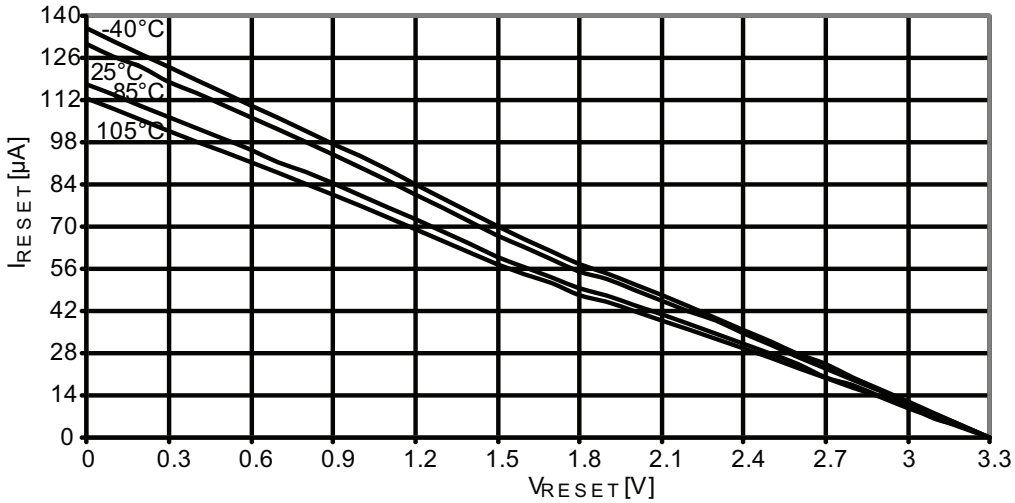


Figure 37-252. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

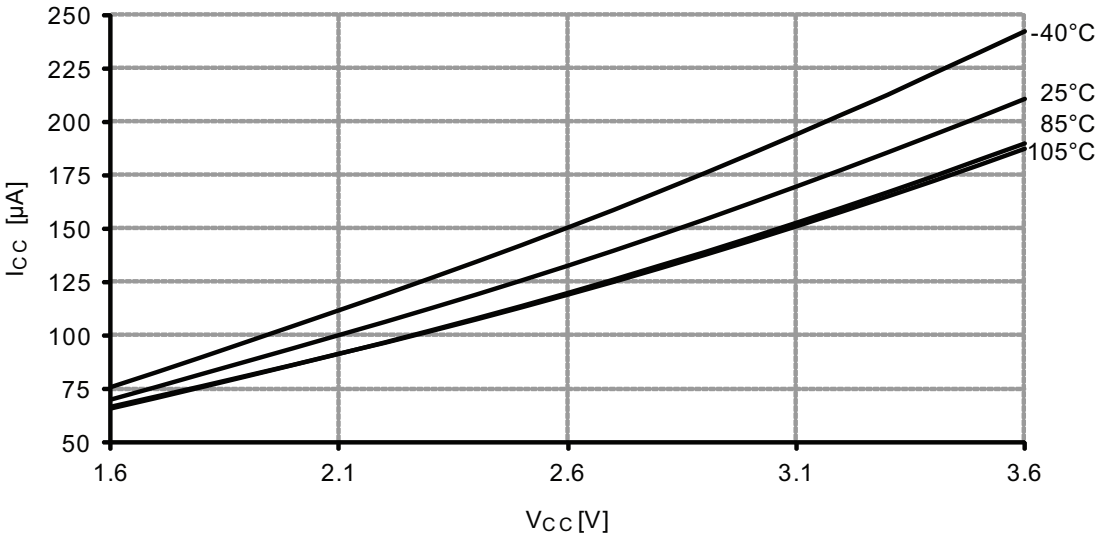


Figure 37-253. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

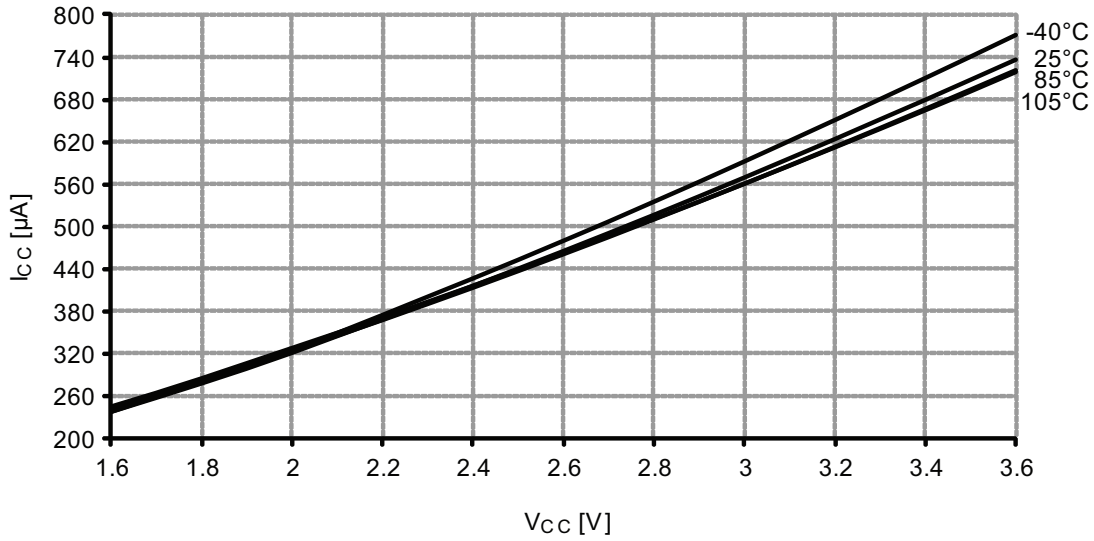


Figure 37-286. INL error vs. input code.

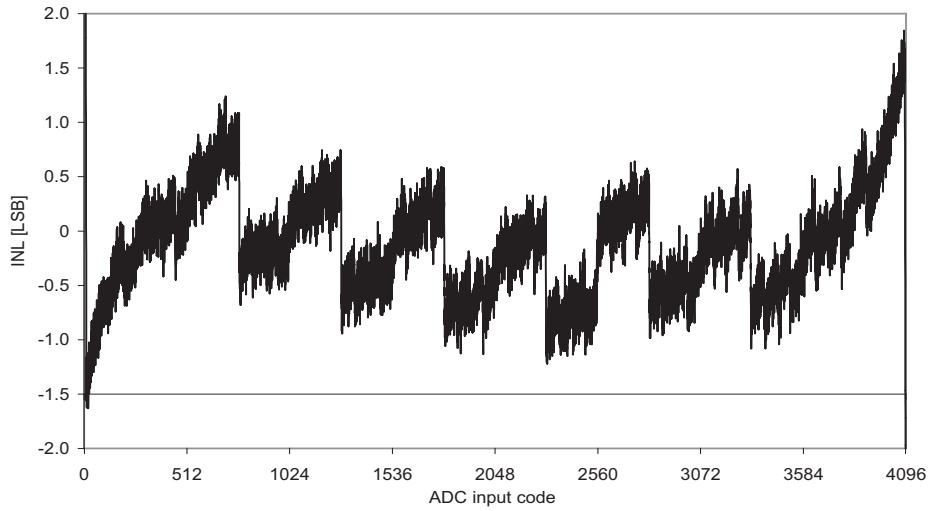


Figure 37-287. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

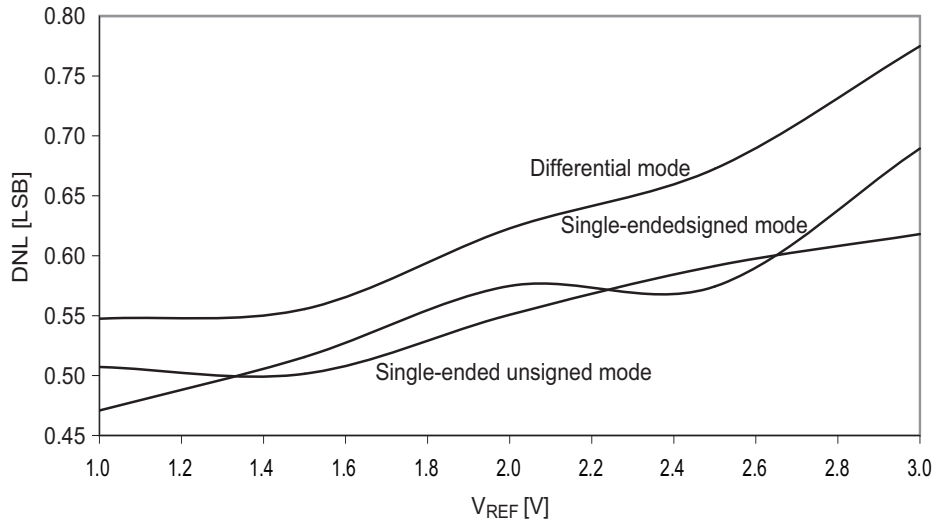


Figure 37-288. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

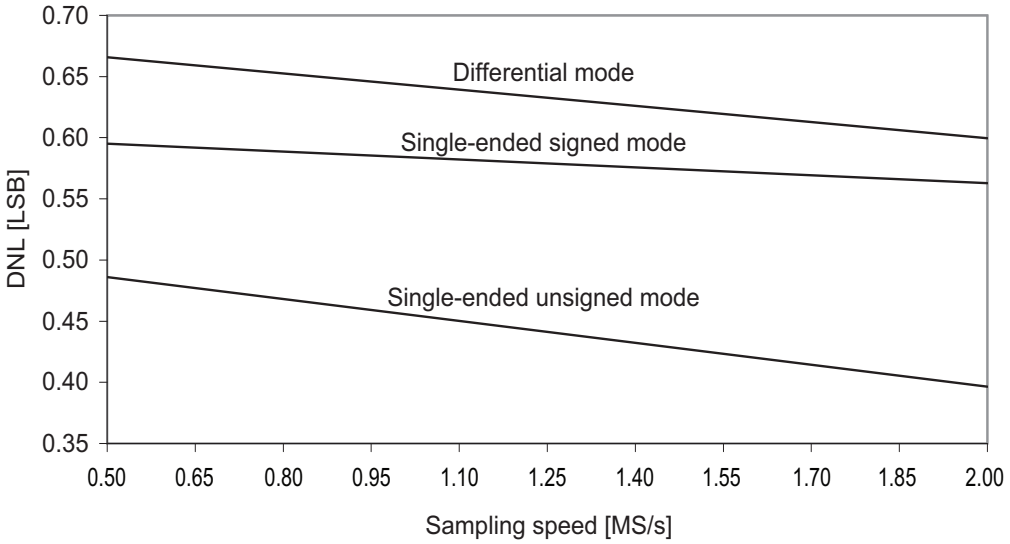


Figure 37-289. DNL error vs. input code.

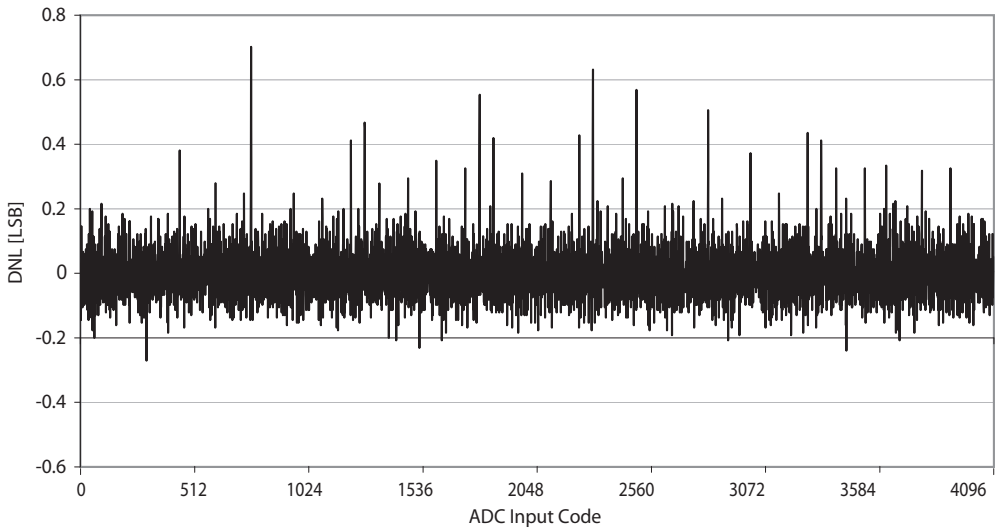


Figure 37-304. Analog comparator current source vs. calibration value.

Temperature = 25°C.

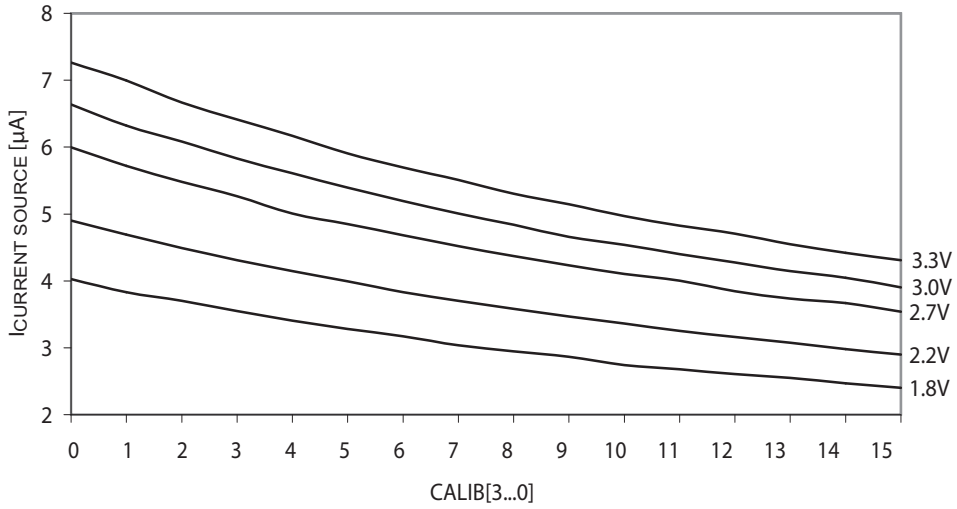
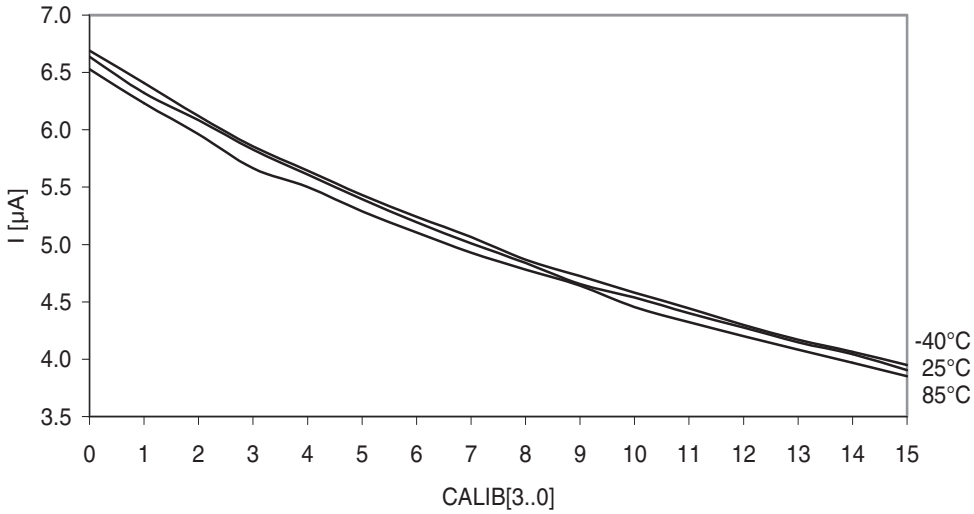


Figure 37-305. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.



37.4.7 BOD Characteristics

Figure 37-308. BOD thresholds vs. temperature.

BOD level = 1.6V.

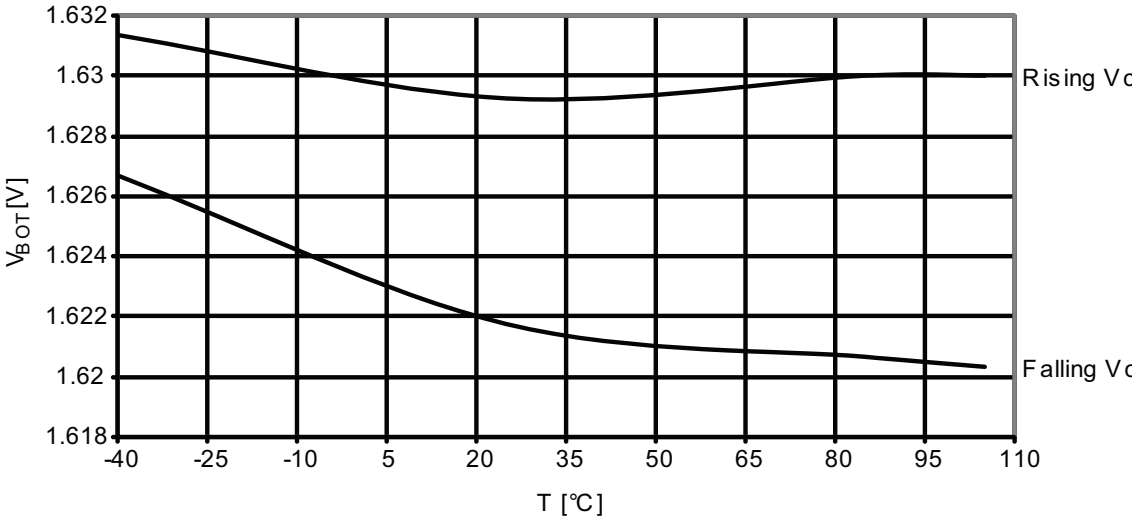
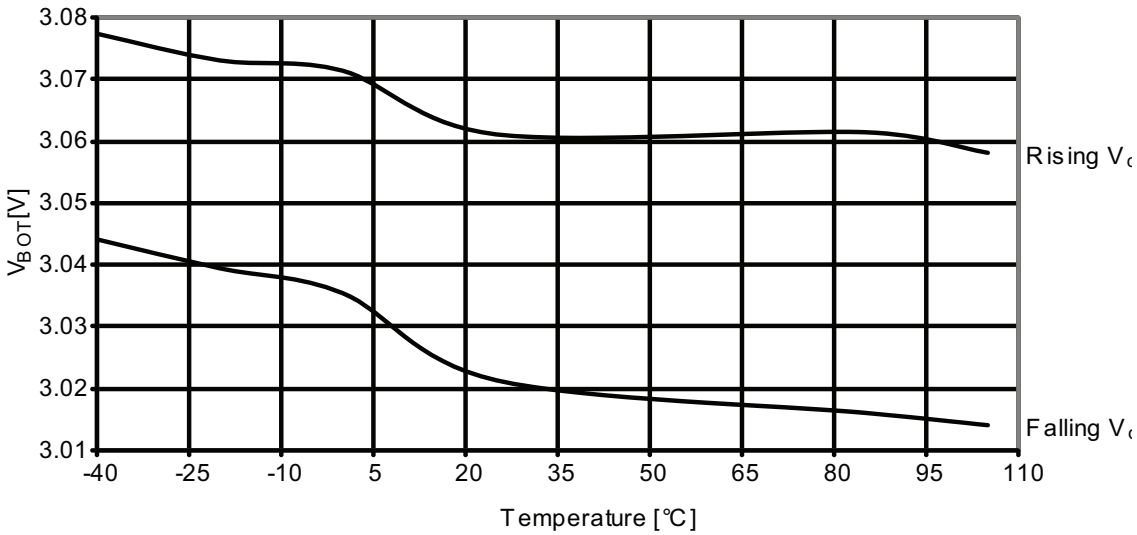


Figure 37-309. BOD thresholds vs. temperature.

BOD level = 3.0V.



37.4.10.4 32MHz Internal Oscillator

Figure 37-323. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

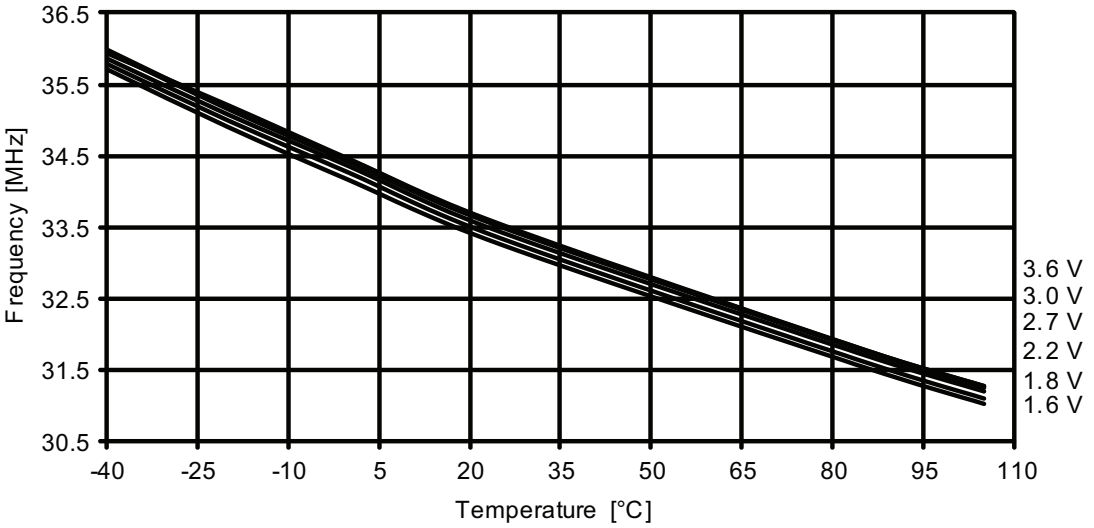


Figure 37-324. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

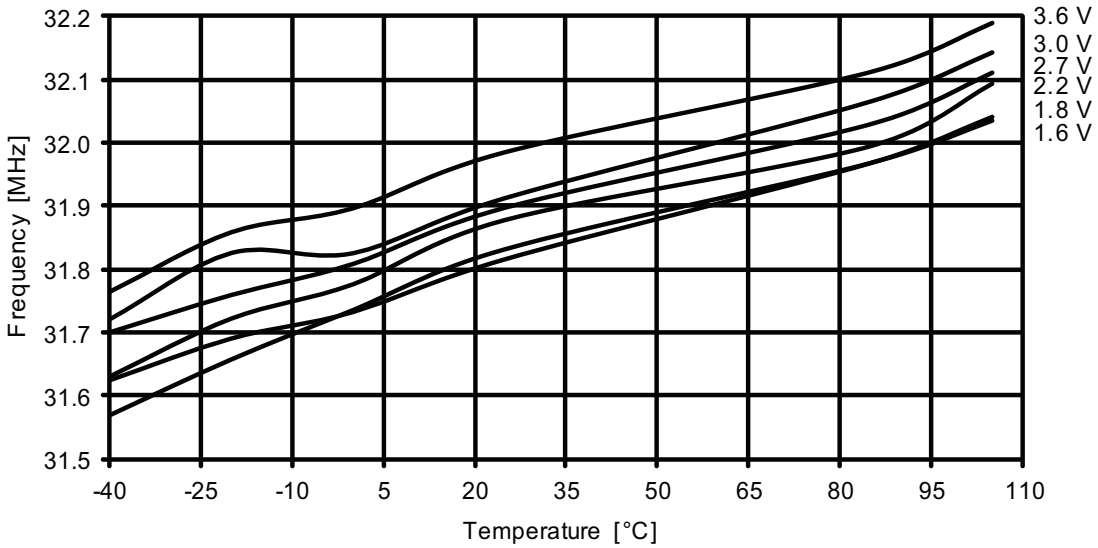


Figure 37-325. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

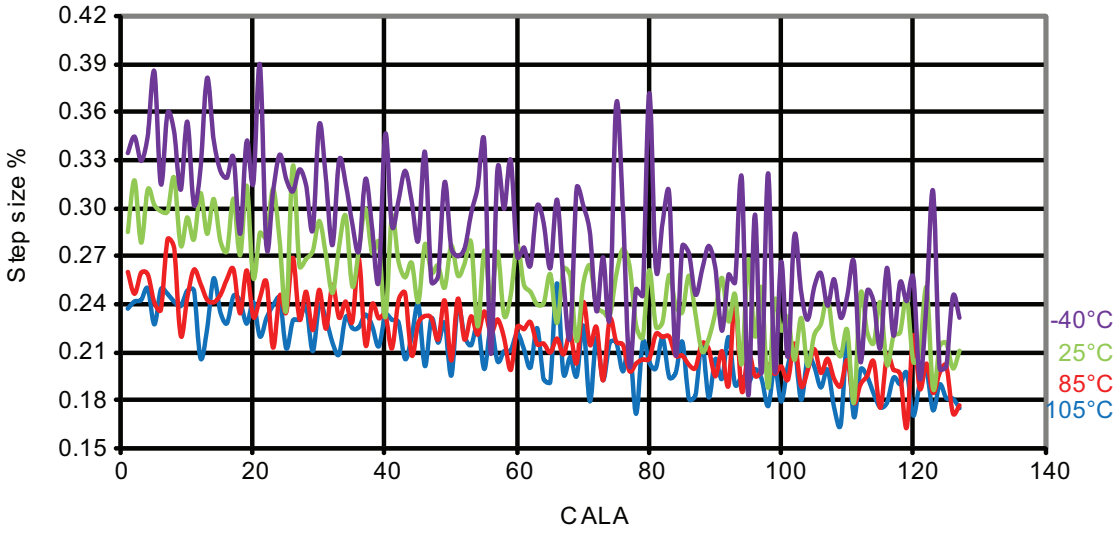


Figure 37-326. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.