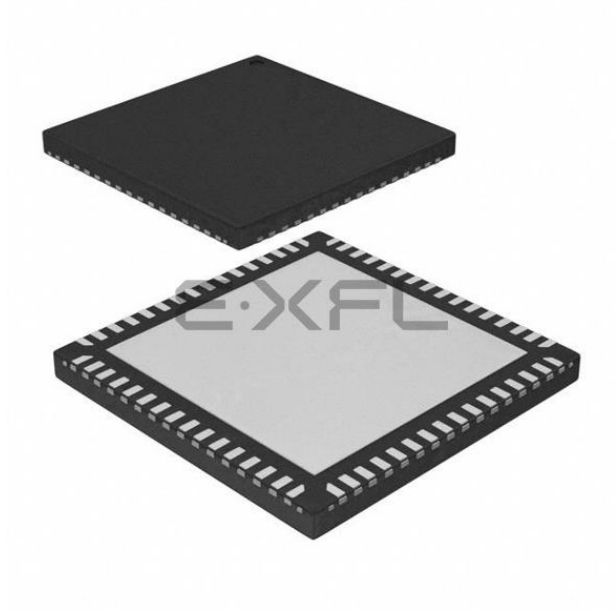

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3u-mh

27. CRC – Cyclic Redundancy Check Generator

27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, DMA controller and CPU
  - Continuous CRC on data going through a DMA channel
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

Polynomial:	$x^{16}+x^{12}+x^5+1$
Hex value:	0x1021

- **CRC-32:**

Polynomial:	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Hex value:	0x04C11DB7

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 (1)
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 (1)
CALL	k	call Subroutine	PC ← k	None	3 / 4 (1)
RET		Subroutine Return	PC ← STACK	None	4 / 5 (1)
RETI		Interrupt Return	PC ← STACK	I	4 / 5 (1)
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

36.1.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 36-7. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} [1]/ I_{OL} [2]	I/O pin source/sink current			-20		20	mA
V_{IH}	High Level Input Voltage	V_{CC} = 2.7 - 3.6V		2		V_{CC}+0.3	V
		V_{CC} = 2.0 - 2.7V		0.7*V_{CC}		V_{CC}+0.3	
		V_{CC} = 1.6 - 2.0V		0.8*V_{CC}		V_{CC}+0.3	
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7- 3.6V		-0.3		0.8	V
		V_{CC} = 2.0 - 2.7V		-0.3		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.0V		-0.3		0.2*V_{CC}	
V_{OH}	High Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OH} = -2mA	2.4	0.94*V_{CC}		V
		V_{CC} = 2.3 - 2.7V	I_{OH} = -1mA	2.0	0.96*V_{CC}		
			I_{OH} = -2mA	1.7	0.92*V_{CC}		
		V_{CC} = 3.3V	I_{OH} = -8mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -6mA	2.1	2.6		
		V_{CC} = 1.8V	I_{OH} = -2mA	1.4	1.6		
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0 - 3.6V	I_{OL} = 2mA		0.05*V_{CC}	0.4	V
		V_{CC} = 2.3 - 2.7V	I_{OL} = 1mA		0.03*V_{CC}	0.4	
			I_{OL} = 2mA		0.06*V_{CC}	0.7	
		V_{CC} = 3.3V	I_{OL} = 15mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 10mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 5mA		0.3	0.46	
I_{IN}	Input Leakage Current	T = 25°C			<0.01	0.1	µA
R_P	Pull/Buss keeper Resistor				27		kΩ
t_r	Rise time	No load			4		ns
			slew rate limitation		7		

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

36.2 ATxmega128A3U

36.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-33. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-34. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		1.60		3.6	V
AV_{CC}	Analog Supply Voltage		1.60		3.6	V
T_A	Temperature range	85 °C	-40		85	°C
		105 °C	-40		105	
T_j	Junction temperature	85°C	-40		105	°C
		105°C	-40		125	

Table 36-35. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

36.2.6 ADC characteristics

Table 36-40. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		5.0		kΩ
C_{sample}	Input capacitance	Switched		5.0		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-41. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling Time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	mode = HS	V_{CC} = 3.0V, T= 85°C		90	100	ns
			VCC = 1.6V - 3.6V		95		
		mode = LP			200	500	
	64-Level Voltage Scaler	Integral non-linearity (INL)			0.5	1.0	lsb

36.2.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-48. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.0		%

36.2.10 Brownout Detection Characteristics

Table 36-49. Brownout detection characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.6		%

Table 36-60. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.2.14.7 External 16MHz crystal oscillator and XOSC characteristics

Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

Table 36-78. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL (1)	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4	
			V_{CC} = 3.6V		±1.5	±4	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL (1)	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3	lsb
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4		lsb
	Gain calibration step size				4		lsb
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

36.3.8 Analog Comparator Characteristics

Table 36-79. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input Offset Voltage			<±10		mV
I_{lk}	Input Leakage Current			<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, None			0		mV
V_{hys2}	Hysteresis, Small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, Large	mode = HS		30		mV
		mode = LP		60		

36.4.11 External Reset Characteristics

Table 36-114. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			95	1000	ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V		0.60*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.70*V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V		0.40*V_{CC}		
		V_{CC} = 1.6 - 2.7V		0.30*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

36.4.12 Power-on Reset Characteristics

Table 36-115. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	V

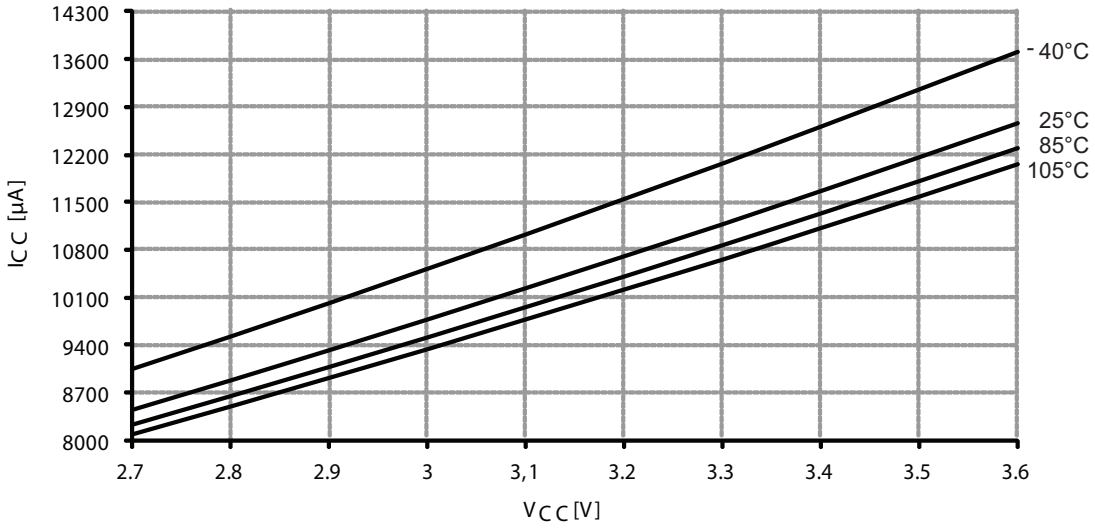
Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

36.4.13 Flash and EEPROM Memory Characteristics

Table 36-116. Endurance and data retention.

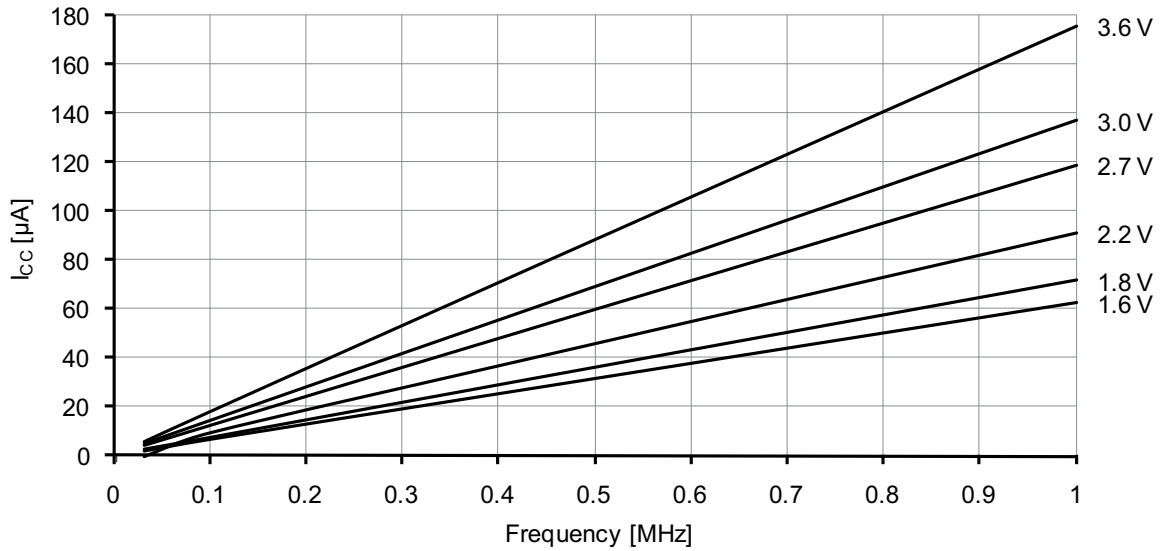
Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Figure 37-7. Active mode supply current vs. V_{CC}.
f_{SYS} = 32MHz internal oscillator.



37.1.1.2 Idle mode supply current

Figure 37-8. Idle mode supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.



37.1.2.2 Output Voltage vs. Sink/Source Current

Figure 37-23. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

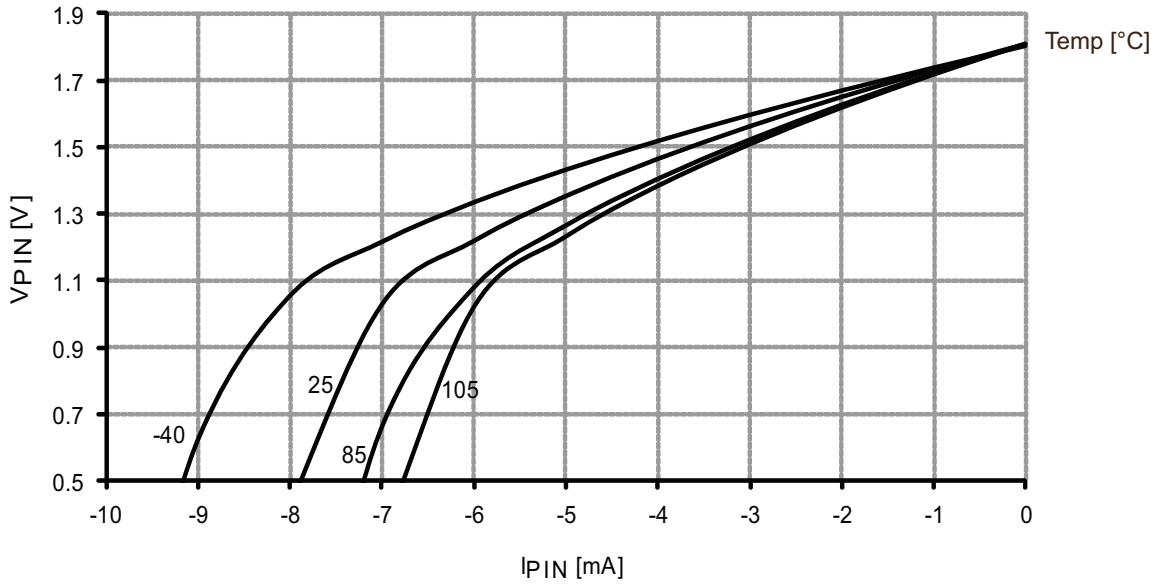
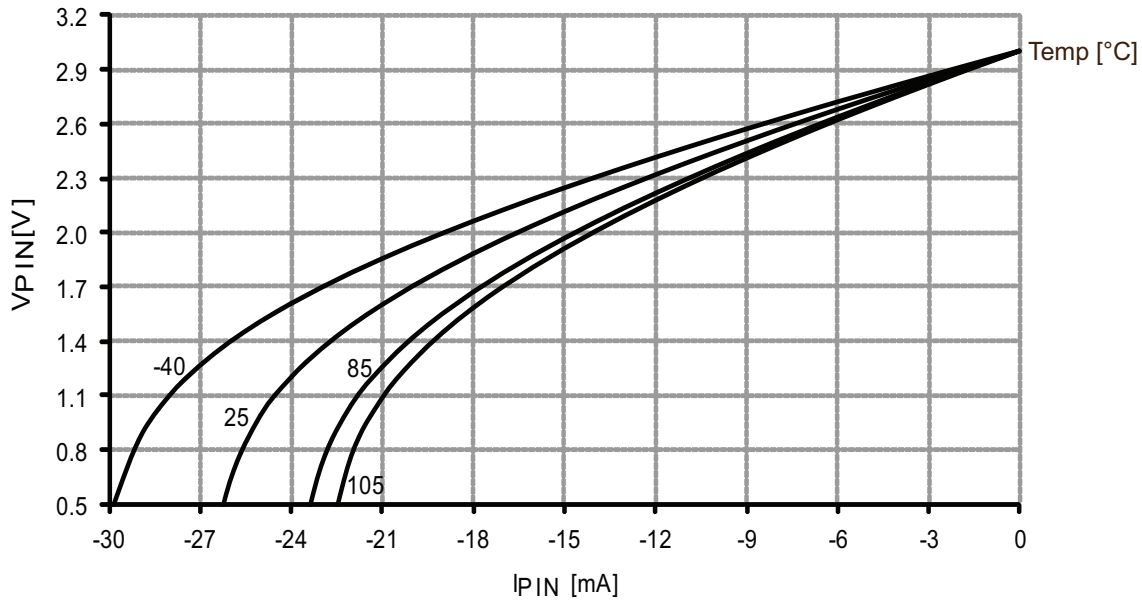


Figure 37-24. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.



37.2 ATxmega128A3U

37.2.1 Current consumption

37.2.1.1 Active mode supply current

Figure 37-84. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

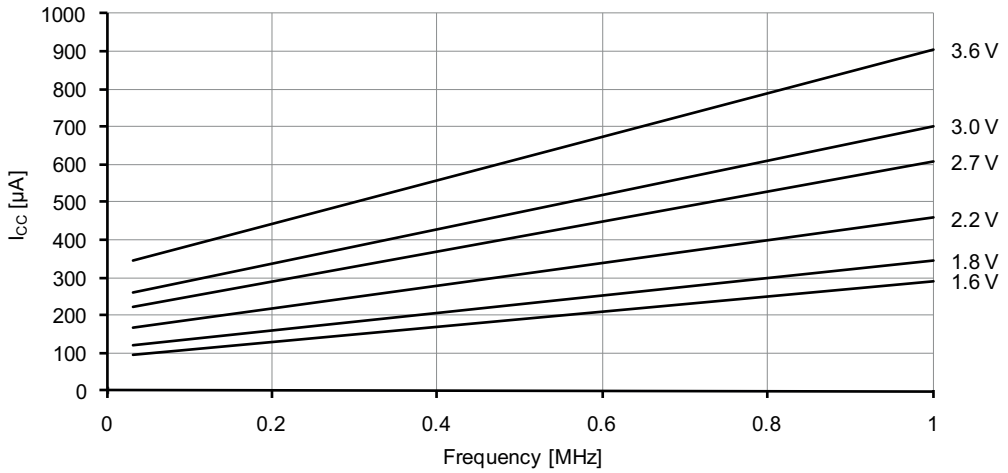


Figure 37-85. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

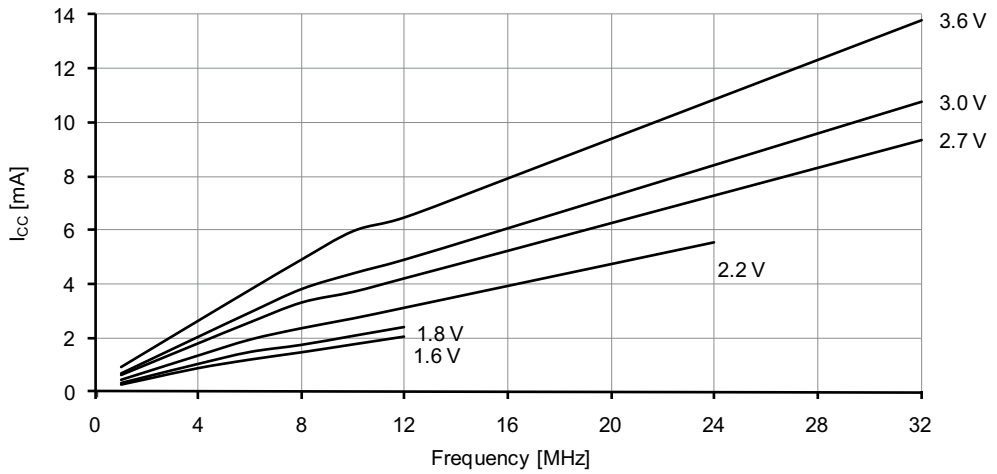


Figure 37-94. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

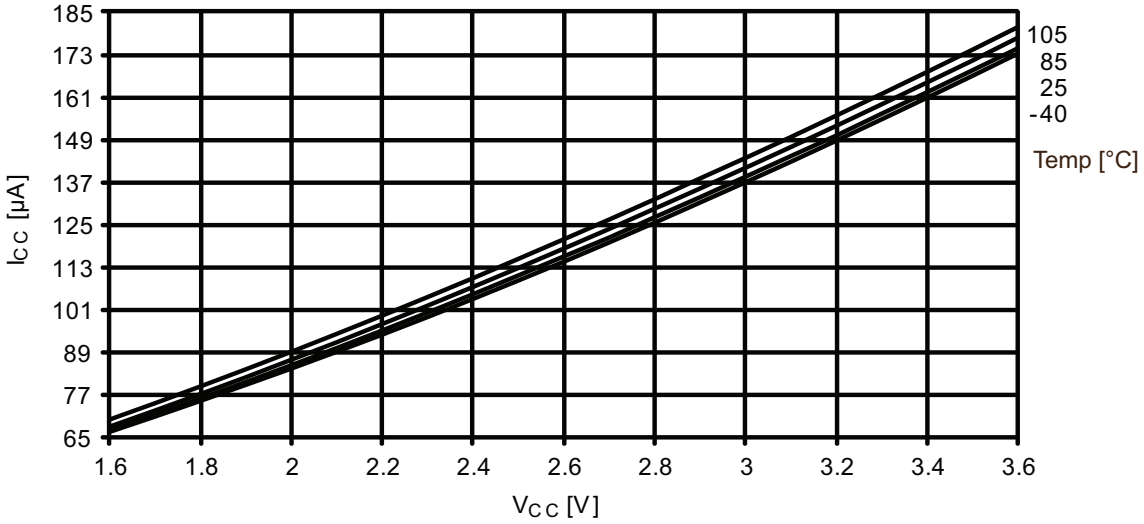


Figure 37-95. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

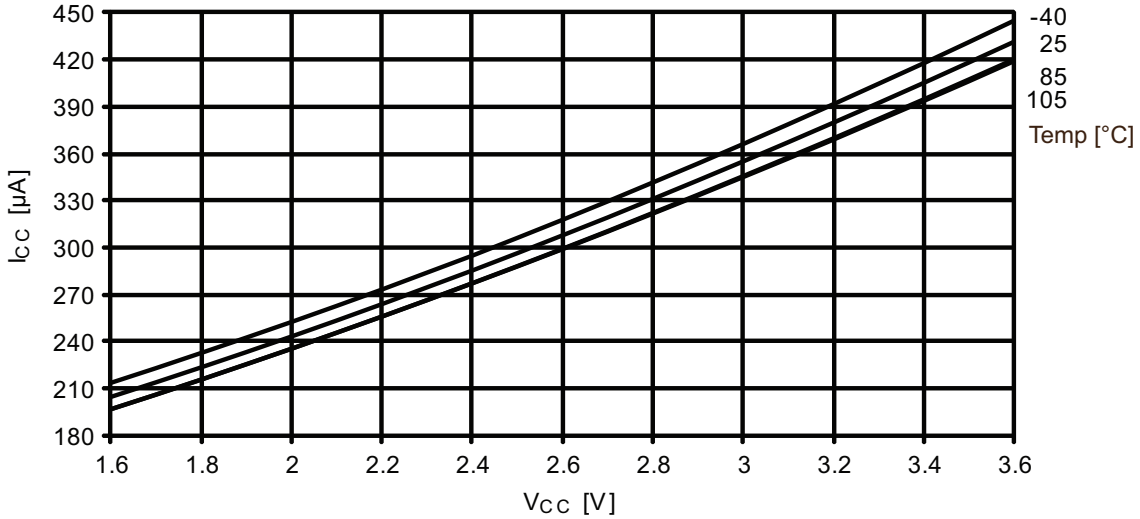


Figure 37-191. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

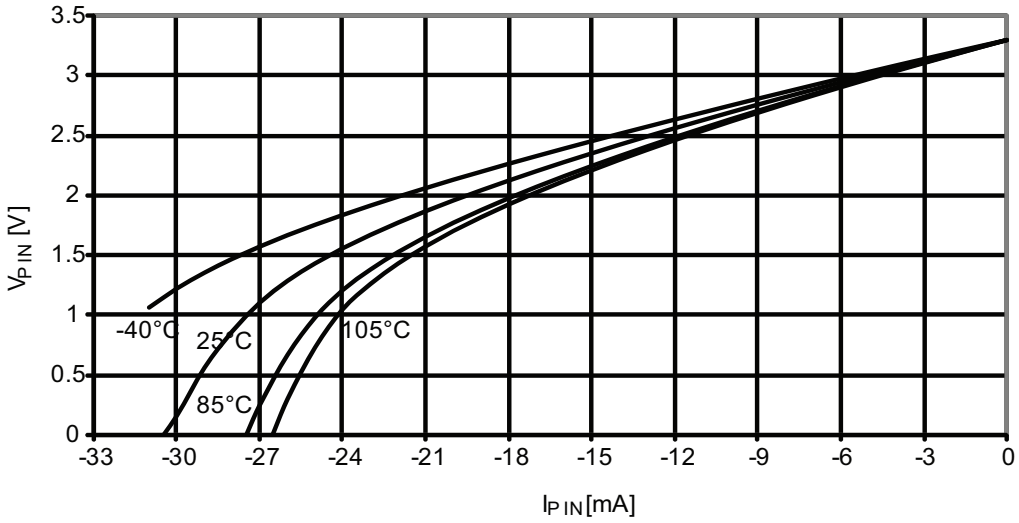


Figure 37-192. I/O pin output voltage vs. source current.

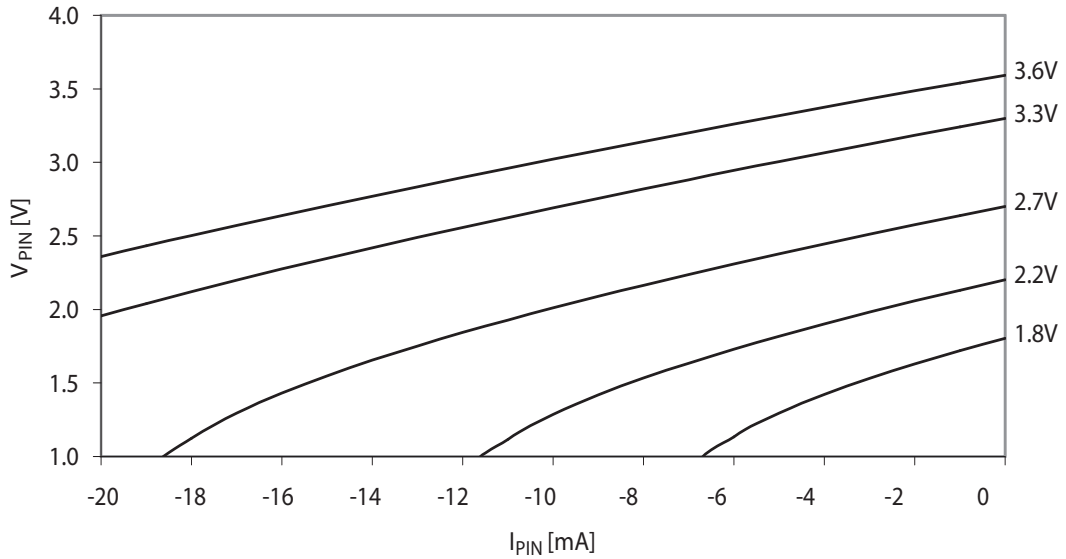


Figure 37-242. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

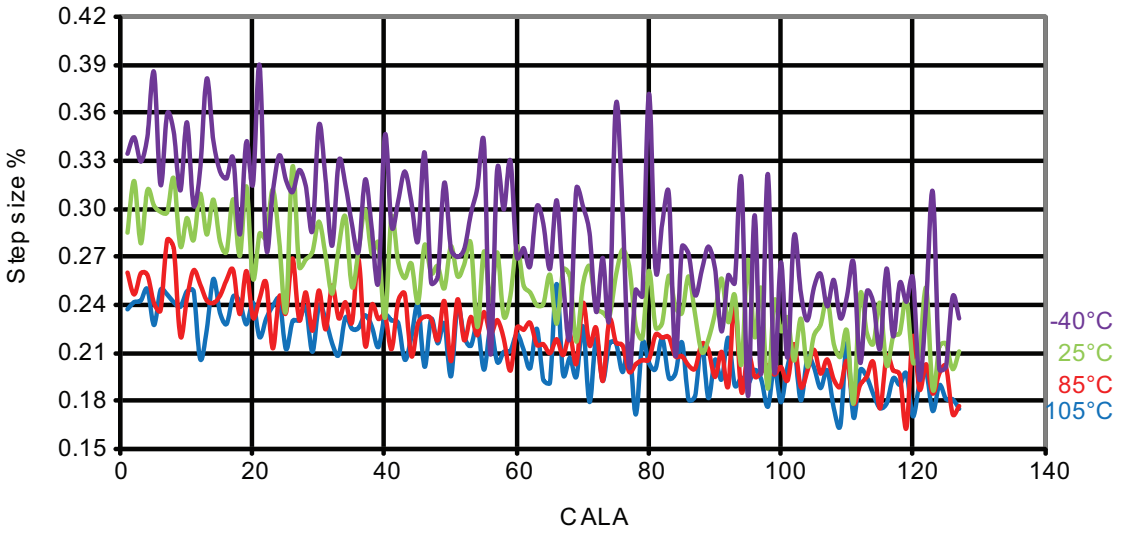


Figure 37-243. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.

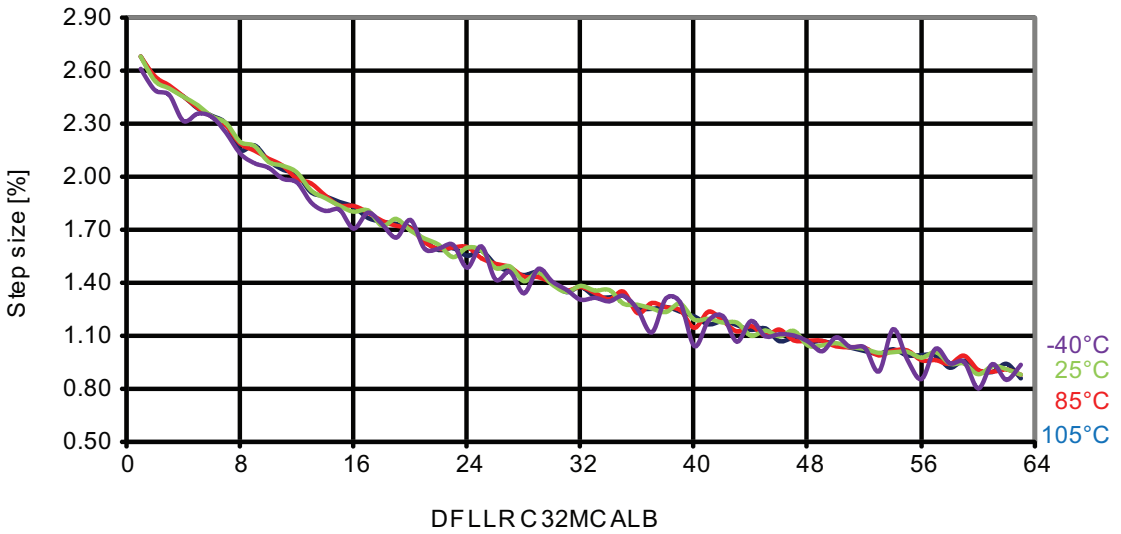


Figure 37-252. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

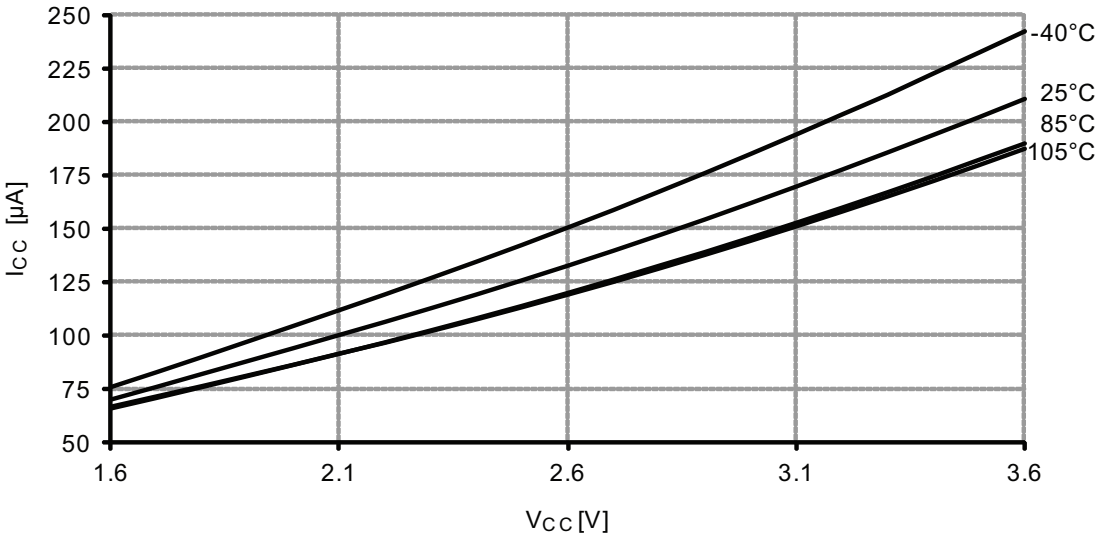


Figure 37-253. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

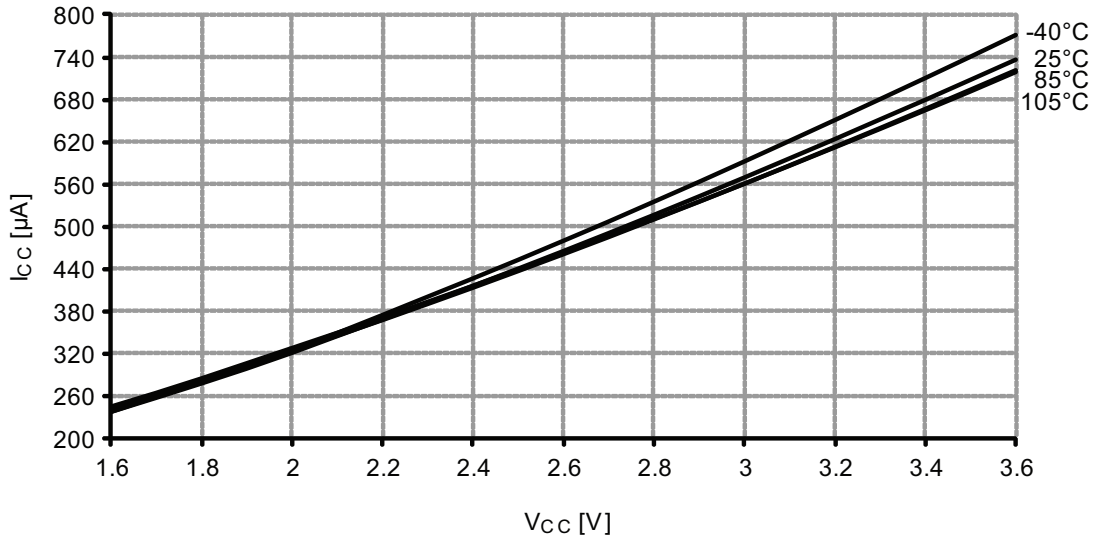


Figure 37-286. INL error vs. input code.

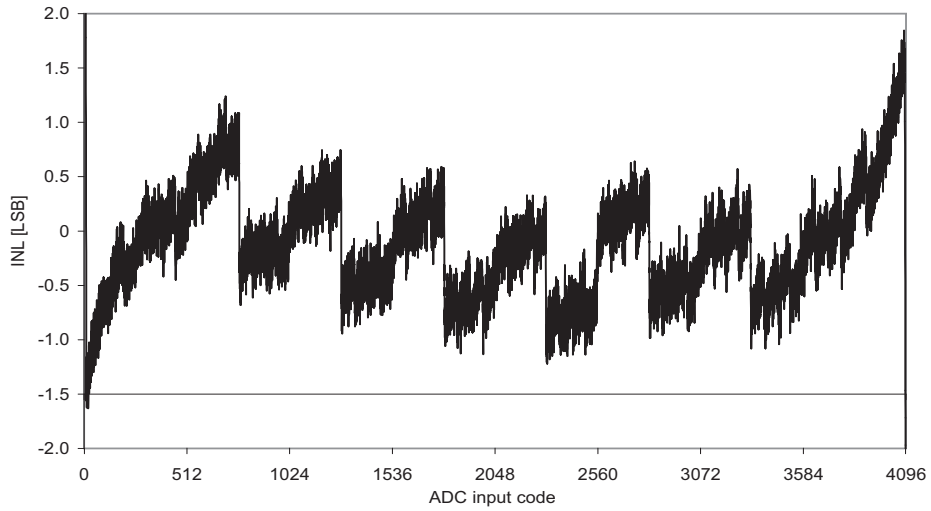


Figure 37-287. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

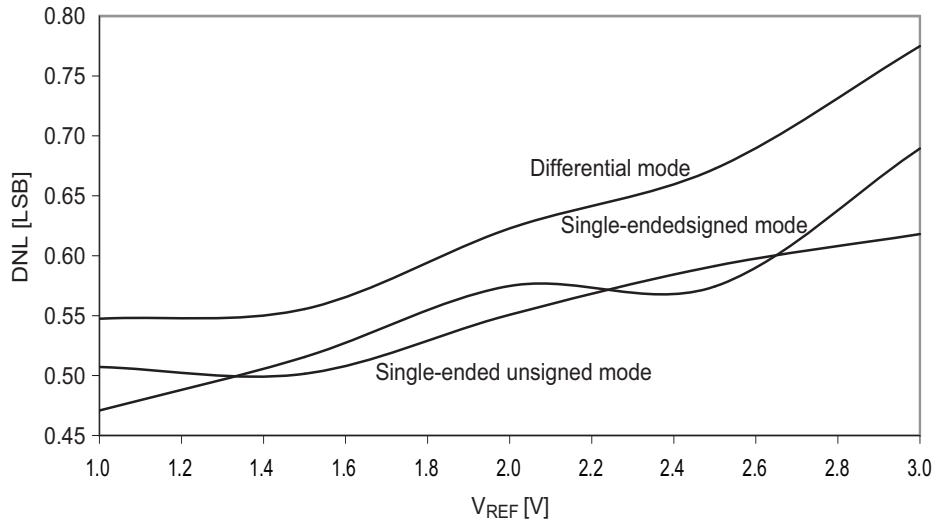
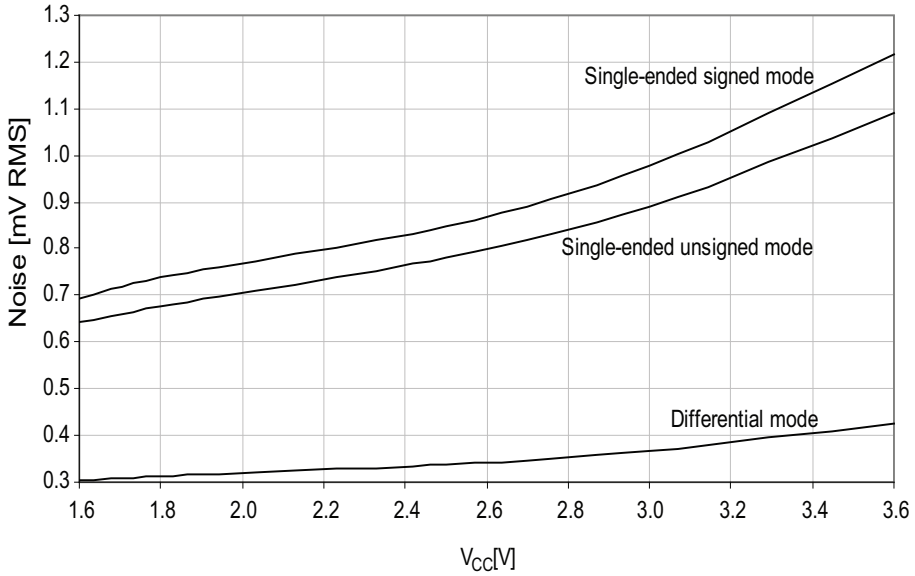


Figure 37-296. Noise vs. V_{CC}.

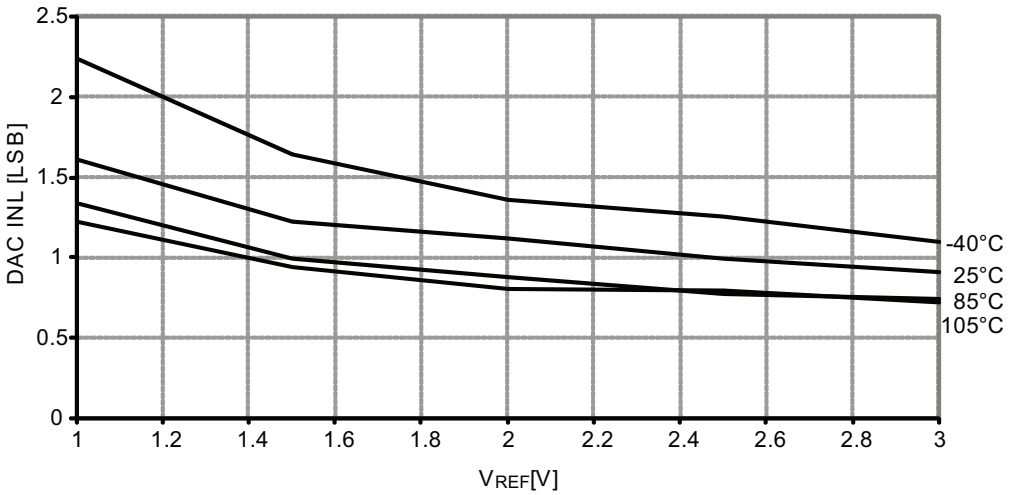
T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.4.4 DAC Characteristics

Figure 37-297. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.



37.4.8 External Reset Characteristics

Figure 37-310. Minimum Reset pin pulse width vs. V_{CC}.

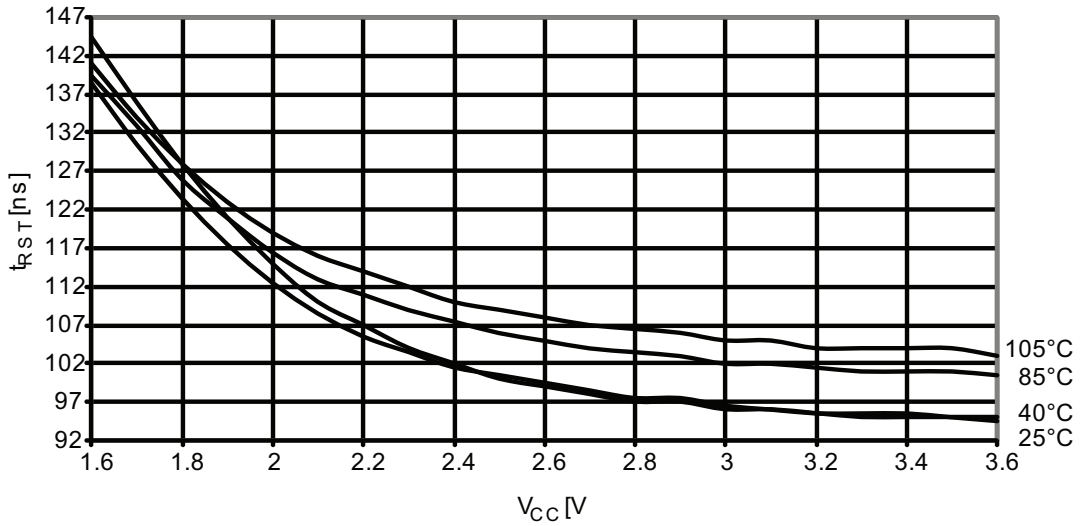


Figure 37-311. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 1.8V.

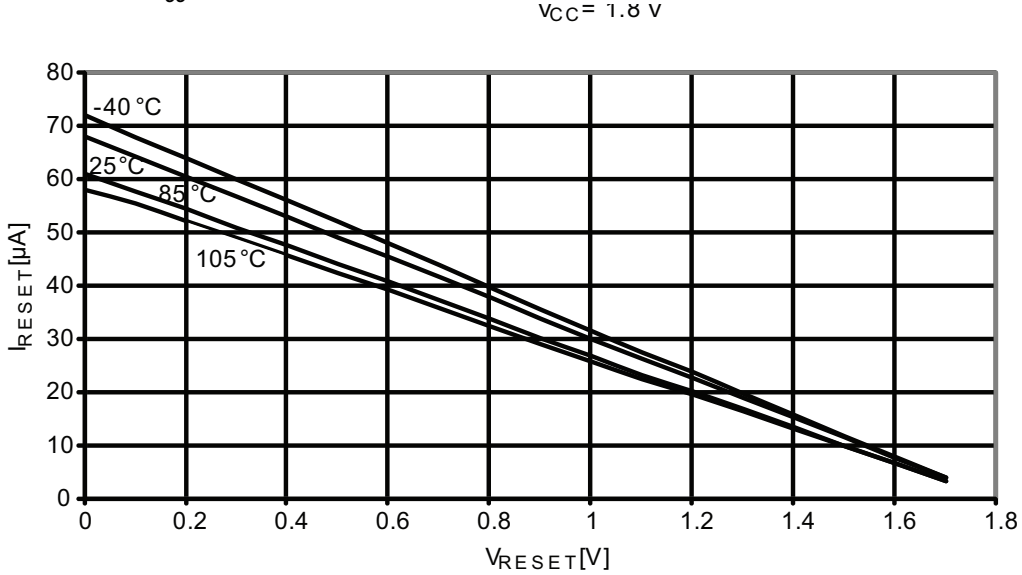


Figure 37-314. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

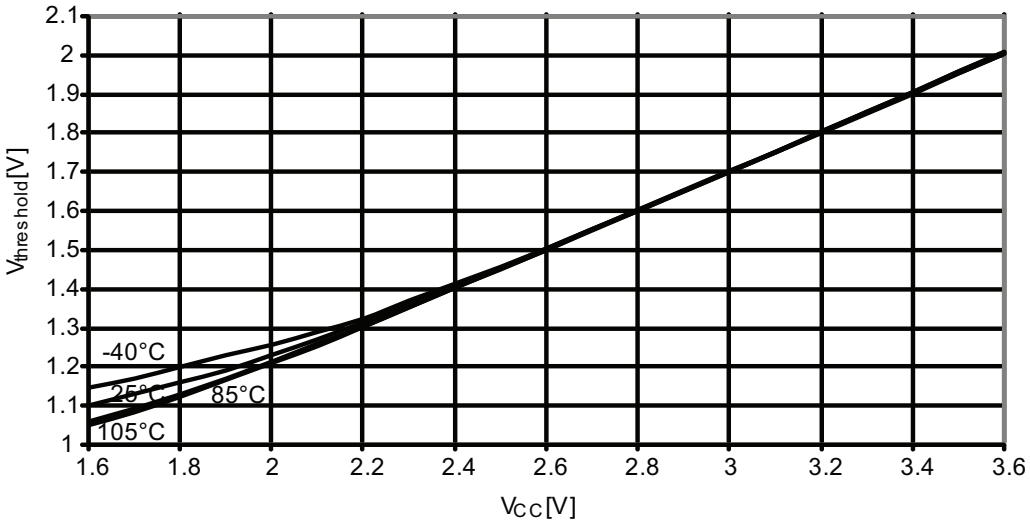


Figure 37-315. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".