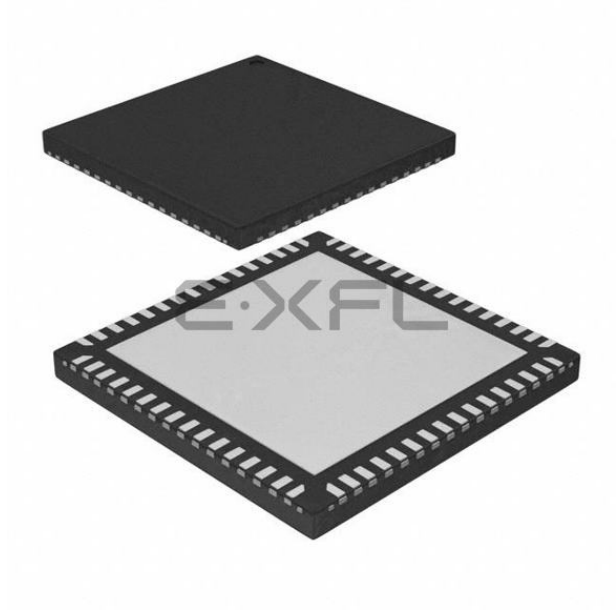

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3u-mhr

3. For packaging information, see “Packaging information” on page 71.
4. Tape and Reel.

Package Type	
64A	64-lead, 14 x 14mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
64M2	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, 7.65mm exposed pad, quad flat no-lead package (QFN)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

17. TC2 - Timer/Counter Type 2

17.1 Features

- Eight eight-bit timer/counters
  - Four Low-byte timer/counter
  - Four High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

17.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2), TCD2, TCE2 and TCF2, respectively.

Table 36-10. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL [1]	Integral non-linearity	500ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
DNL [1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	lsb
	Offset Error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain Error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-11. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL [1]	Integral Non-Linearity	500ksps	All gain settings		±1.5	±4	lsb
	Gain Error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

36.2.3 Current consumption

Table 36-36. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		280		
			V_{CC} = 3.0V		600		
		2MHz, Ext. Clk	V_{CC} = 1.8V		510	600	
			V_{CC} = 3.0V		1.1	1.5	mA
		32MHz, Ext. Clk			10.5	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		147		
		2MHz, Ext. Clk	V_{CC} = 1.8V		156	250	
			V_{CC} = 3.0V		293	600	
		32MHz, Ext. Clk			4.7	7	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.75	5.0	
		T= 105°C			4	8	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.2	3.0	
		WDT and Sampled BOD enabled, T = 85°C			3.1	7	
		WDT and Sampled BOD enabled, T = 105°C			5.3	10	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3	
			V_{CC} = 3.0V		1.2	3.5	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		150		µA

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

36.3 ATxmega192A3U

36.3.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-65. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.3.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-66. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		1.60		3.6	V
AV_{CC}	Analog Supply Voltage		1.60		3.6	V
T_A	Temperature range	85 °C	-40		85	°C
		105 °C	-40		105	
T_j	Junction temperature	85°C	-40		105	°C
		105°C	-40		125	

Table 36-67. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

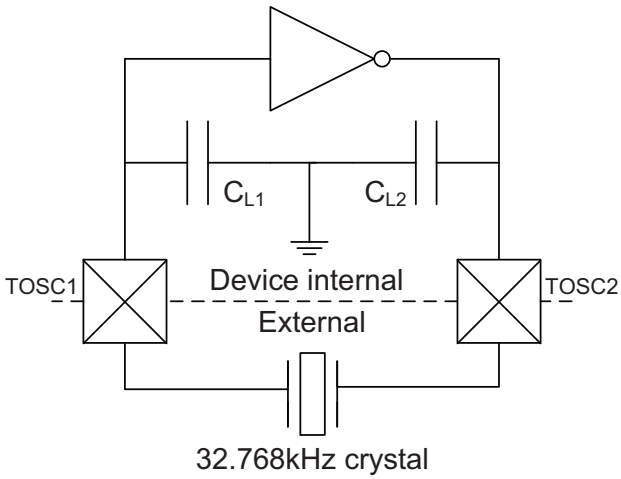
36.3.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-94. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			4.2		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			4.3		pF
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-4 for definition.

Figure 36-18. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 36-22. Maximum Frequency vs. V_{CC}.

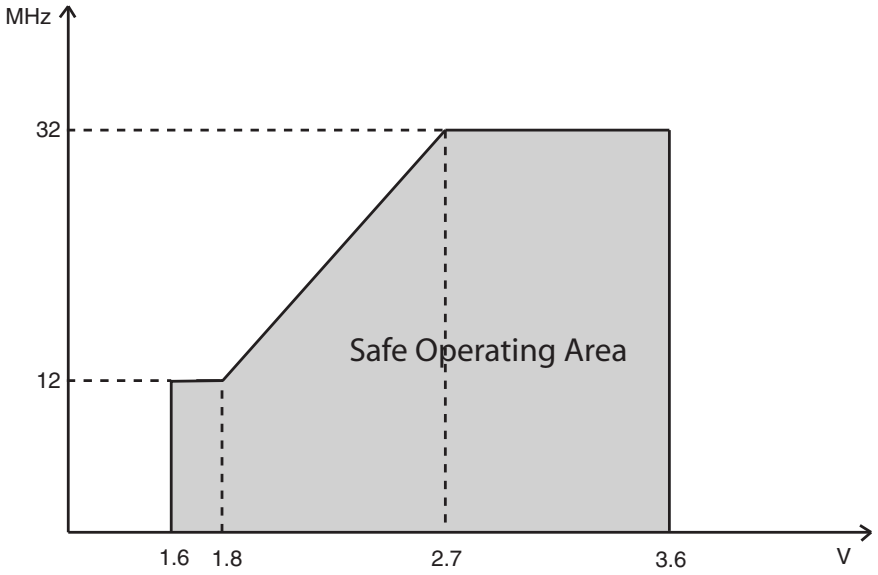


Figure 37-45. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

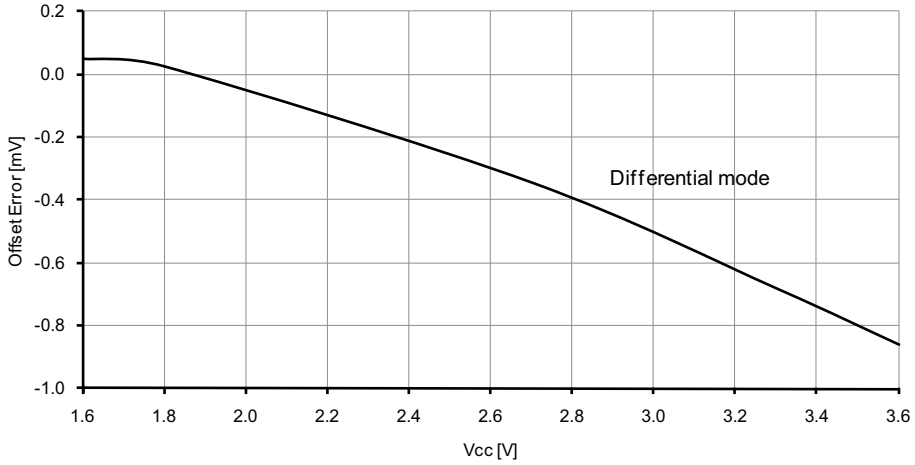


Figure 37-46. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

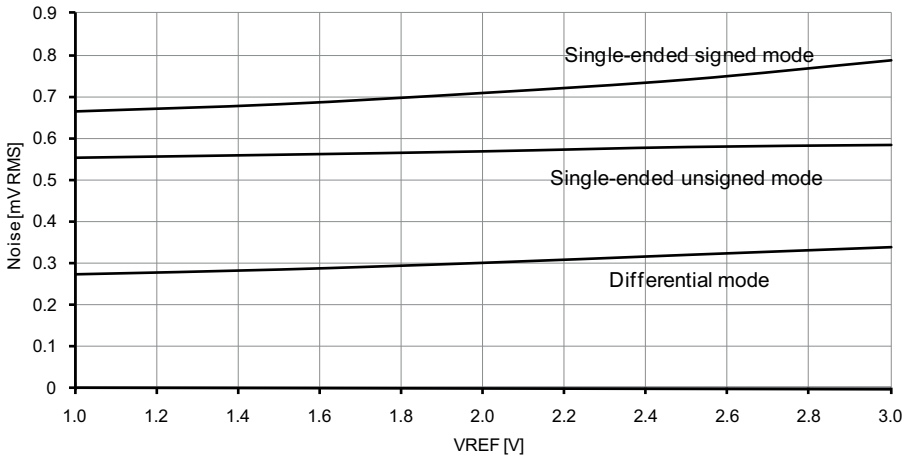
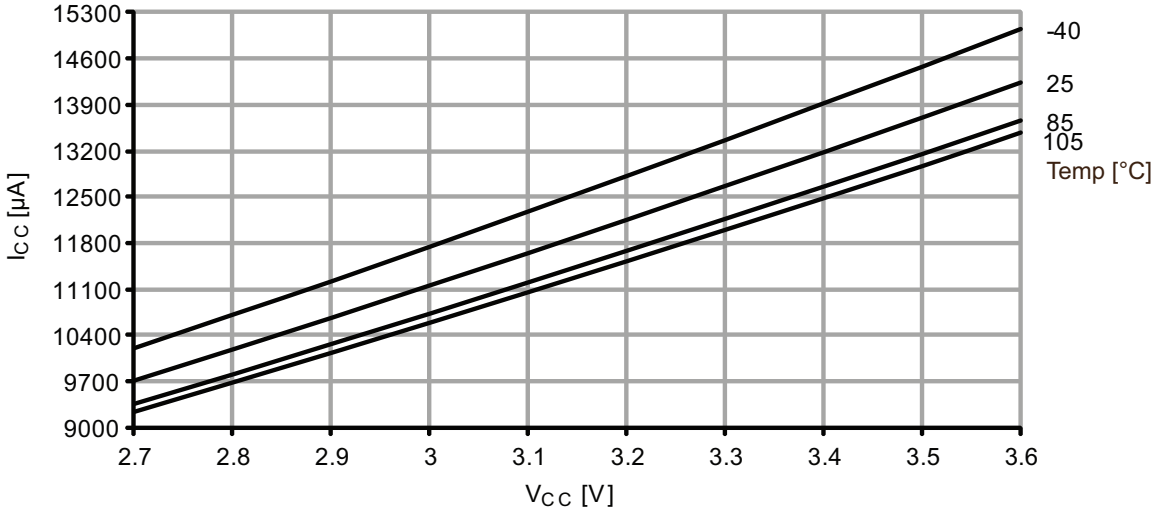


Figure 37-90. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.2.1.2 Idle mode supply current

Figure 37-91. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

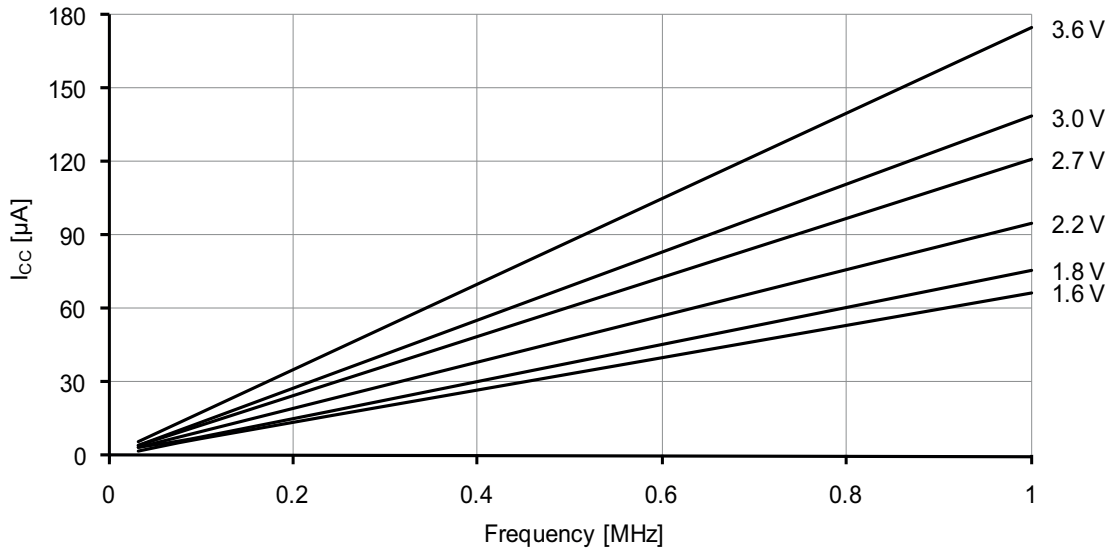


Figure 37-92. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

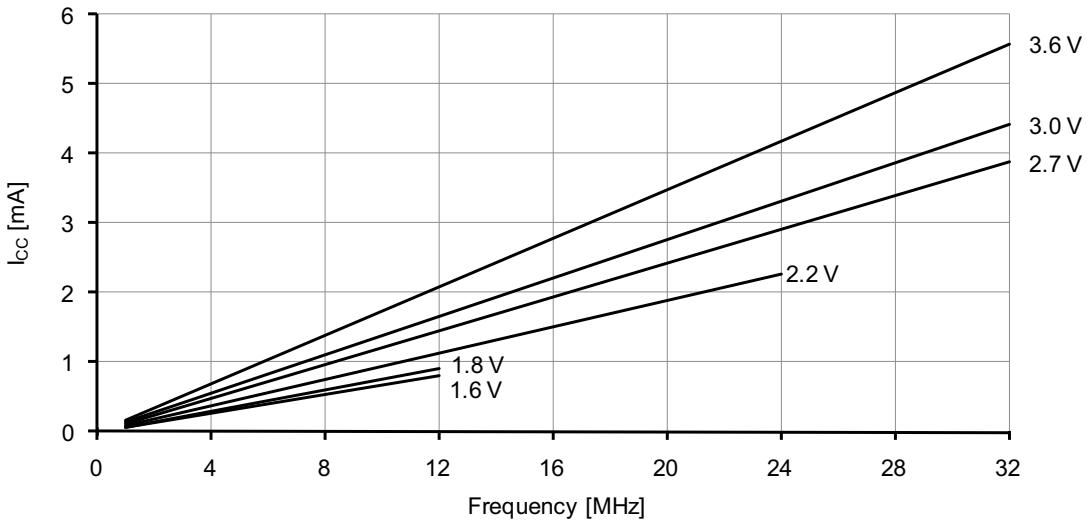


Figure 37-93. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

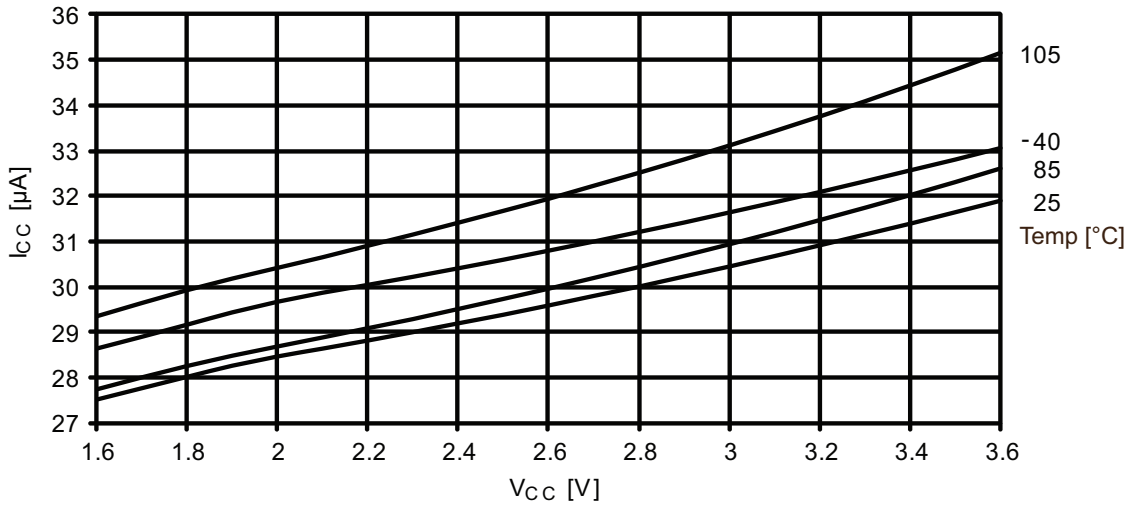


Figure 37-124. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

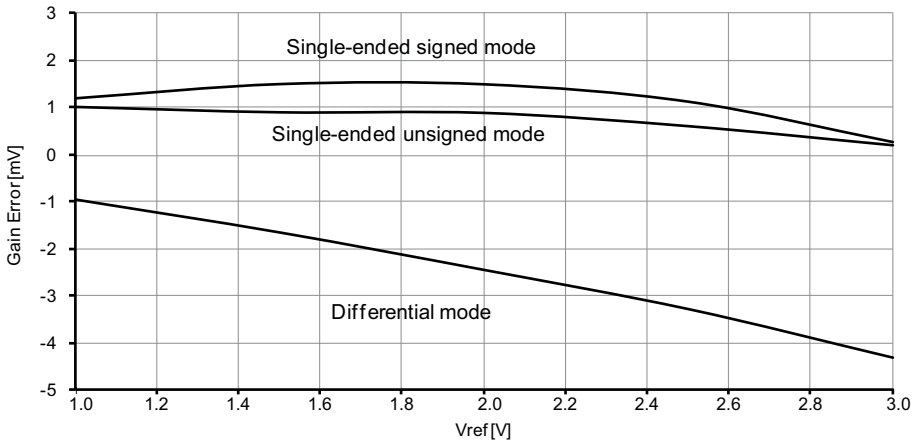


Figure 37-125. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

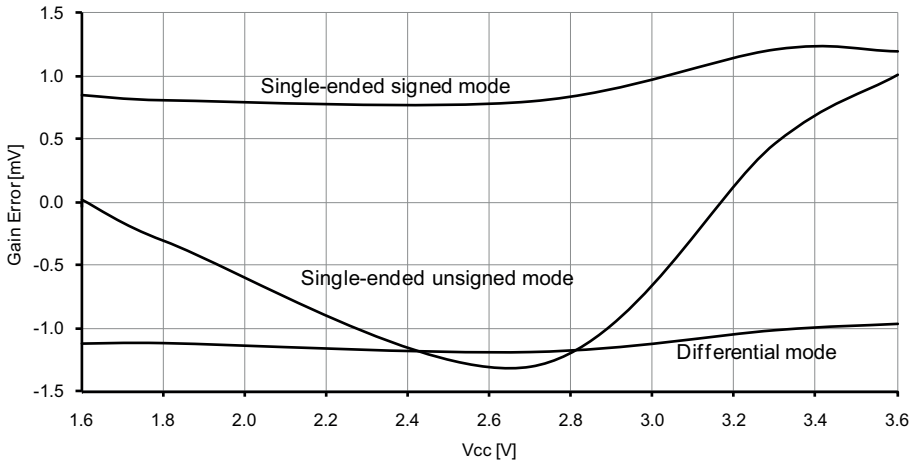


Figure 37-146. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

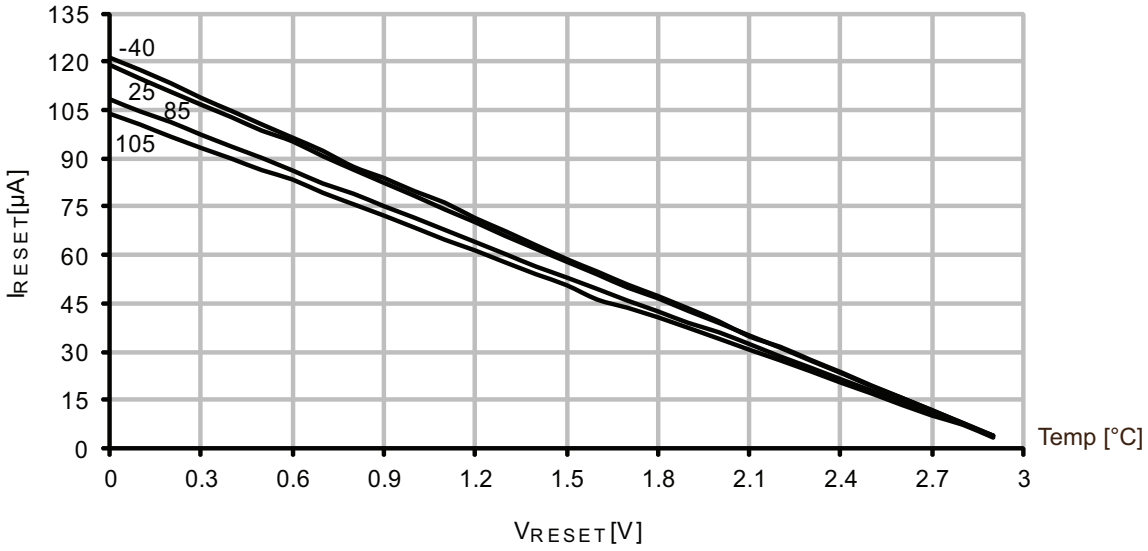


Figure 37-147. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

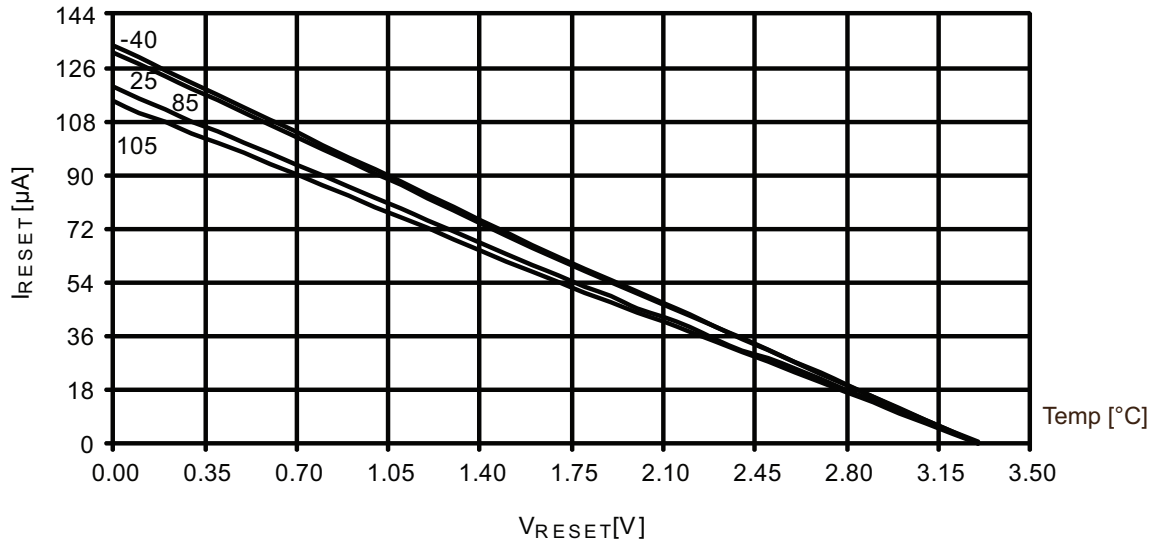


Figure 37-193. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

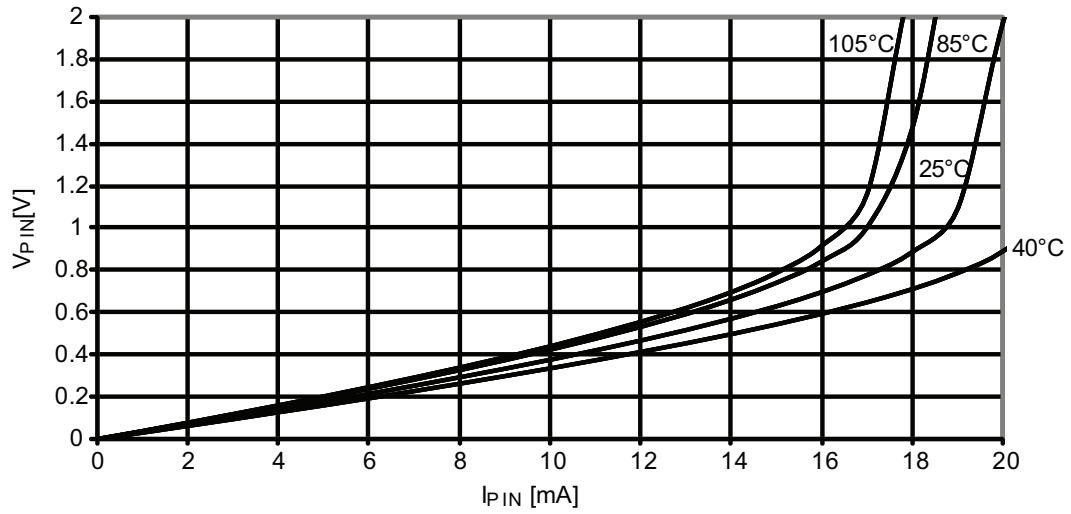


Figure 37-194. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

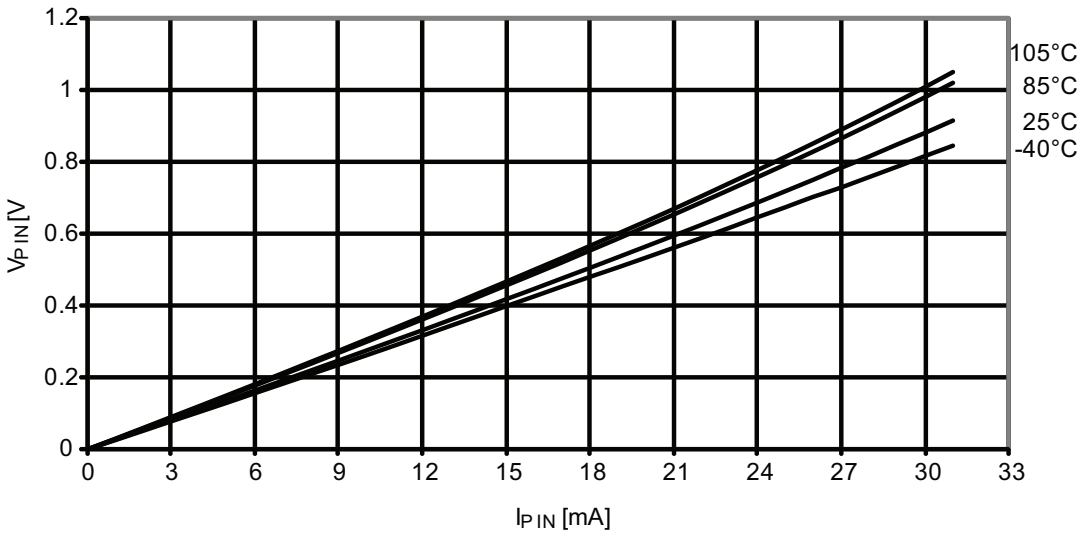


Figure 37-219. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

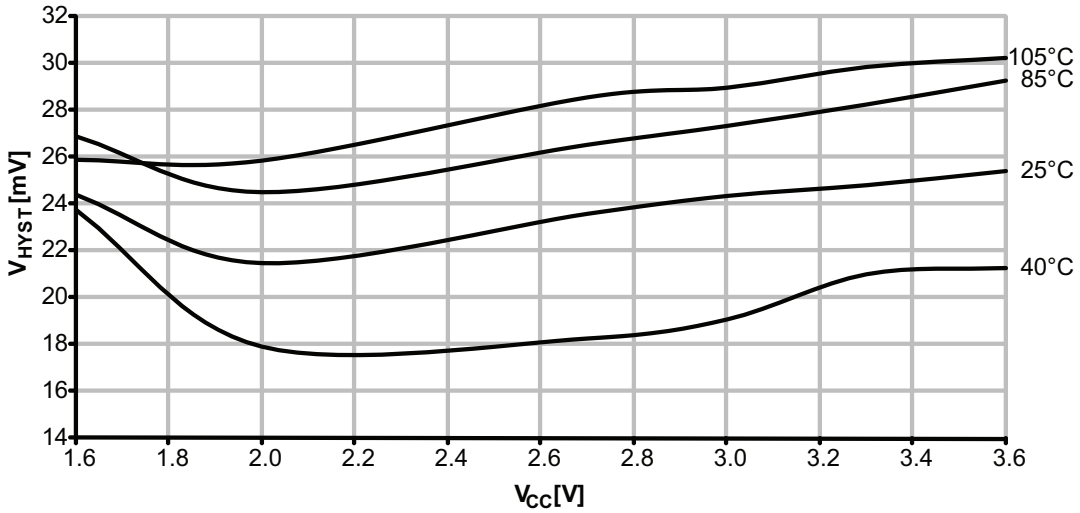


Figure 37-220. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

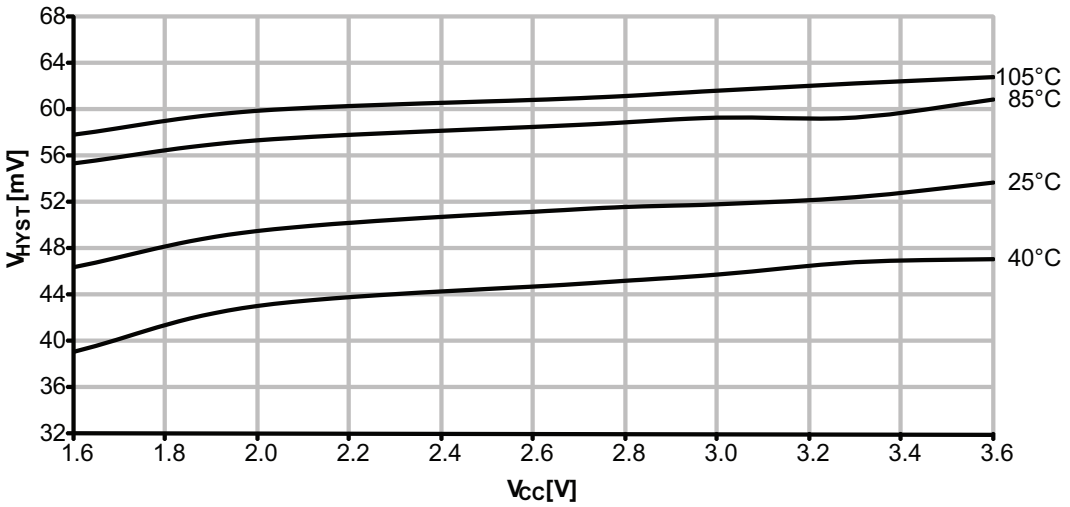


Figure 37-282. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

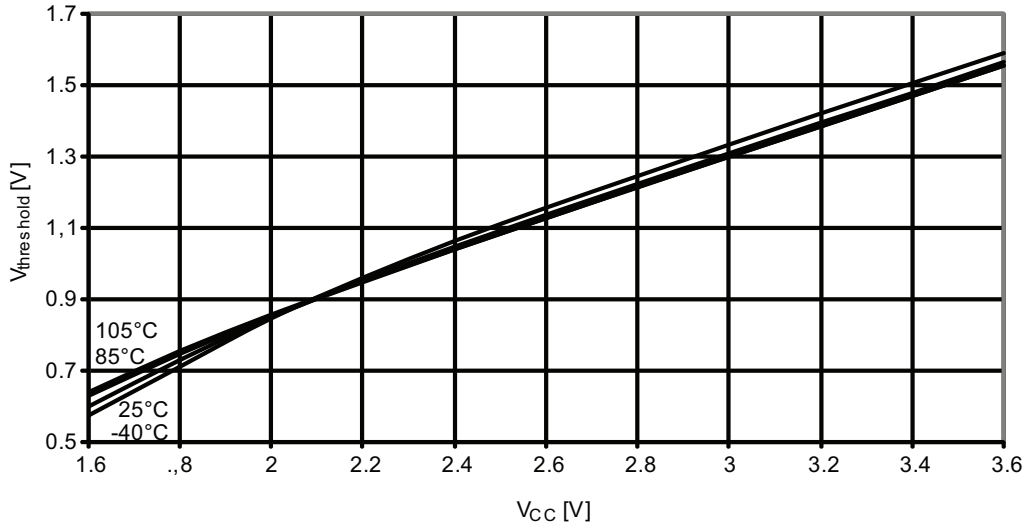


Figure 37-283. I/O pin input hysteresis vs. V_{CC}.

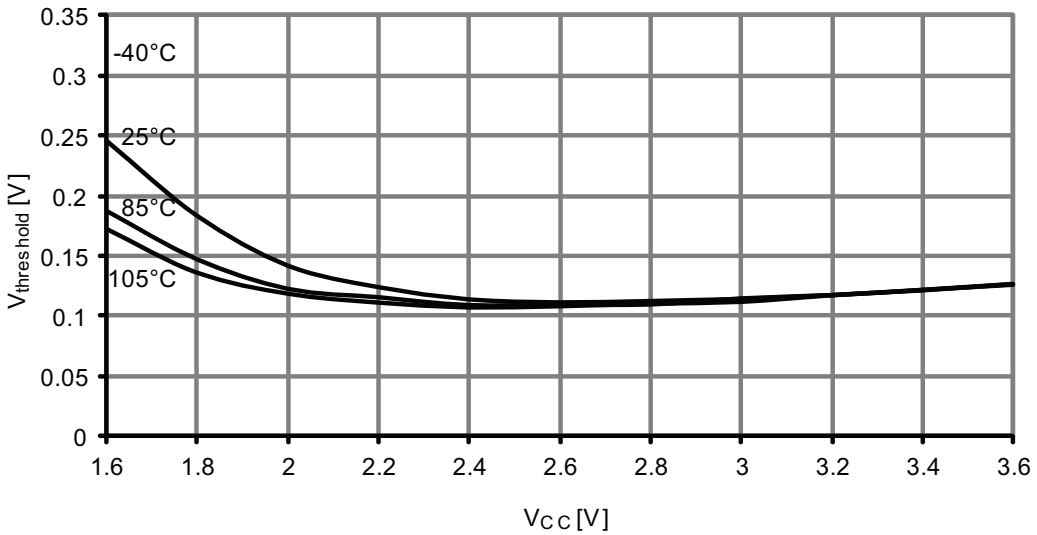


Figure 37-302. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

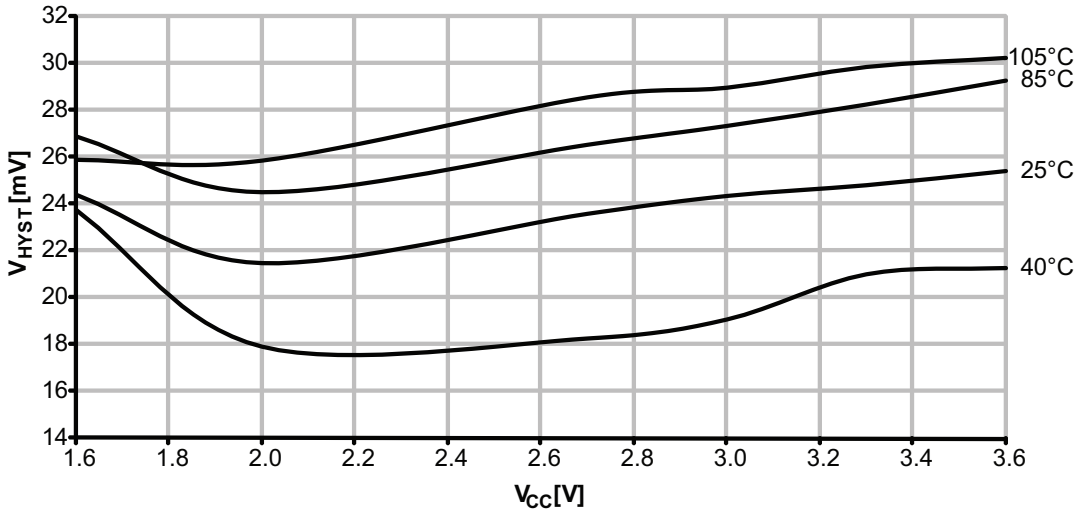


Figure 37-303. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

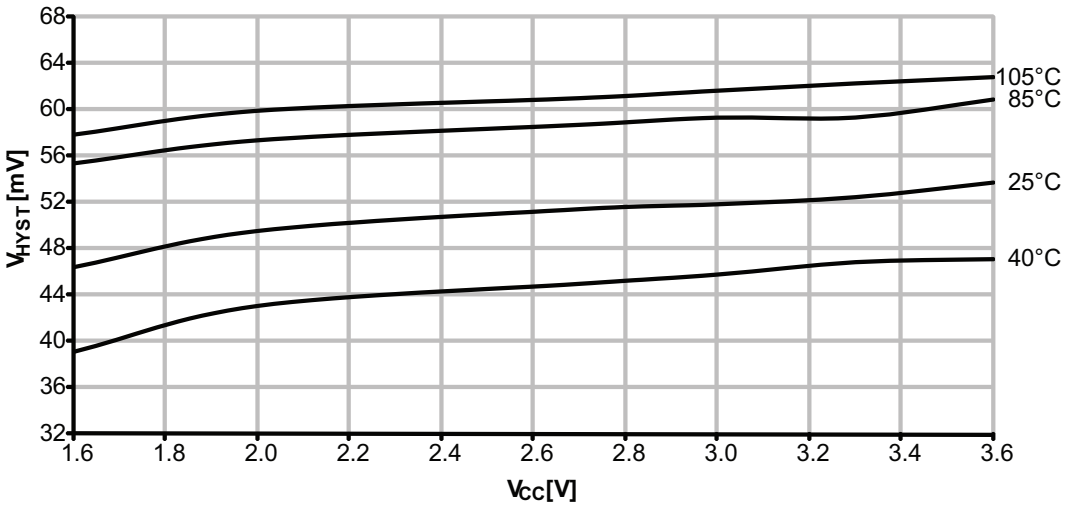


Figure 37-304. Analog comparator current source vs. calibration value.

Temperature = 25°C.

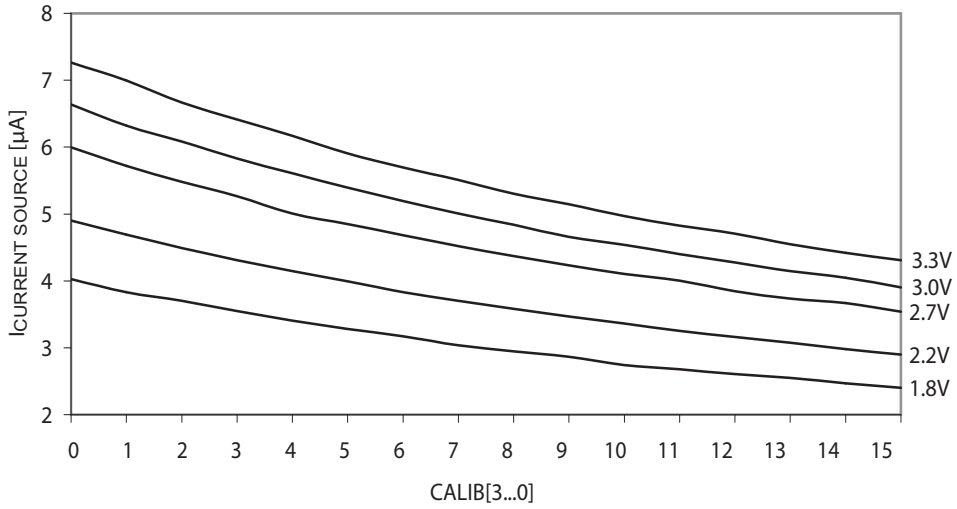
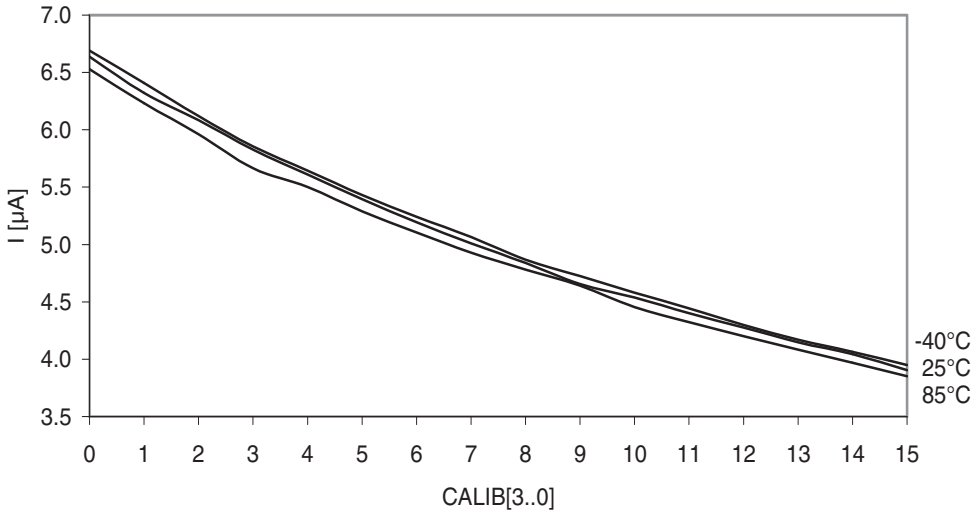


Figure 37-305. Analog comparator current source vs. calibration value.

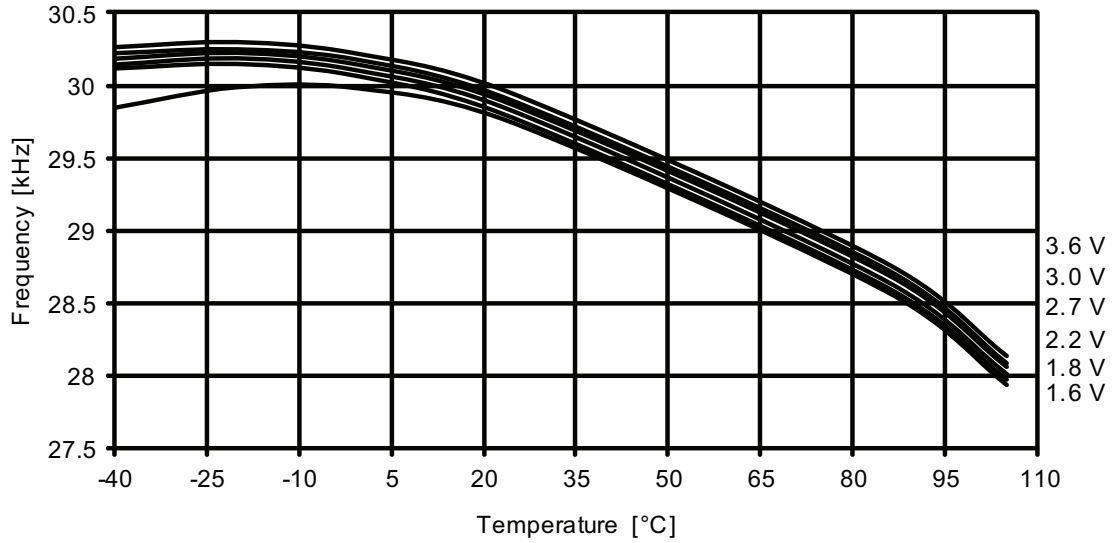
V_{CC} = 3.0V.



37.4.10 Oscillator Characteristics

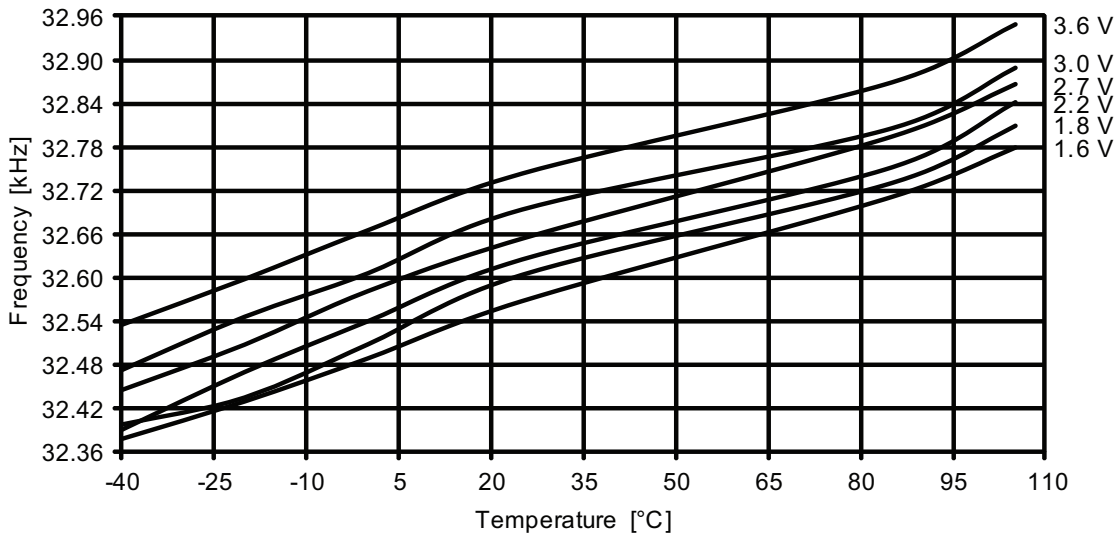
37.4.10.1 Ultra Low-Power internal oscillator

Figure 37-317. Ultra Low-Power internal oscillator frequency vs. temperature.



37.4.10.2 32.768kHz Internal Oscillator

Figure 37-318. 32.768kHz internal oscillator frequency vs. temperature.



37.4.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-327. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

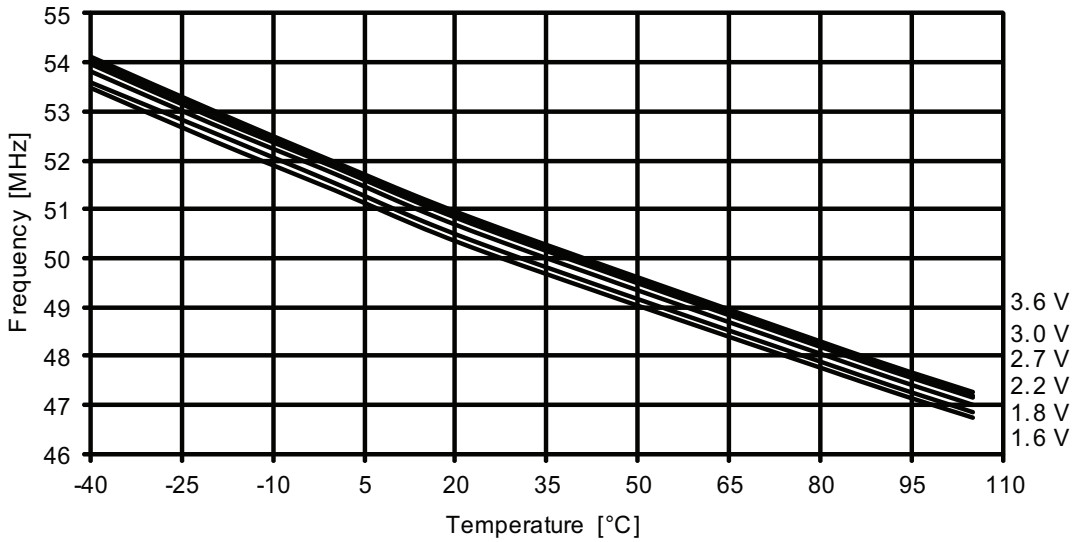
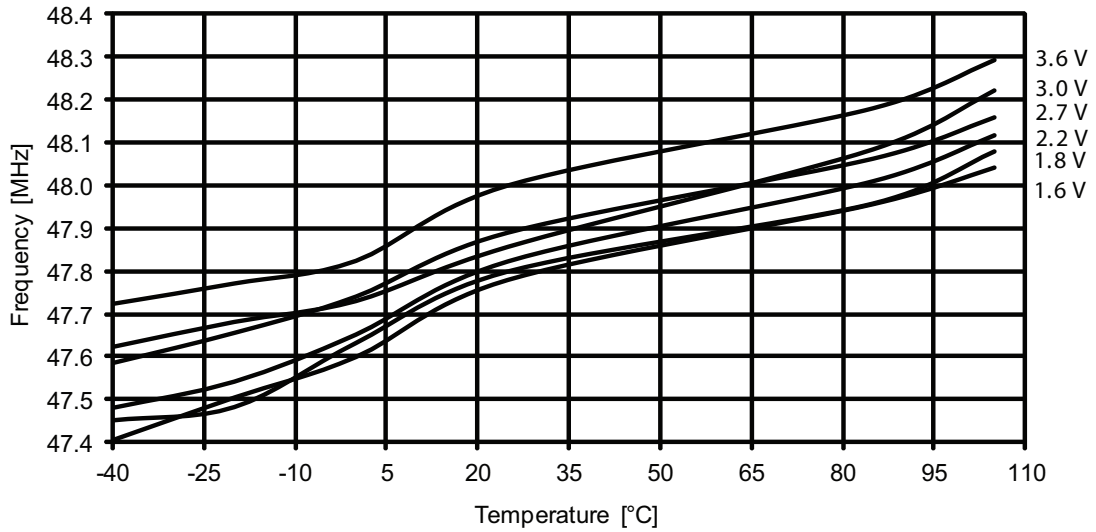


Figure 37-328. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.



6.	Updated pin numbers for Port D and F in “Alternate Pin Functions” on page 61.
7.	Removed AWEXE from the peripheral module address map in Table 33-1 on page 64.
8.	Updated the “Electrical Characteristics” on page 73 by separating the characteristics for each device.
9.	Updated DAC clock and timing characteristics for all memory: ATxmega64A3U: Table 36-13 on page 81. ATxmega128A3U: Table 36-45 on page 103. ATxmega192A3U: Table 36-77 on page 125. ATxmega256A3U: Table 36-109 on page 147.
10.	Added ESR parameter to External 16MHz crystal oscillator and XOSC characteristics: ATxmega64A3U: Table 36-29 on page 88. ATxmega128A3U: Table 36-61 on page 110 ATxmega192A3U: Table 36-93 on page 132 ATxmega256A3U: Table 36-125 on page 154
11.	Updated the “Typical Characteristics” on page 161 by separating the characteristics for each device.
12.	Added “Electrical Characteristics” and “Typical Characteristics” for both ATxmega64A3U and ATxmega128A3U.

39.4 8386B – 12/2011

1.	Updated the Figure 2-1 on page 5. JTAG written in the white color.
2.	Updated “Overview” on page 13.
3.	Updated Figure 30-1 on page 57.
4.	Updated “Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.” on page 70.
5.	Updated “Electrical Characteristics” on page 73.
6.	Updated “Typical Characteristics” on page 161.
7.	Several changes in “Typical Characteristics”

39.5 8386A – 07/2011

1.	Initial revision.