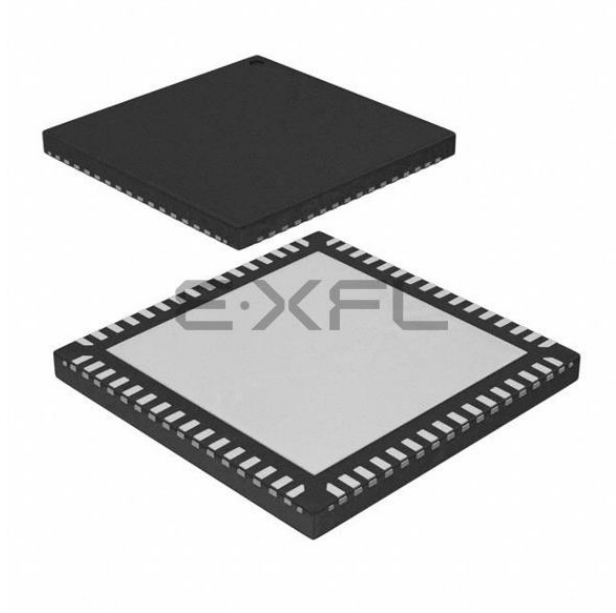


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

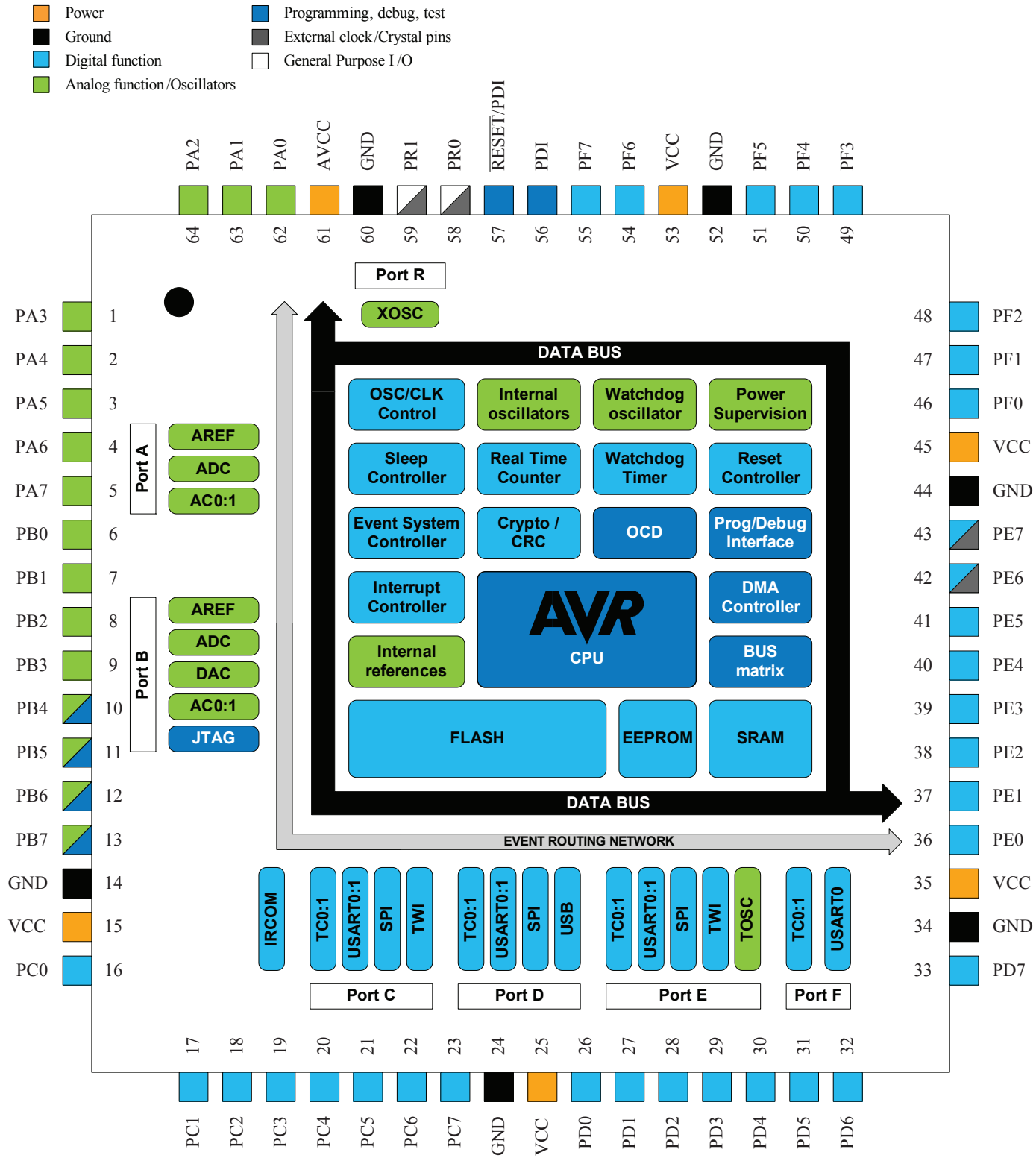
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3u-mnr

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Note: 1. For full details on pinout and alternate pin functions refer to "Pinout and Pin Functions" on page 59.

8. DMAC – Direct Memory Access Controller

8.1 Features

- Allows high speed data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four DMA channels with separate
  - transfer triggers
  - interrupt vectors
  - addressing modes
- Programmable channel priority
- From 1 byte to 16MB of data in a single transaction
  - Up to 64KB block transfers with repeat
  - 1, 2, 4, or 8 byte burst transfers
- Multiple addressing modes
  - Static
  - Incremental
  - Decremental
- Optional reload of source and destination addresses at the end of each
  - Burst
  - Block
  - Transaction
- Optional interrupt on end of transaction
- Optional connection to CRC generator for CRC on DMA data

8.2 Overview

The four-channel direct memory access (DMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four DMA channels enable up to four independent and parallel transfers.

The DMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the DMA controller can handle automatic transfer of data to/from communication modules. The DMA controller can also read from memory mapped EEPROM.

Data transfers are done in continuous bursts of 1, 2, 4, or 8 bytes. They build block transfers of configurable size from 1 byte to 64KB. A repeat counter can be used to repeat each block transfer for single transactions up to 16MB. Source and destination addressing can be static, incremental or decremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger DMA transfers.

The four DMA channels have individual configuration and control settings. This include source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the DMA controller detects an error on a DMA channel.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished, and vice versa.

MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes:
1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

36.2.11 External Reset Characteristics

Table 36-50. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			95	1000	ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 3.0 - 3.6V		0.50*V_{CC}		V
		V_{CC} = 2.3 - 2.7V		0.40*V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 3.0 - 3.6V		0.50*V_{CC}		
		V_{CC} = 2.3 - 2.7V		0.40*V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

36.2.12 Power-on Reset Characteristics

Table 36-51. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} [1]	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	V

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

36.2.13 Flash and EEPROM Memory Characteristics

Table 36-52. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

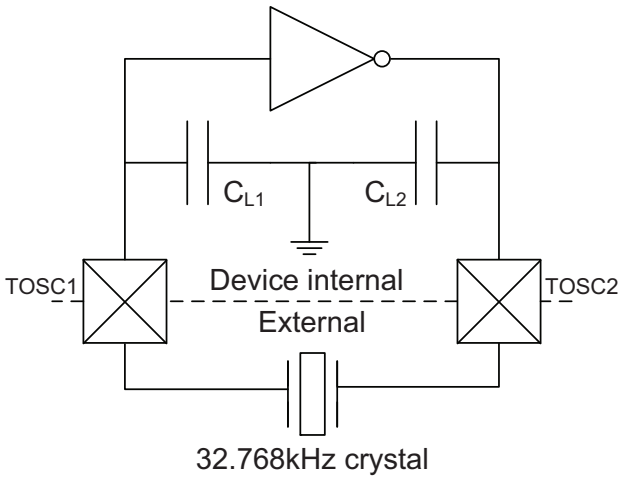
36.2.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-62. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			4.2		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			4.3		pF
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-4 for definition.

Figure 36-11. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

36.4.14.6 External clock characteristics

Figure 36-24. External clock drive waveform

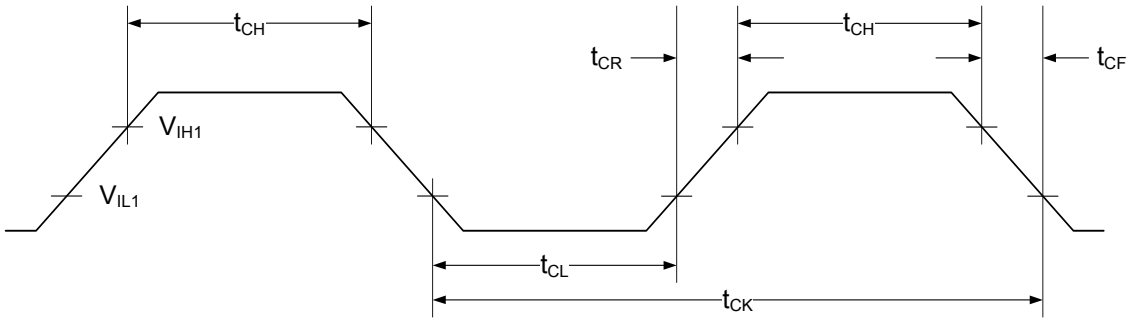


Table 36-123. External clock used as system clock without prescaling.

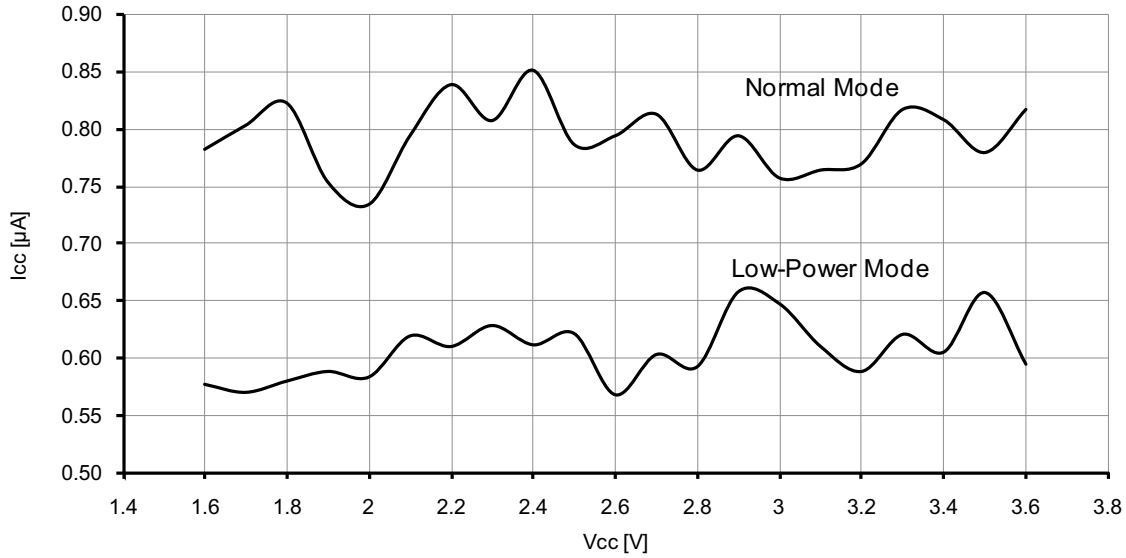
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

37.1.1.4 Power-save mode supply current

Figure 37-17. Power-save mode supply current vs. V_{CC}.

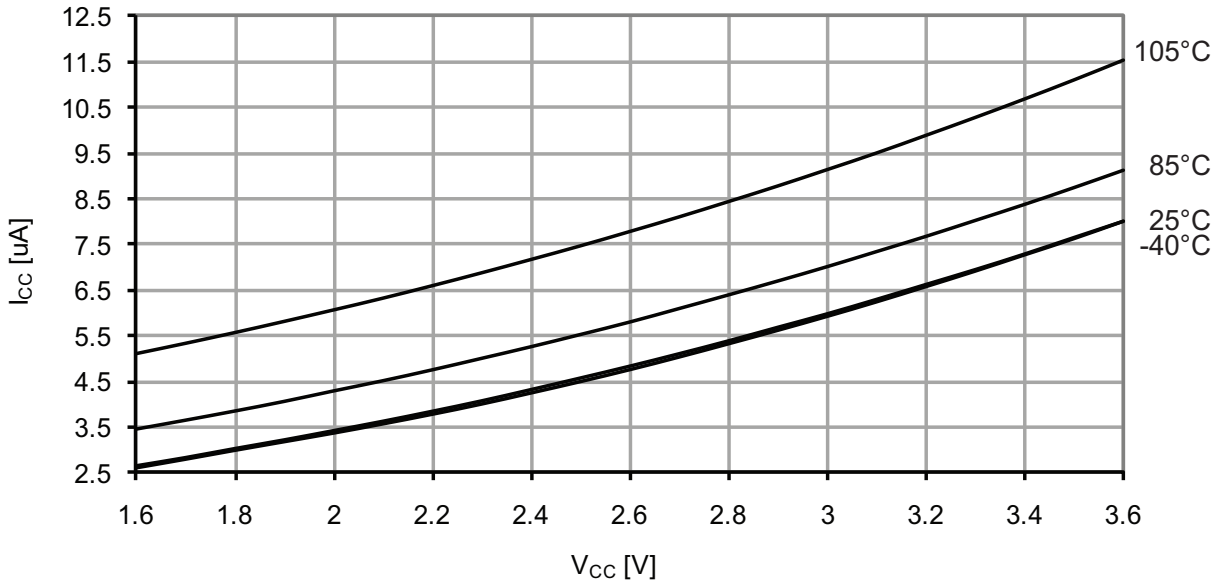
Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.1.1.5 Standby mode supply current

Figure 37-18. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.



37.1.2.2 Output Voltage vs. Sink/Source Current

Figure 37-23. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

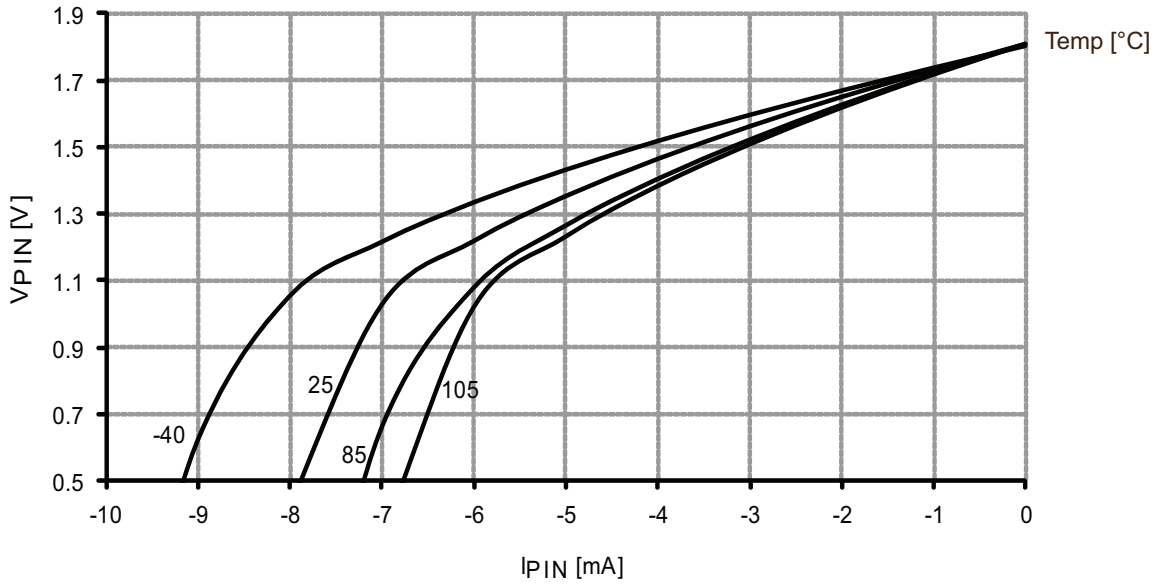


Figure 37-24. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

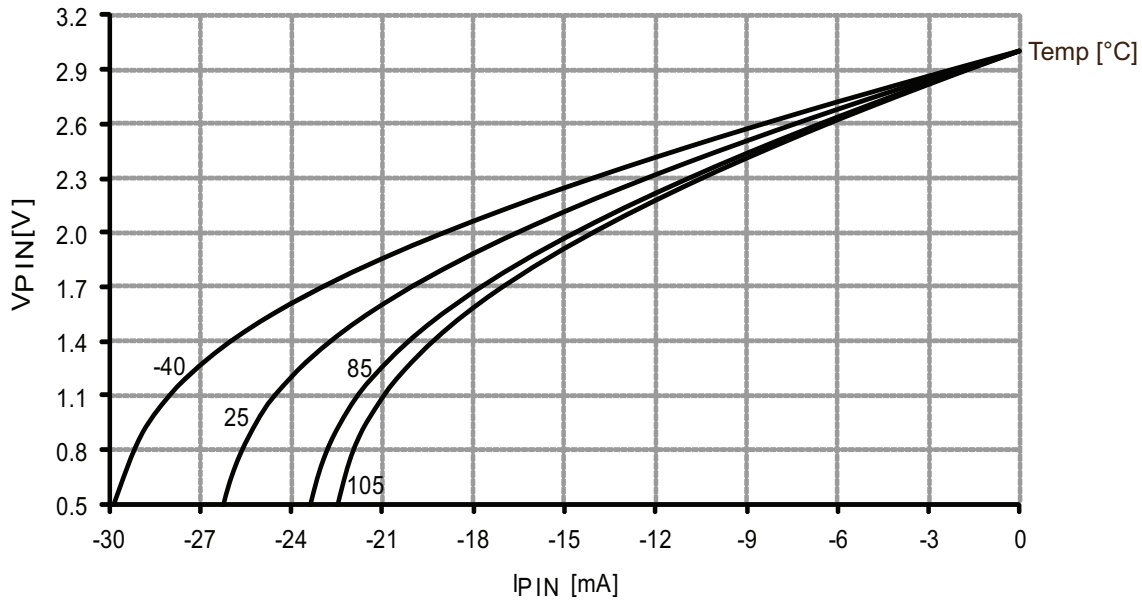


Figure 37-92. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

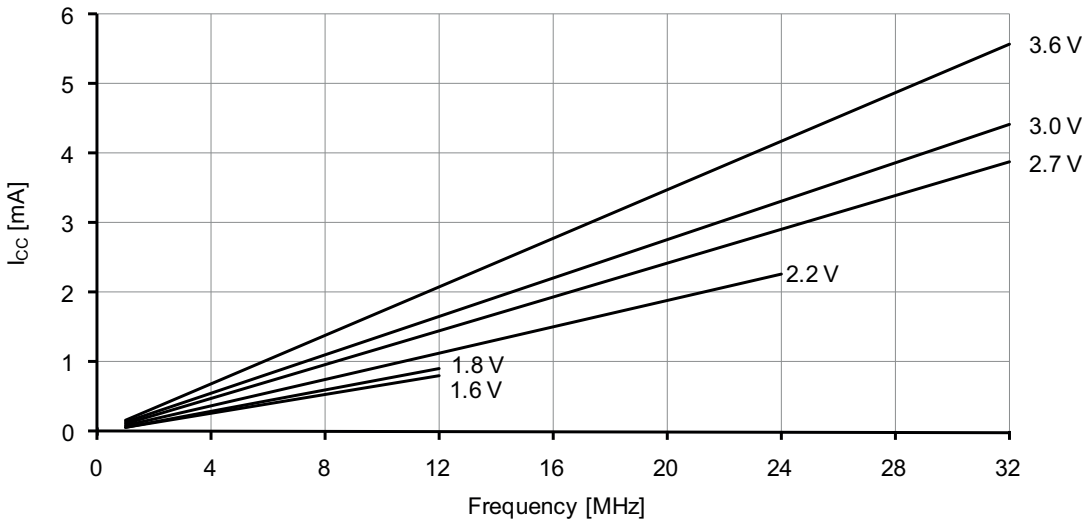


Figure 37-93. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

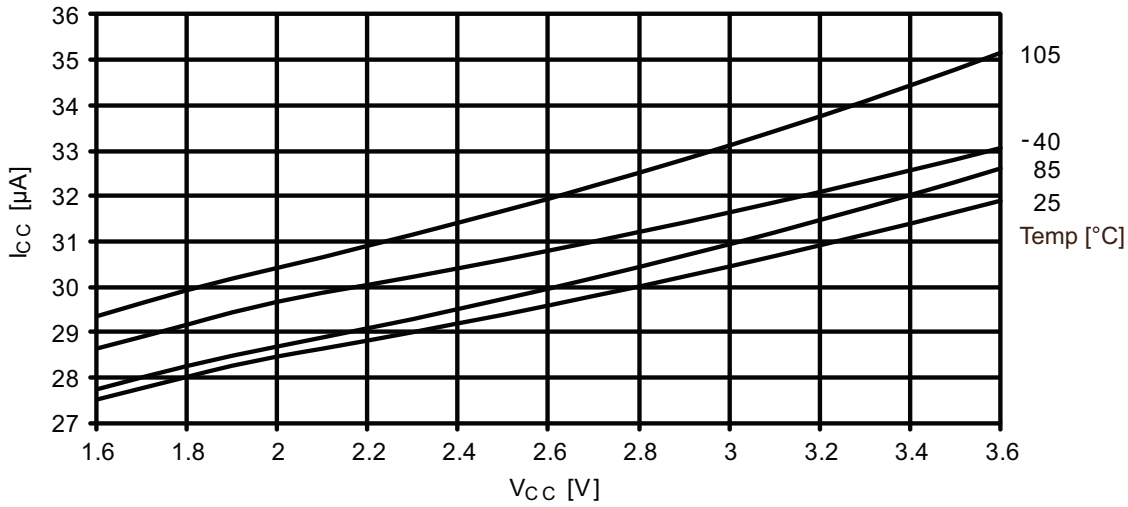


Figure 37-96. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

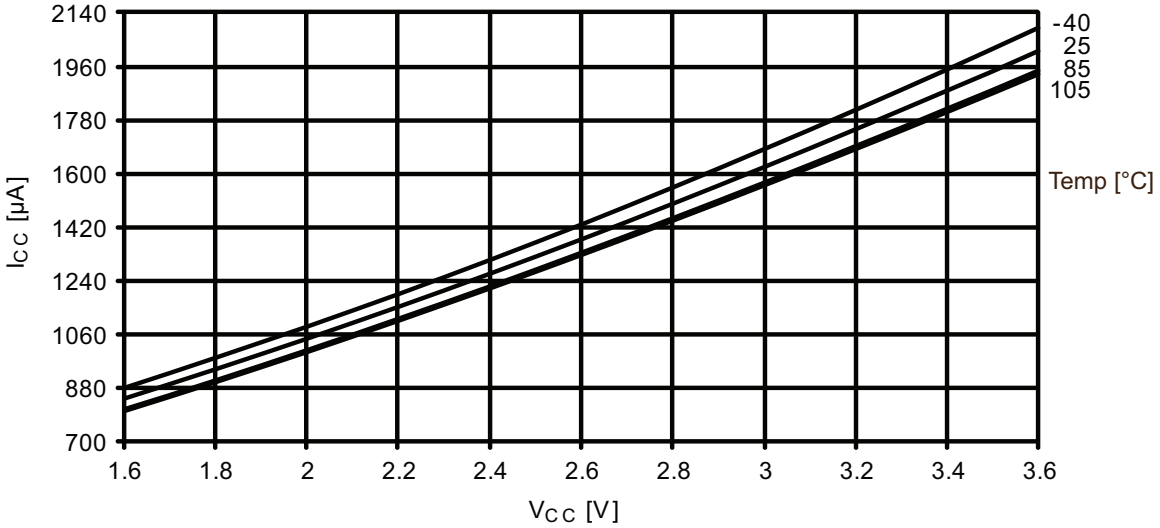


Figure 37-97. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.

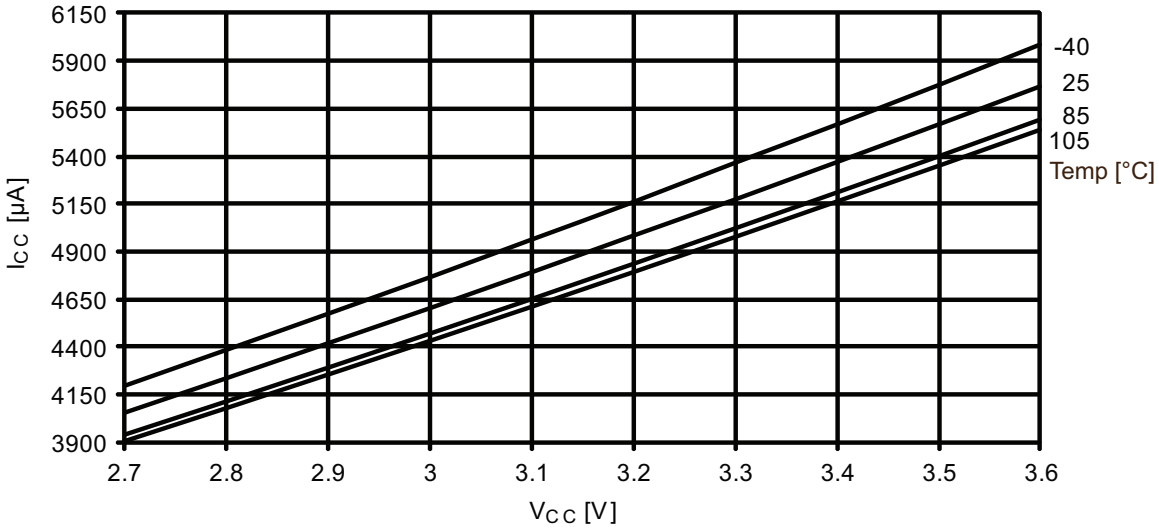
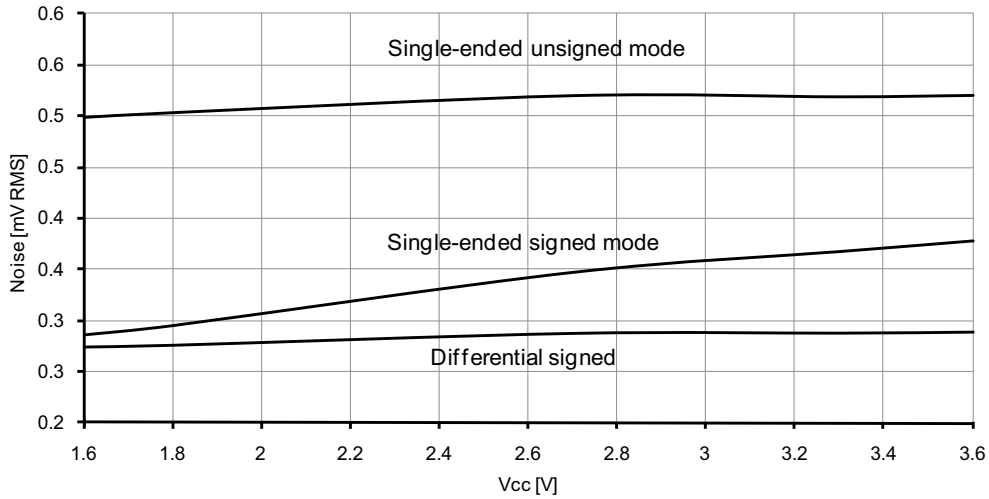


Figure 37-130. Noise vs. V_{CC}.

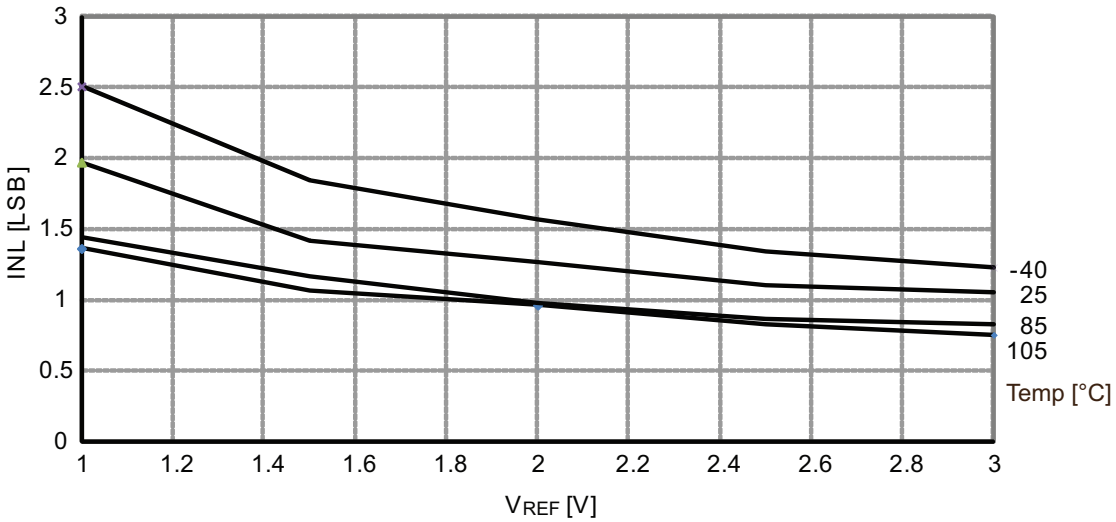
T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.2.4 DAC Characteristics

Figure 37-131. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.



37.2.5 Analog Comparator Characteristics

Figure 37-134. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis.

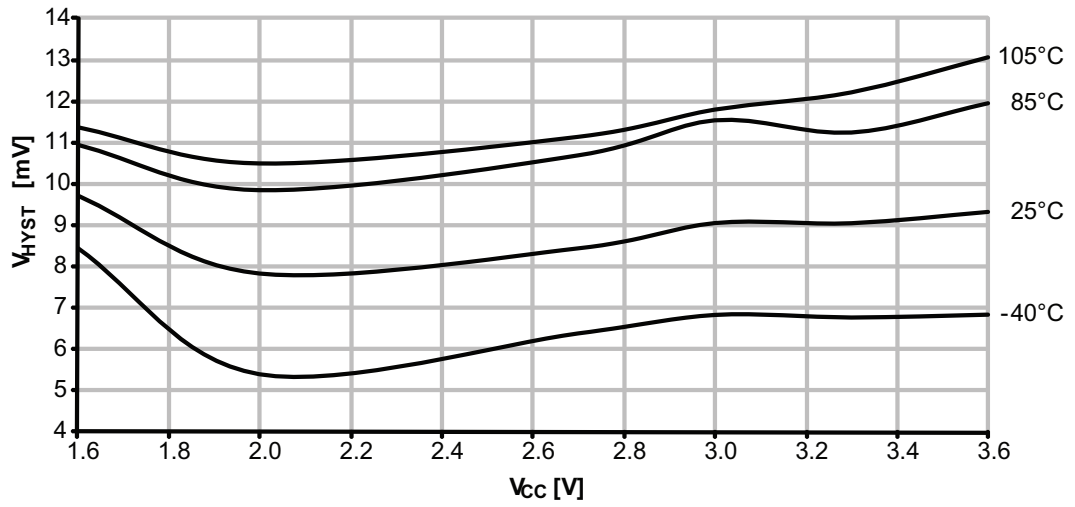


Figure 37-135. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis.

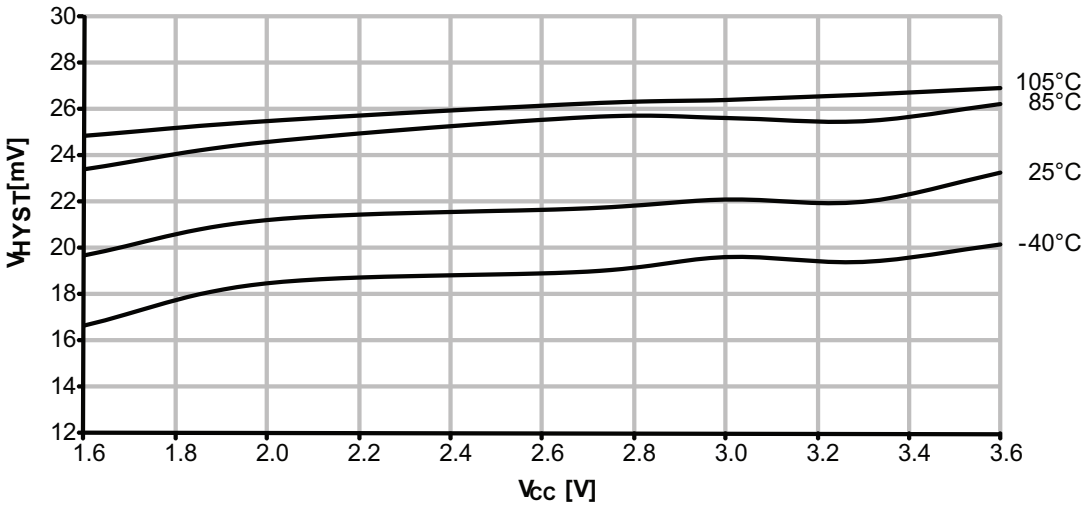


Figure 37-136. Analog comparator hysteresis vs. V_{CC}

High-speed mode, large hysteresis.

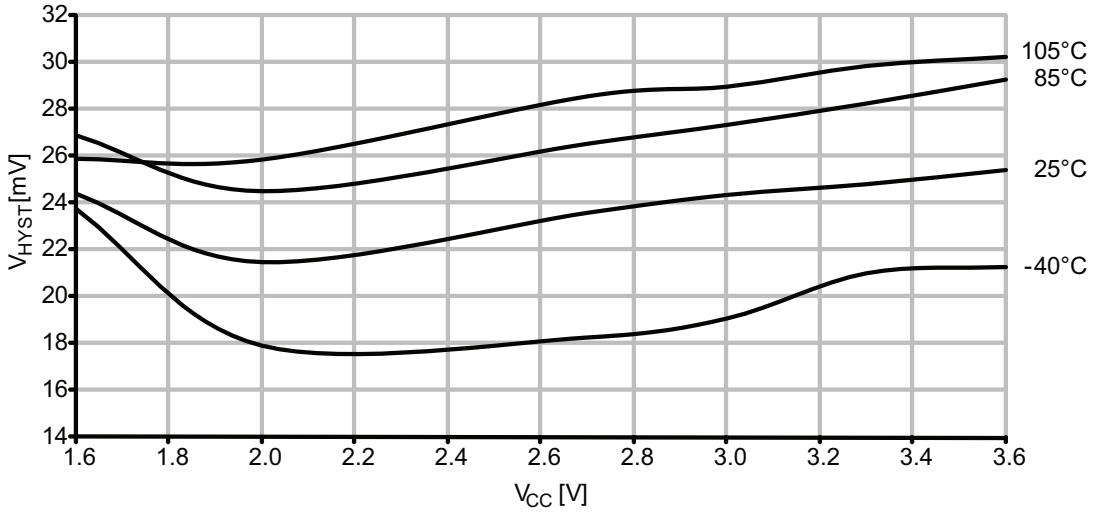


Figure 37-137. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

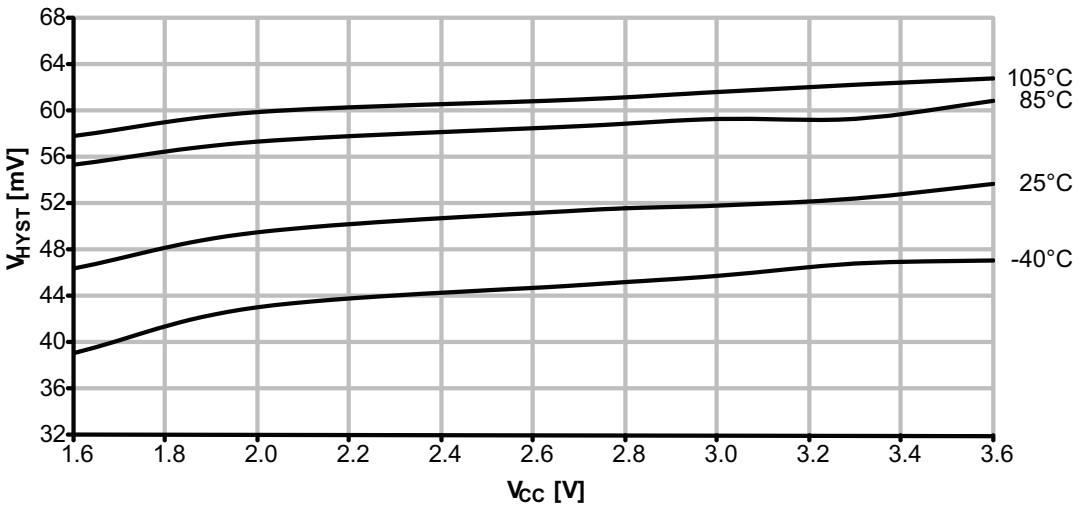


Figure 37-146. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

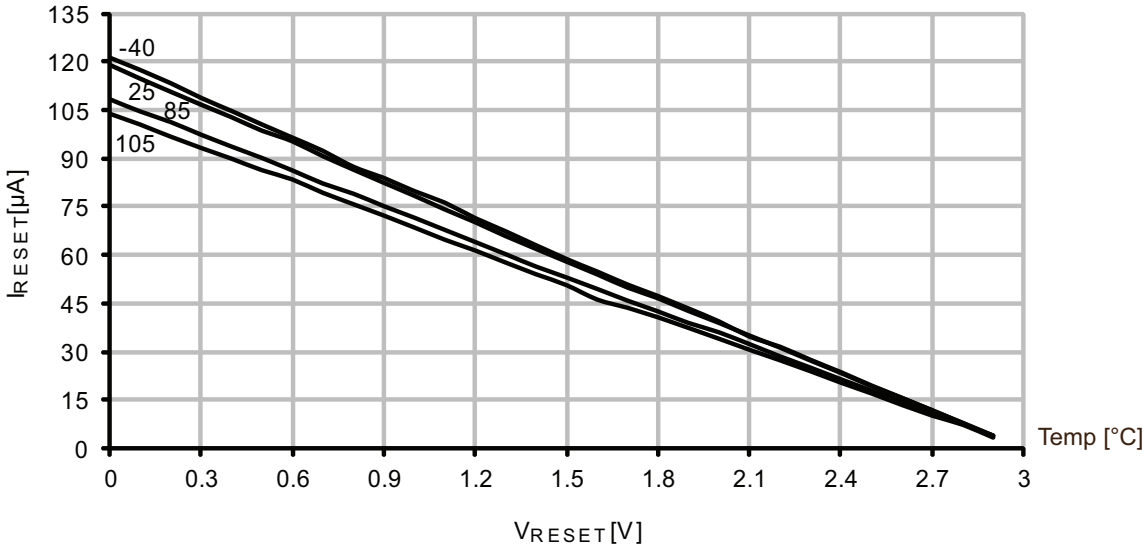
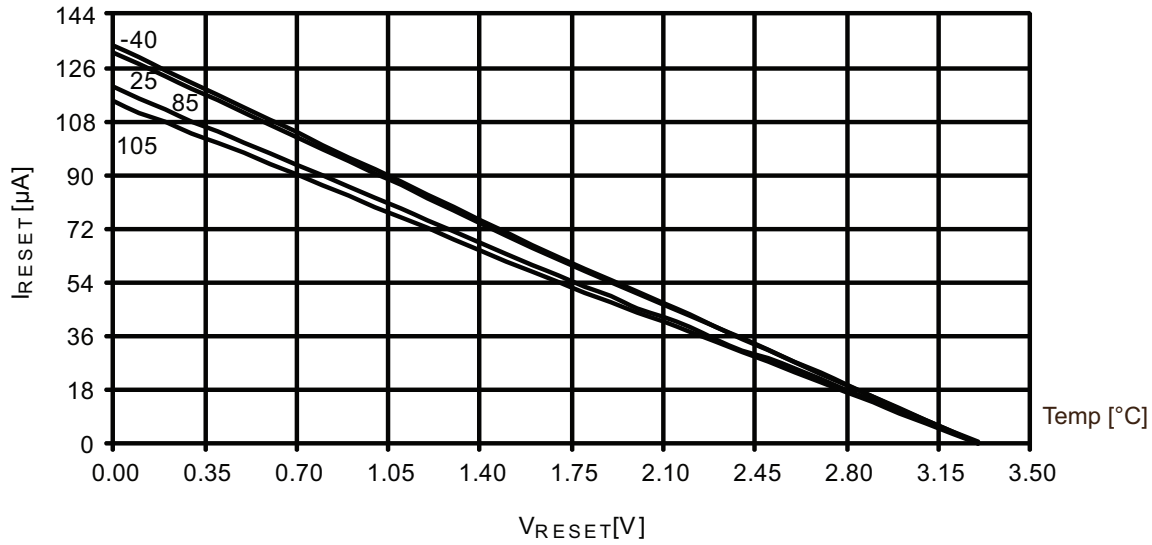


Figure 37-147. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.



37.3.2.3 Thresholds and Hysteresis

Figure 37-197. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

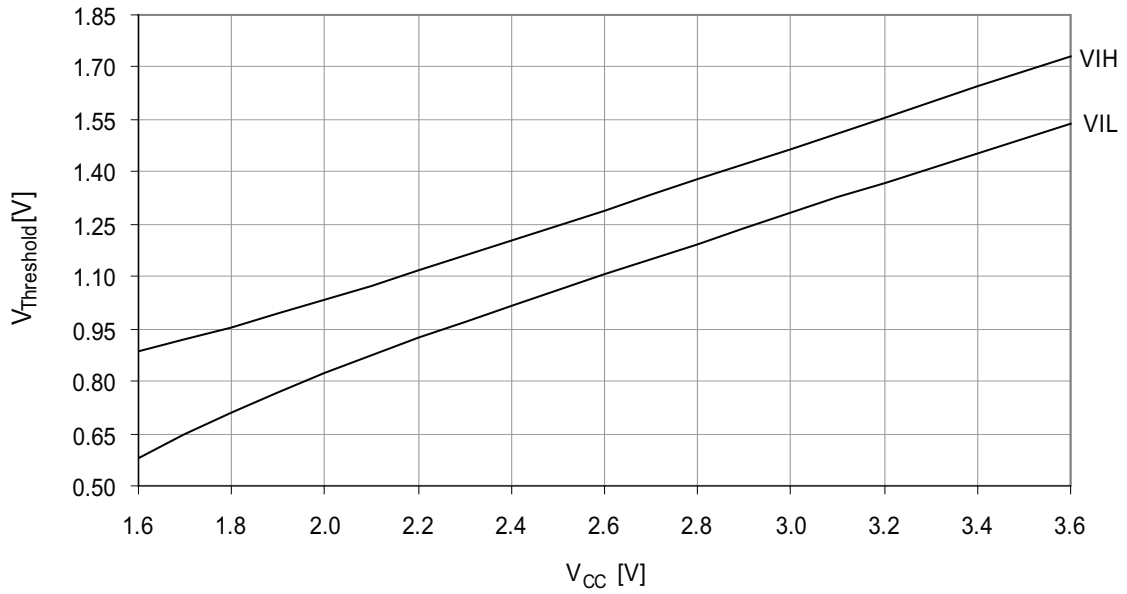


Figure 37-198. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

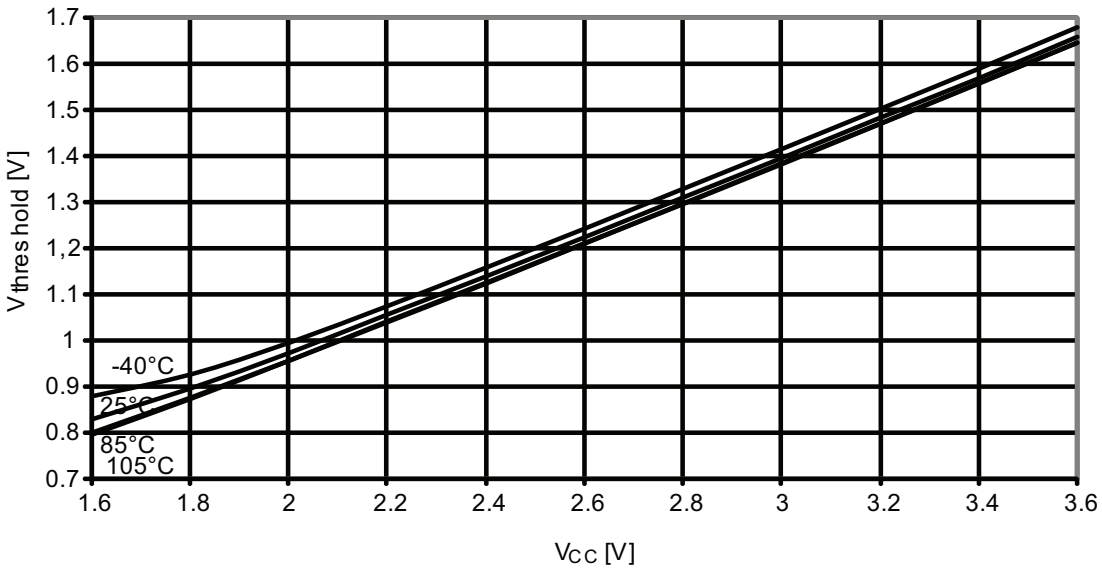


Figure 37-215. DNL error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V.

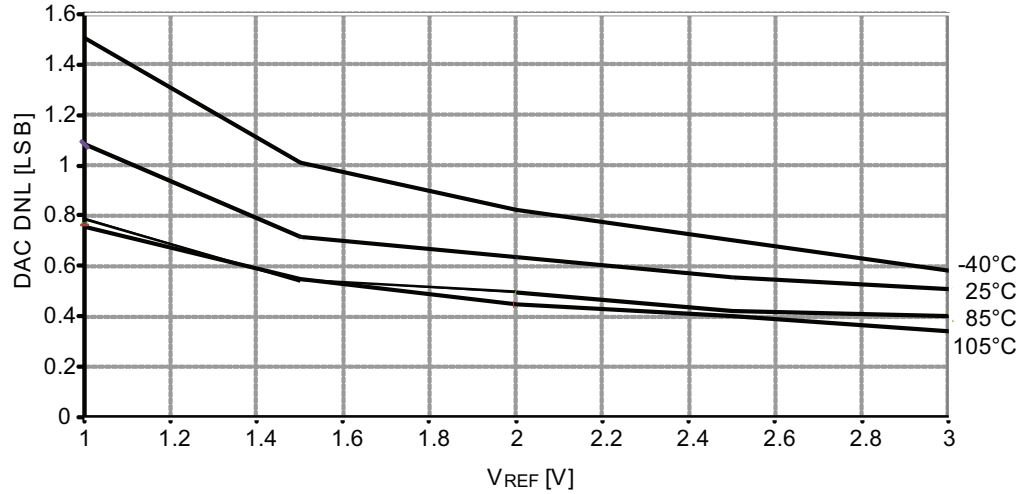


Figure 37-216. DAC noise vs. temperature.

V_{CC} = 3.3V, V_{REF} = 2.0V.

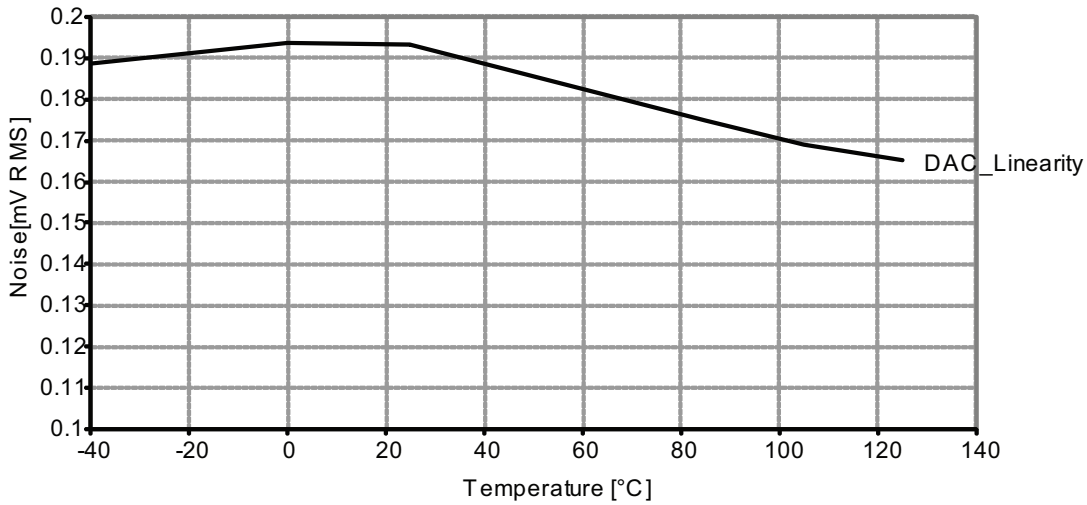


Figure 37-270. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

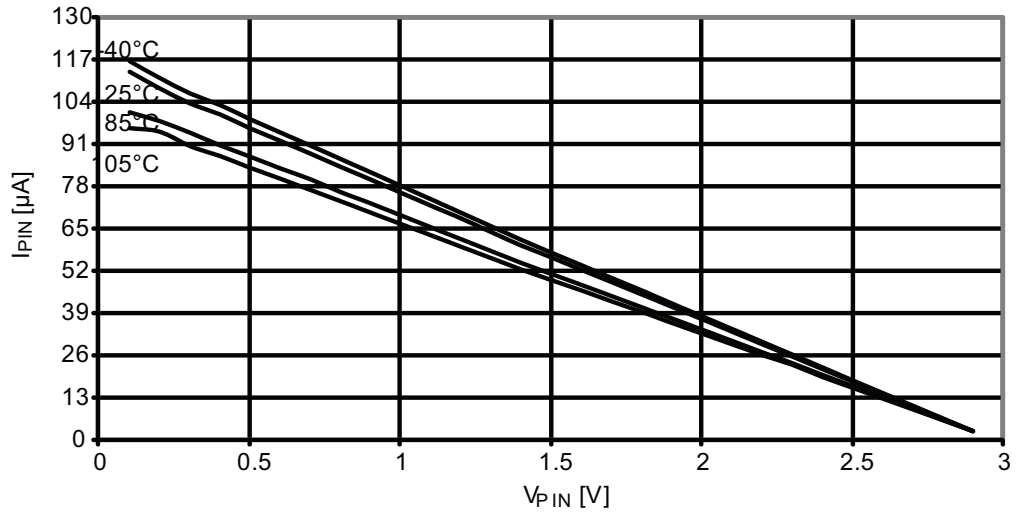


Figure 37-271. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.

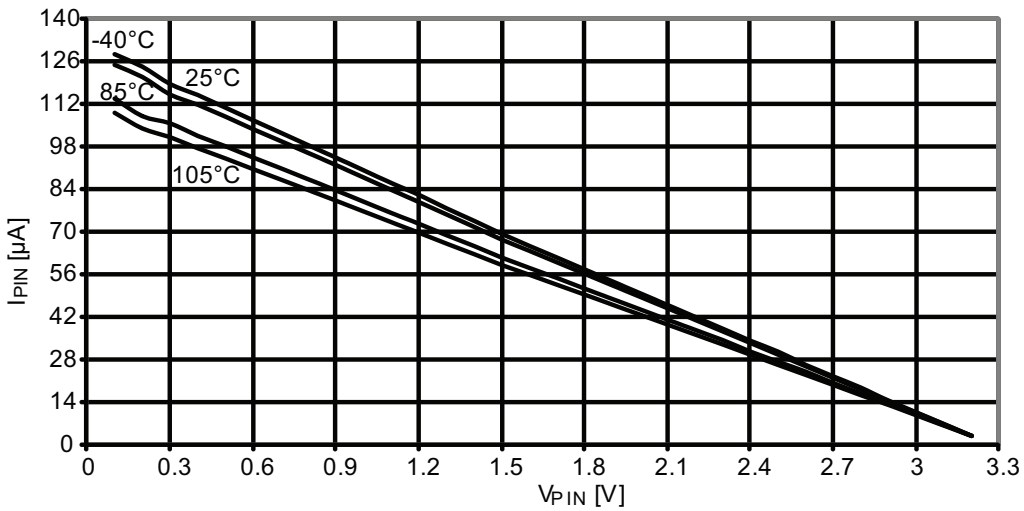


Figure 37-314. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

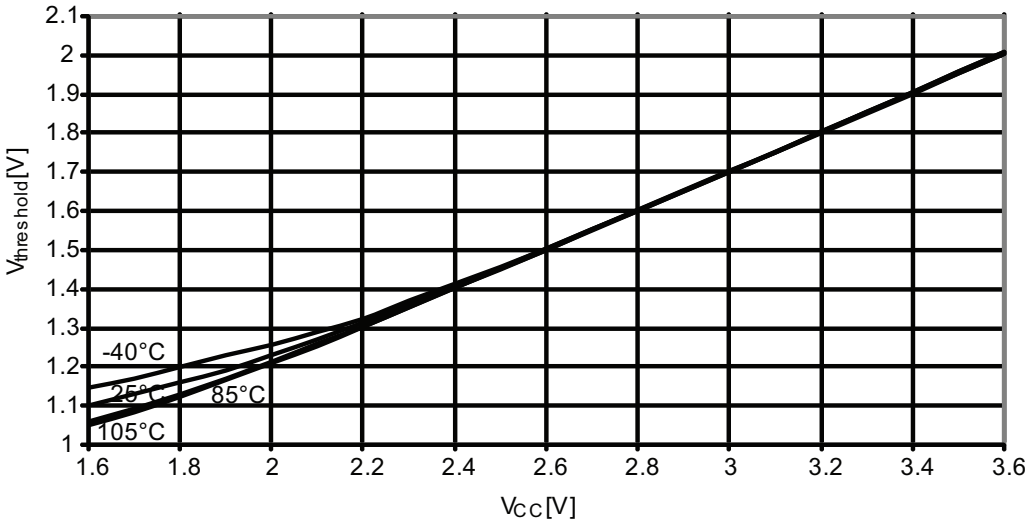


Figure 37-315. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".

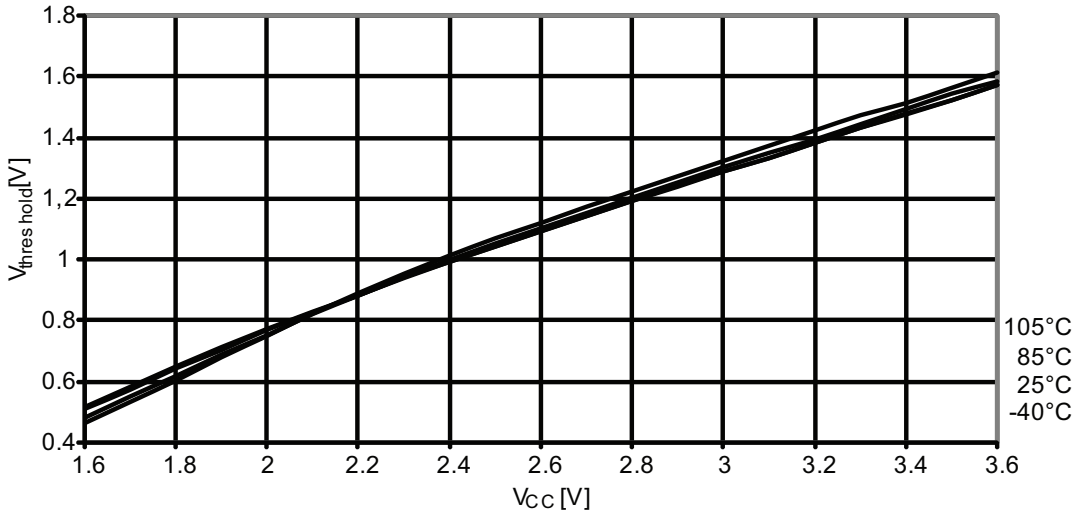


Table of Contents