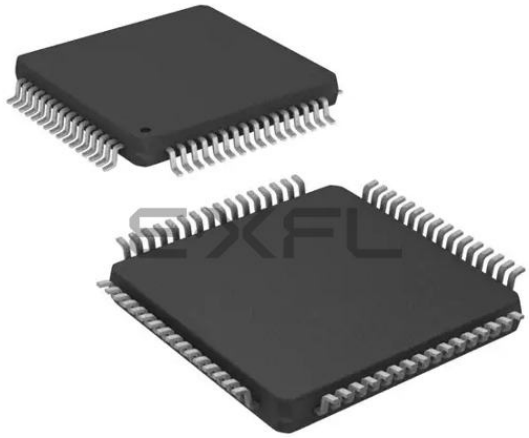

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3u-anr

17. TC2 - Timer/Counter Type 2

17.1 Features

- Eight eight-bit timer/counters
  - Four Low-byte timer/counter
  - Four High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

17.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2), TCD2, TCE2 and TCF2, respectively.

18. AWeX – Advanced Waveform Extension

18.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

18.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

24. USART

24.1 Features

- Seven identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multidevice bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

24.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

36.3.3 Current consumption

Table 36-68. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		260		
			V_{CC} = 3.0V		600		
		2MHz, Ext. Clk	V_{CC} = 1.8V		510	600	
			V_{CC} = 3.0V		1.1	1.5	mA
		32MHz, Ext. Clk			10.6	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		150		
		2MHz, Ext. Clk	V_{CC} = 1.8V		150	350	
			V_{CC} = 3.0V		290	600	
		32MHz, Ext. Clk			4.7	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.8	5.0	
		T = 105°C			6.5	17	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			3.1	7.0	
		WDT and Sampled BOD enabled, T = 105°C			7.3	20	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		250		µA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

36.4 ATxmega256A3U

36.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-97. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-98. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		1.60		3.6	V
AV_{CC}	Analog Supply Voltage		1.60		3.6	V
T_A	Temperature range	85 °C	-40		85	°C
		105 °C	-40		105	
T_j	Junction temperature	85°C	-40		105	°C
		105°C	-40		125	

Table 36-99. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset Error, input referred	1x gain, normal mode			-2		mV
		8x gain, normal mode			-5		
		64x gain, normal mode			-4		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.4.7 DAC Characteristics

Table 36-108. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7		pF
	Minimum Resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-109. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode	0		500	

Figure 37-76. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

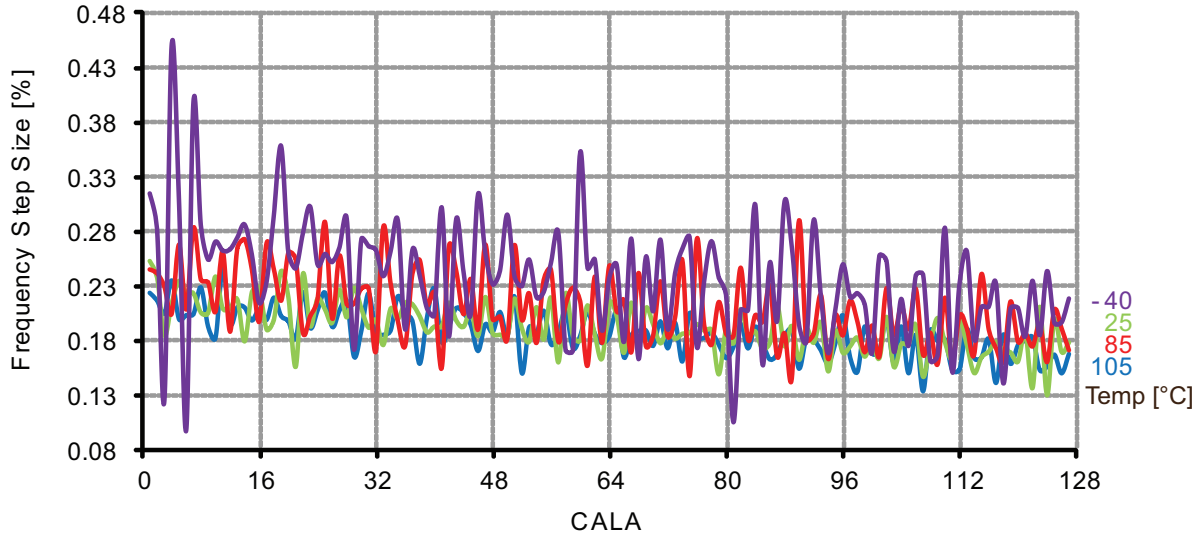


Figure 37-77. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.

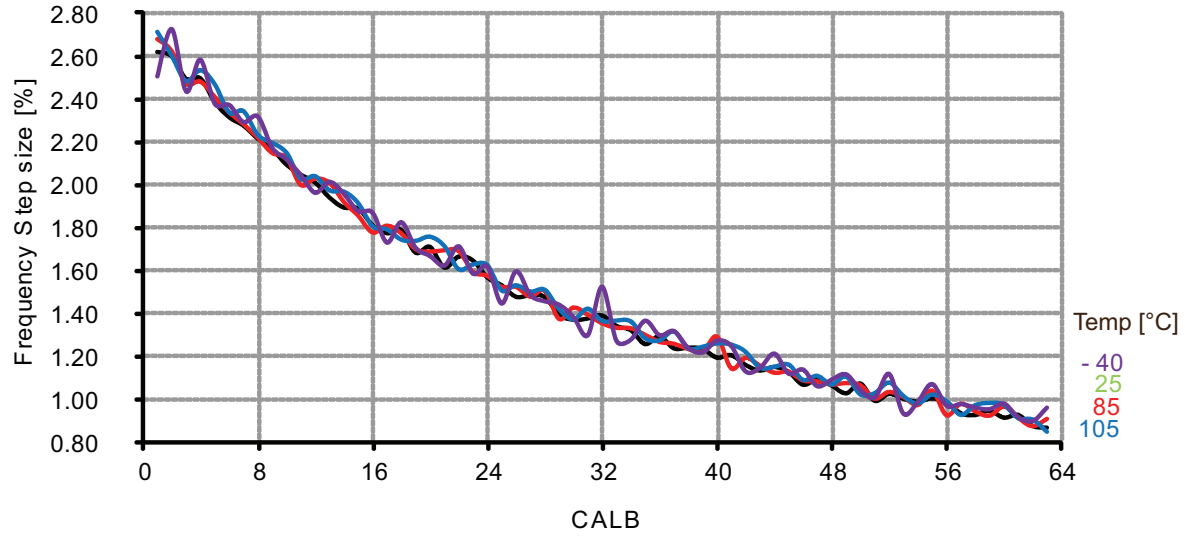


Figure 37-124. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

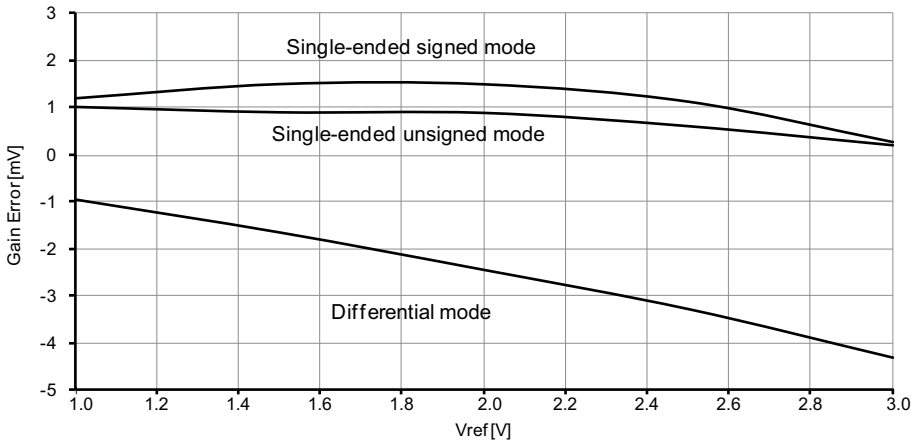


Figure 37-125. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

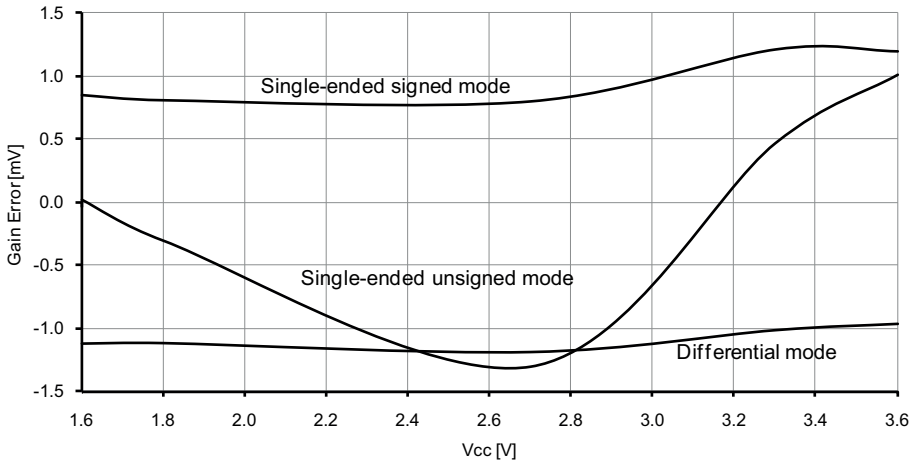
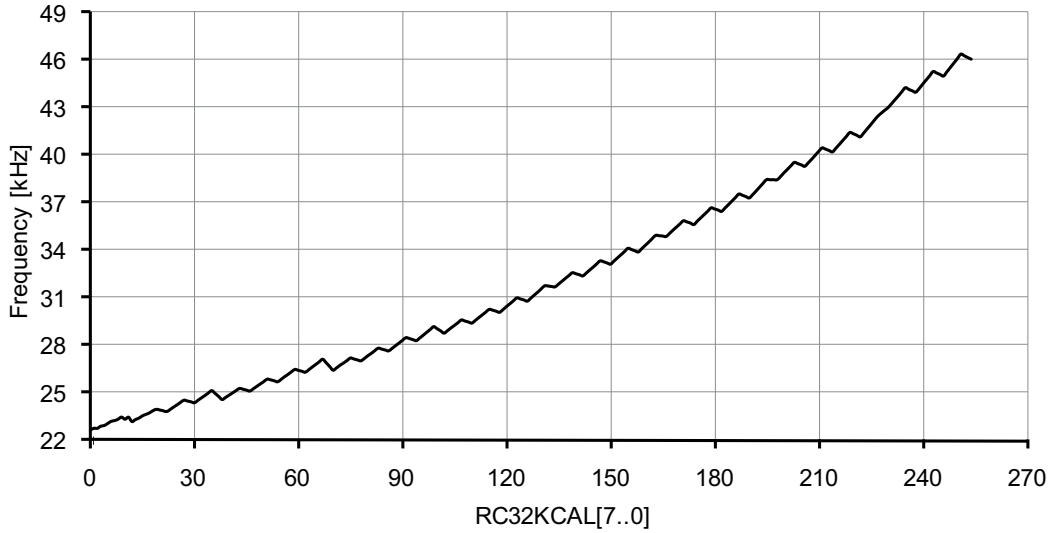


Figure 37-153. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.2.10.3 2MHz Internal Oscillator

Figure 37-154. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

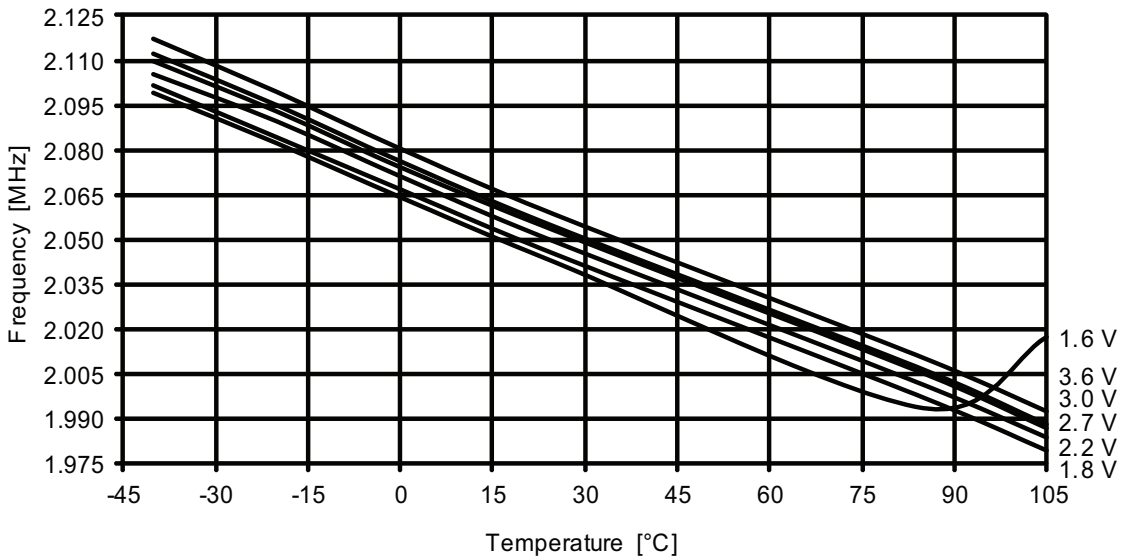


Figure 37-169. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

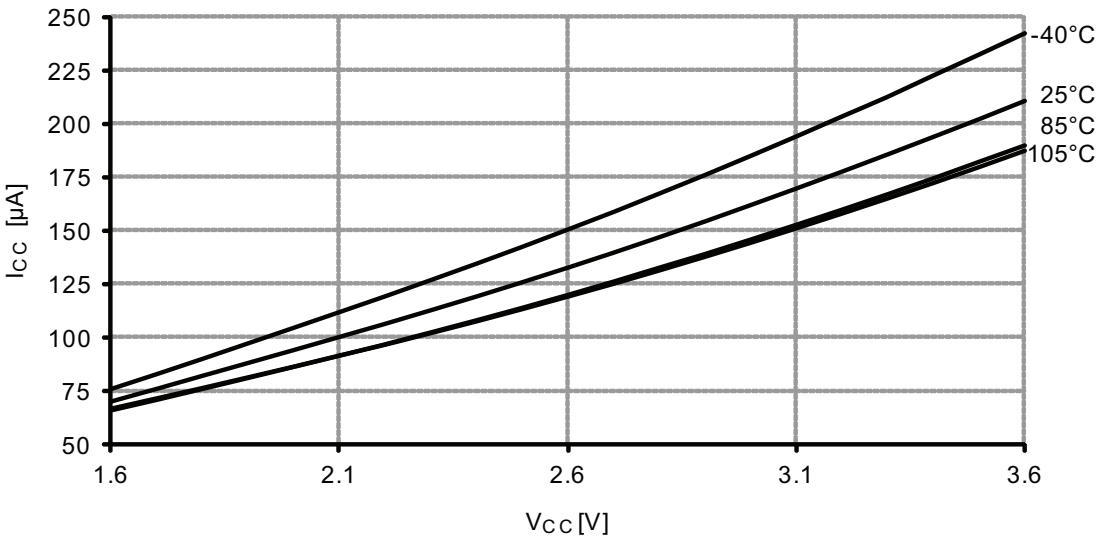


Figure 37-170. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

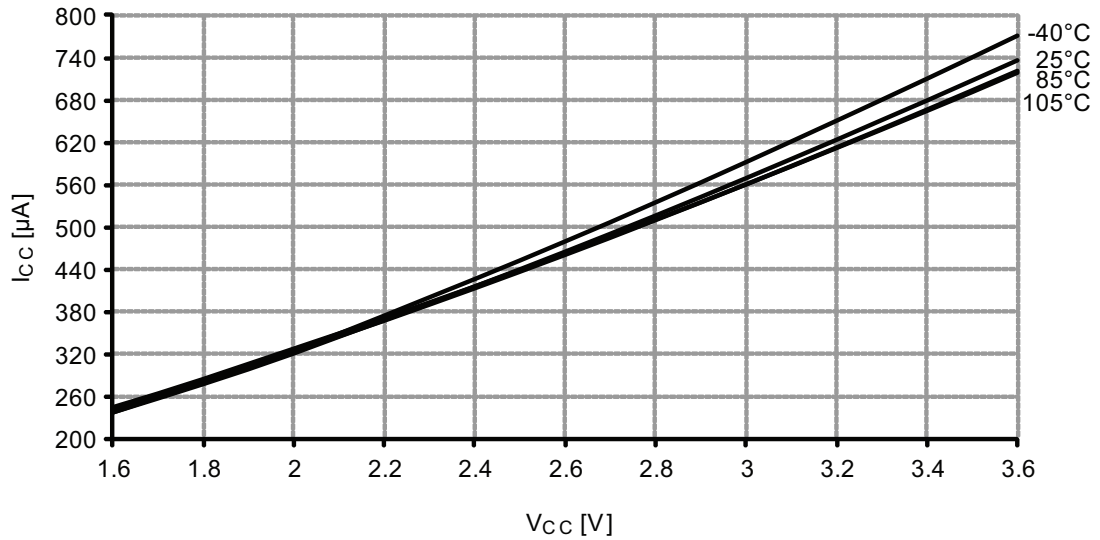


Figure 37-199. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

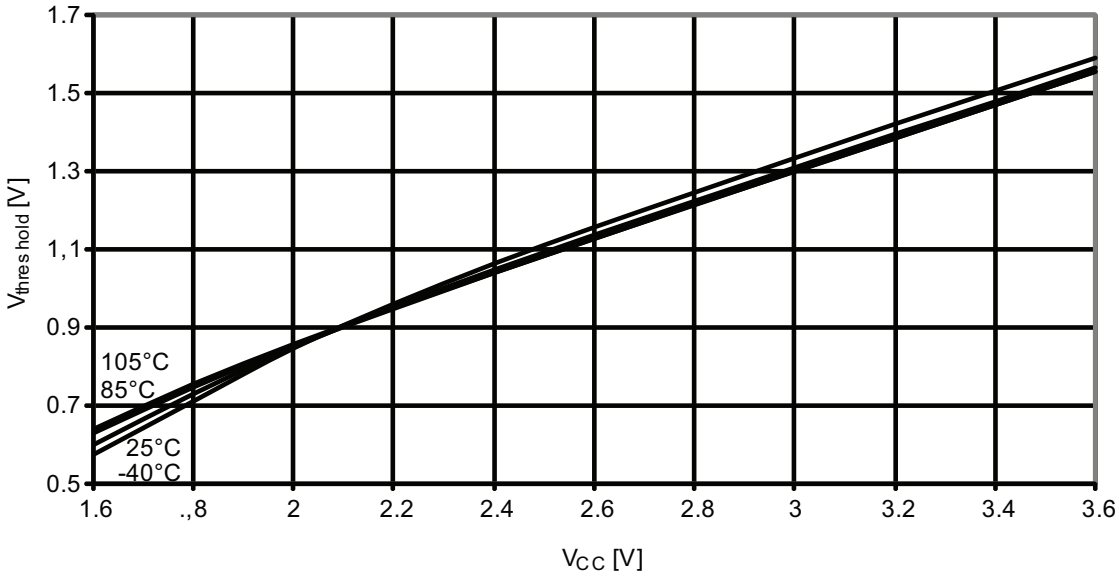


Figure 37-200. I/O pin input hysteresis vs. V_{CC} .

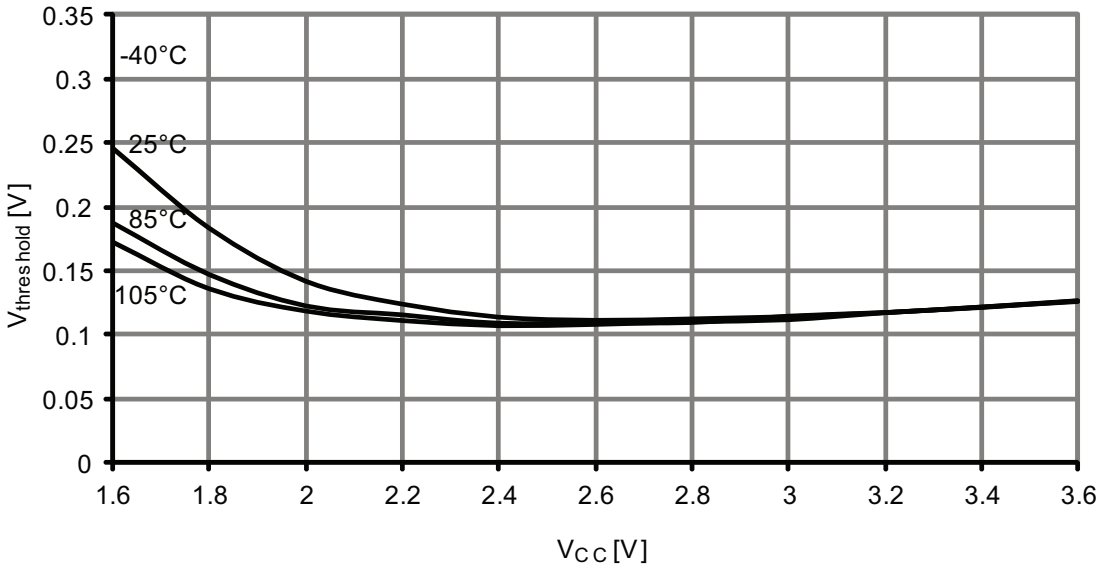


Figure 37-209. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

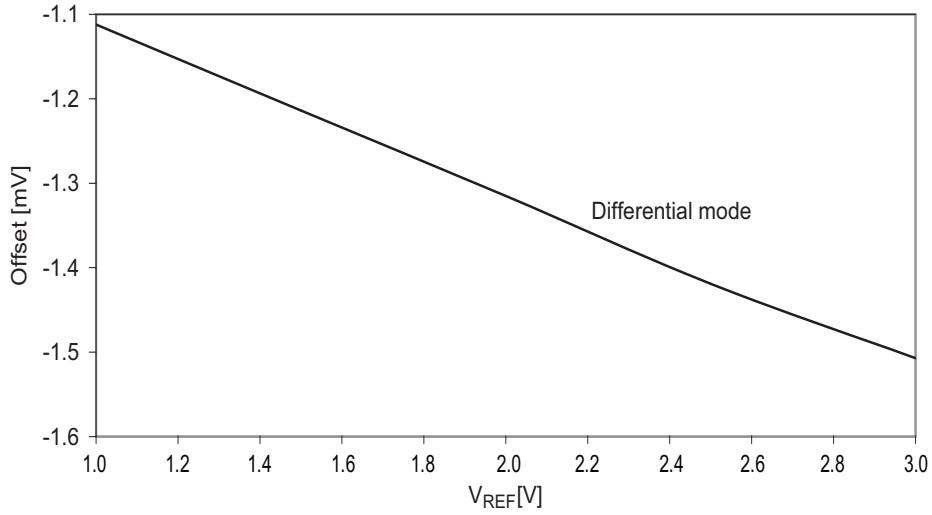


Figure 37-210. Gain error vs. temperature.

V_{CC} = 2.7V, V_{REF} = external 1.0V .

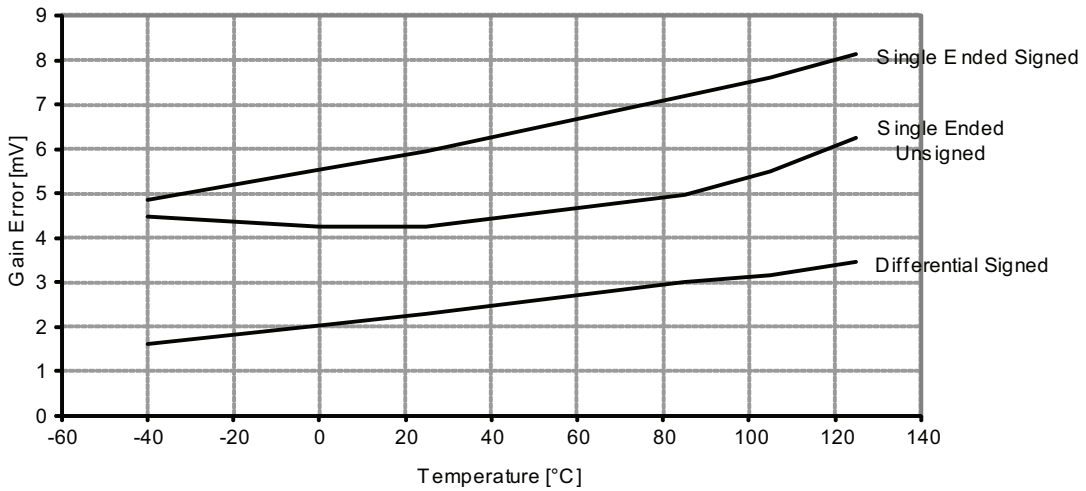
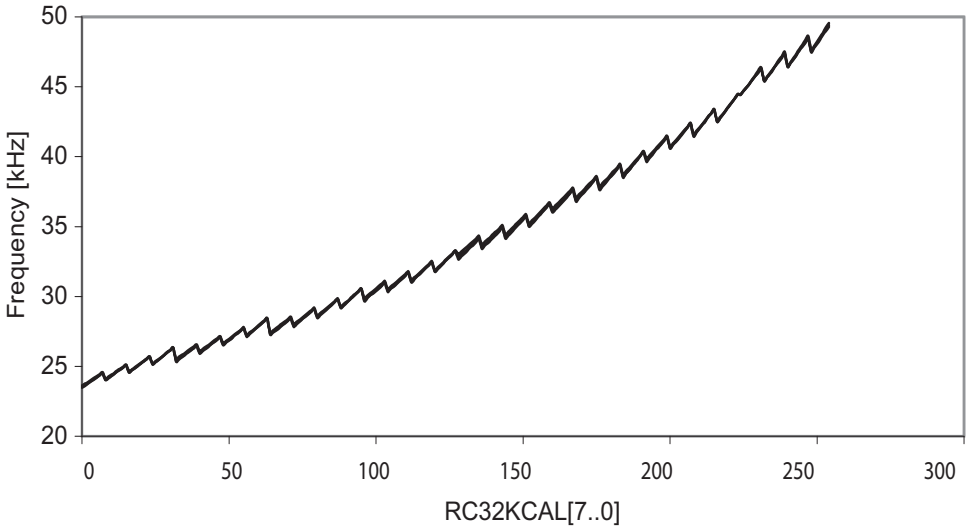


Figure 37-236. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.3.10.3 2MHz Internal Oscillator

Figure 37-237. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

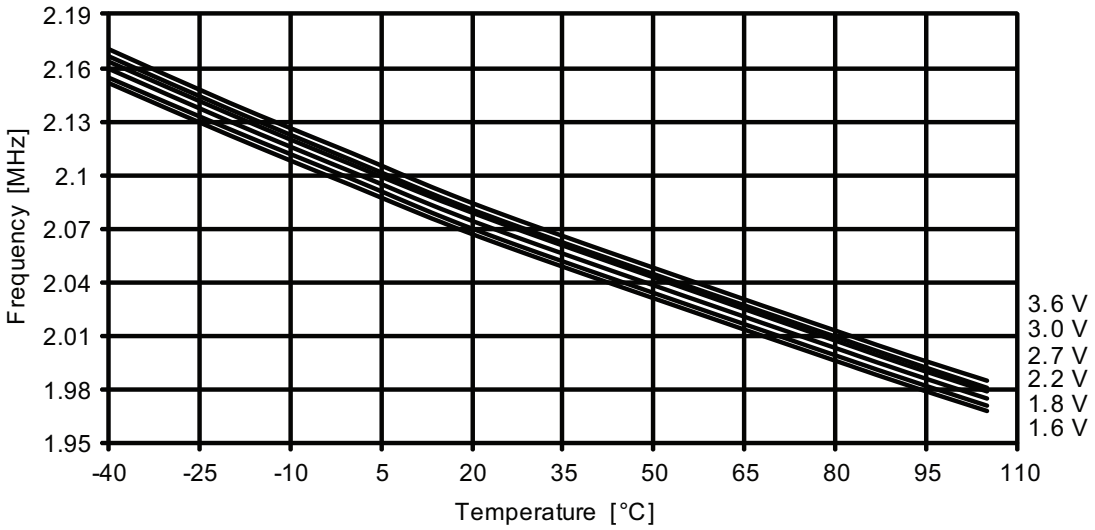


Figure 37-238. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

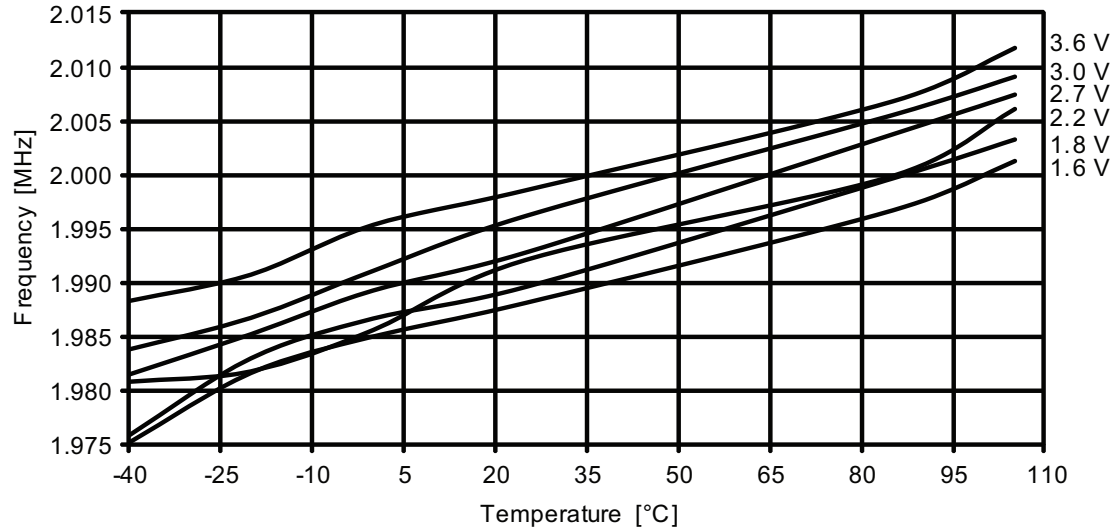
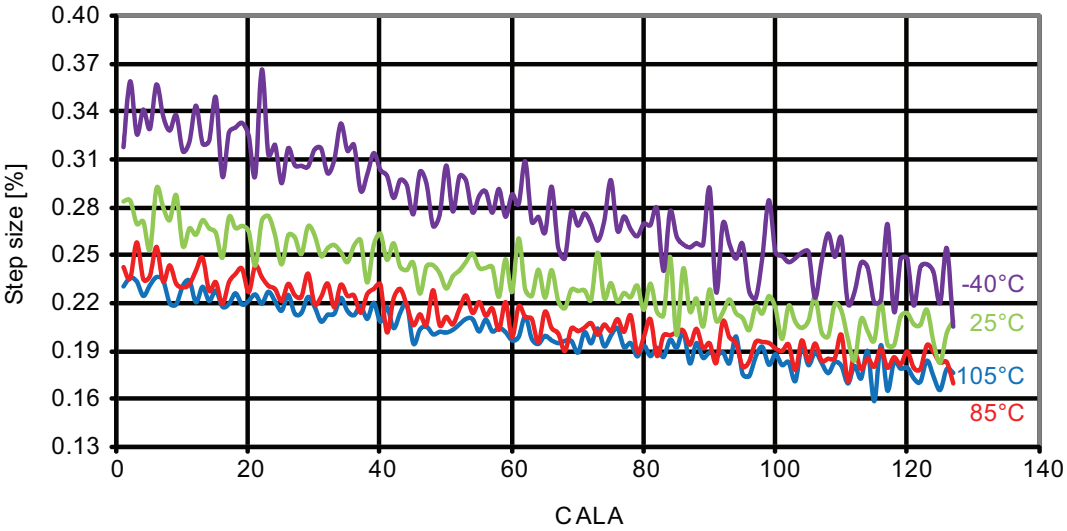


Figure 37-239. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.



37.3.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-244. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

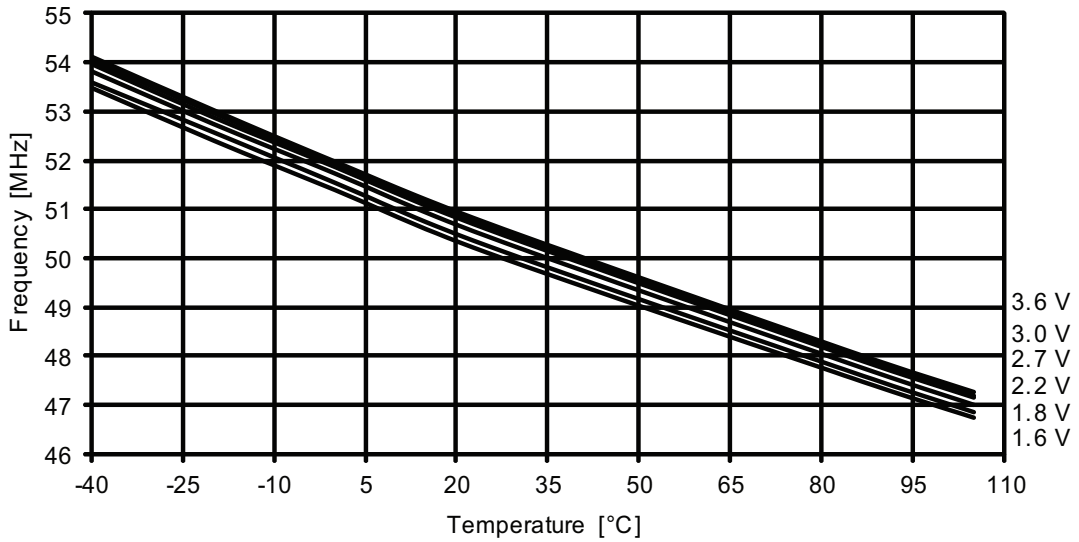


Figure 37-245. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

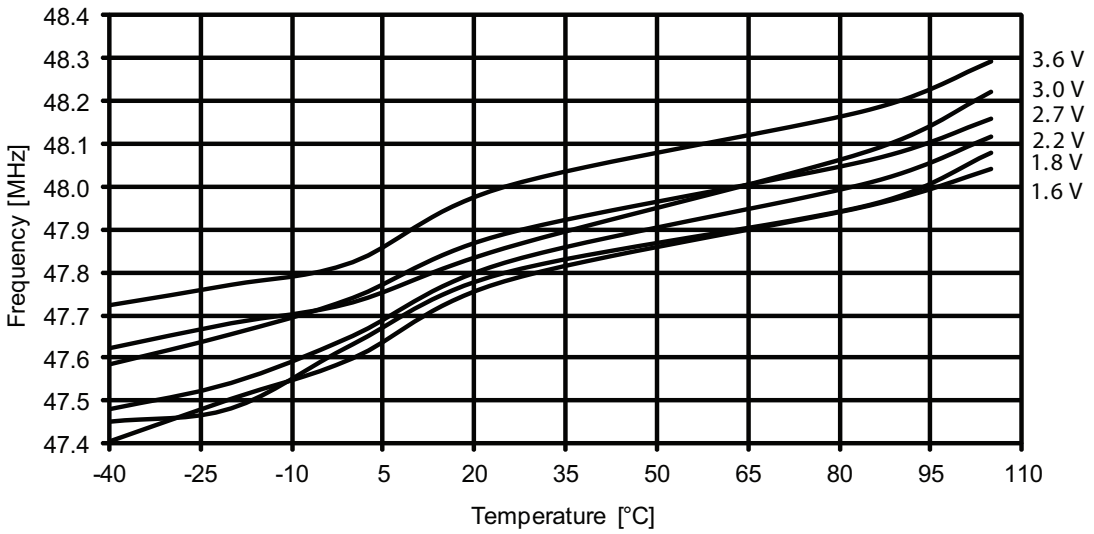
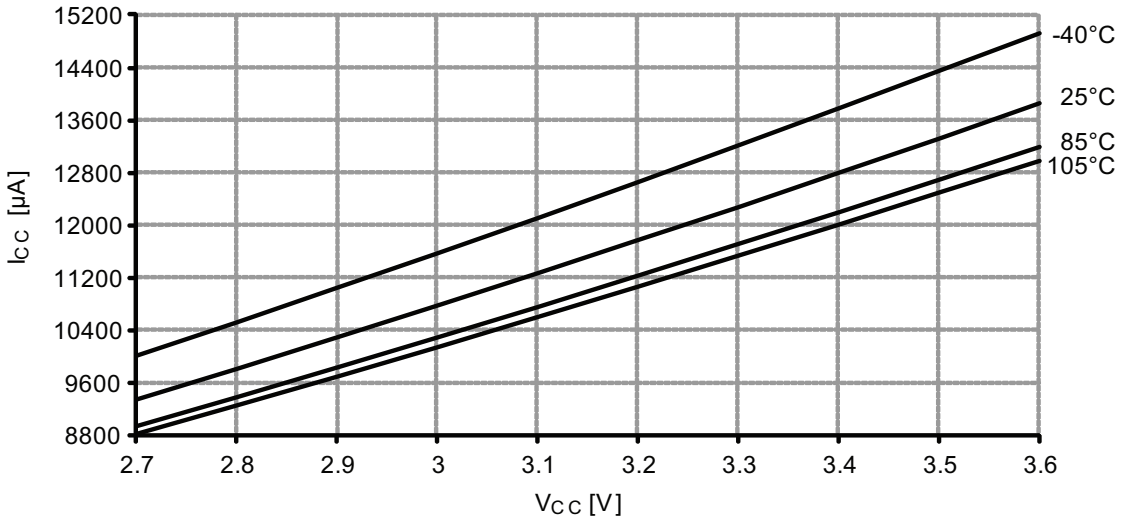


Figure 37-256. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.2 Idle mode supply current

Figure 37-257. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

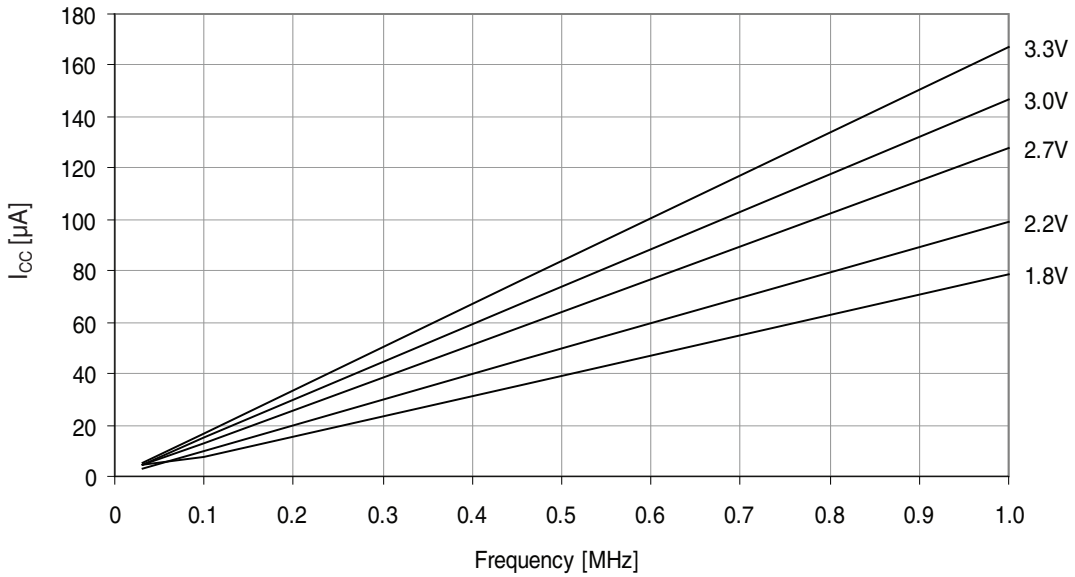


Figure 37-270. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

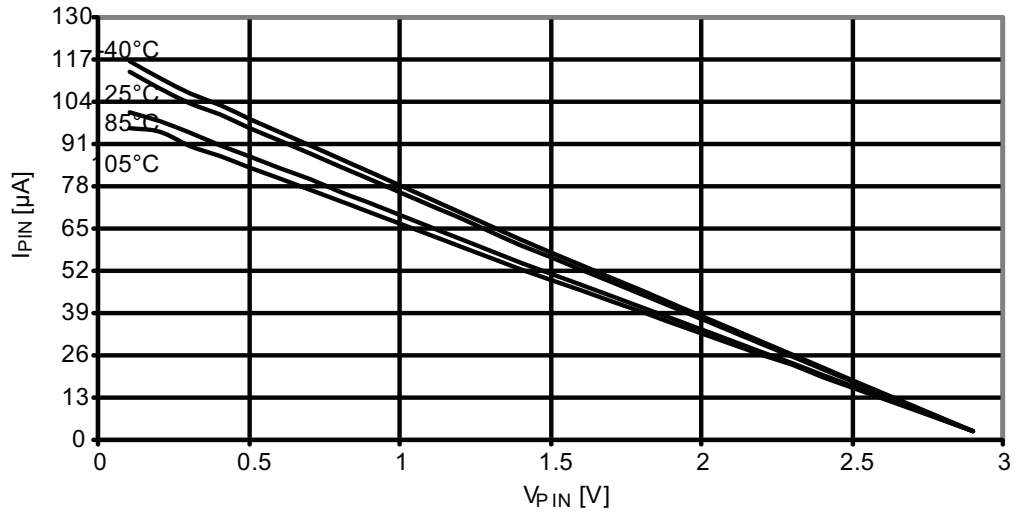
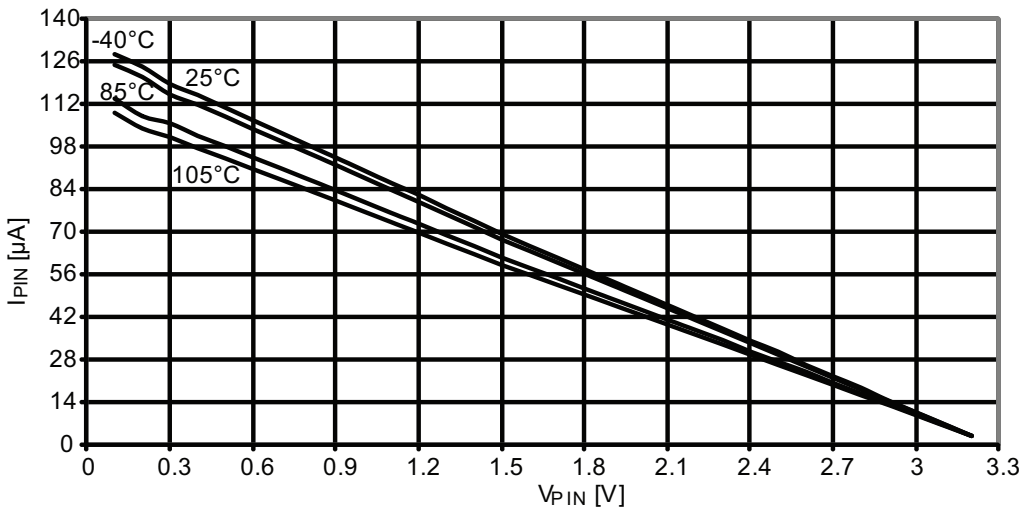


Figure 37-271. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.4.2.2 Output Voltage vs. Sink/Source Current

Figure 37-272. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

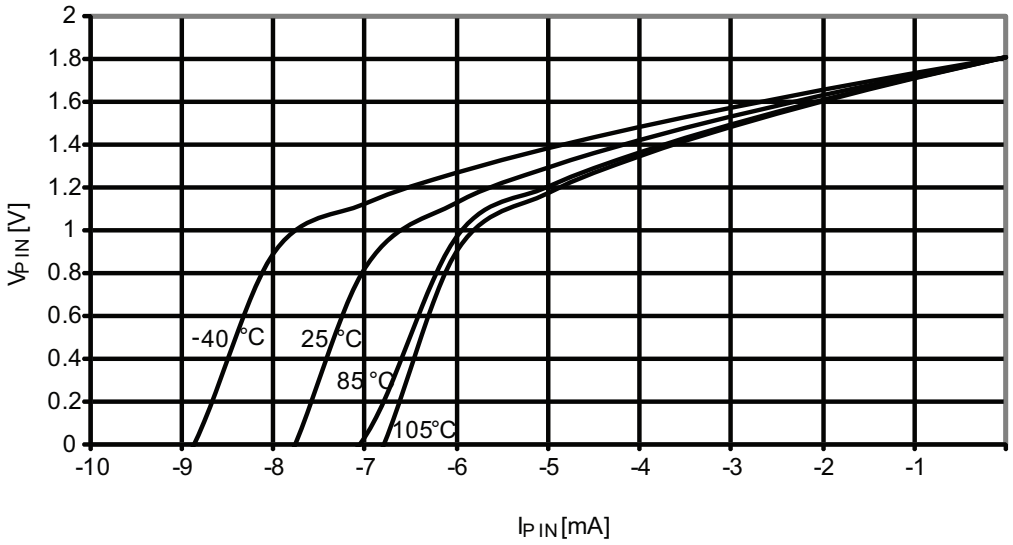


Figure 37-273. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

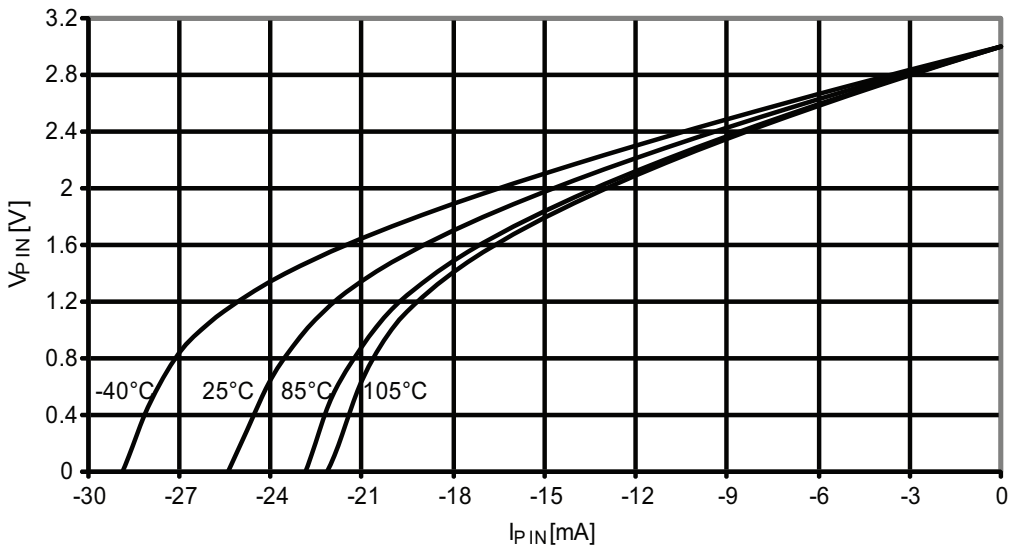


Figure 37-298. DNL error vs. V_{REF}.

$T = 25°C$, $V_{CC} = 3.6V$.

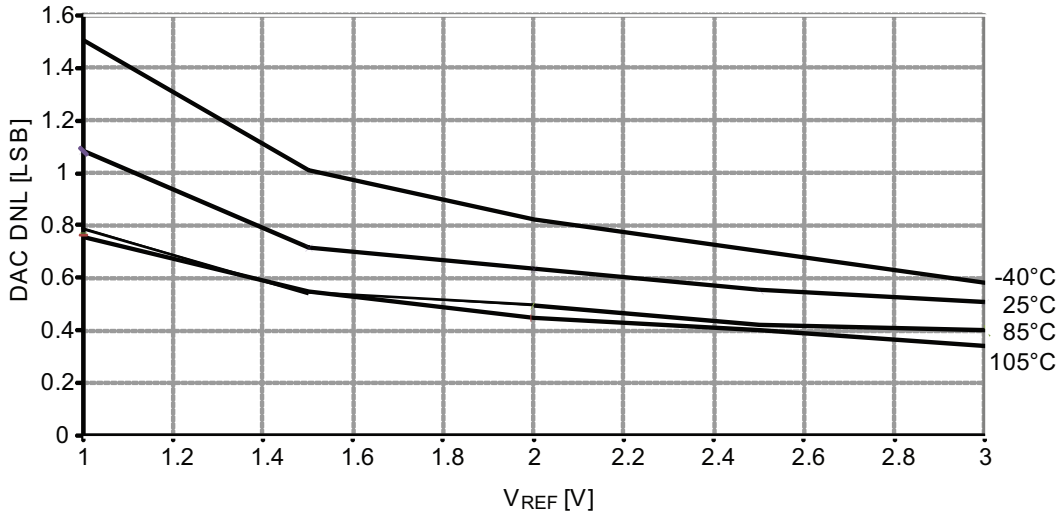
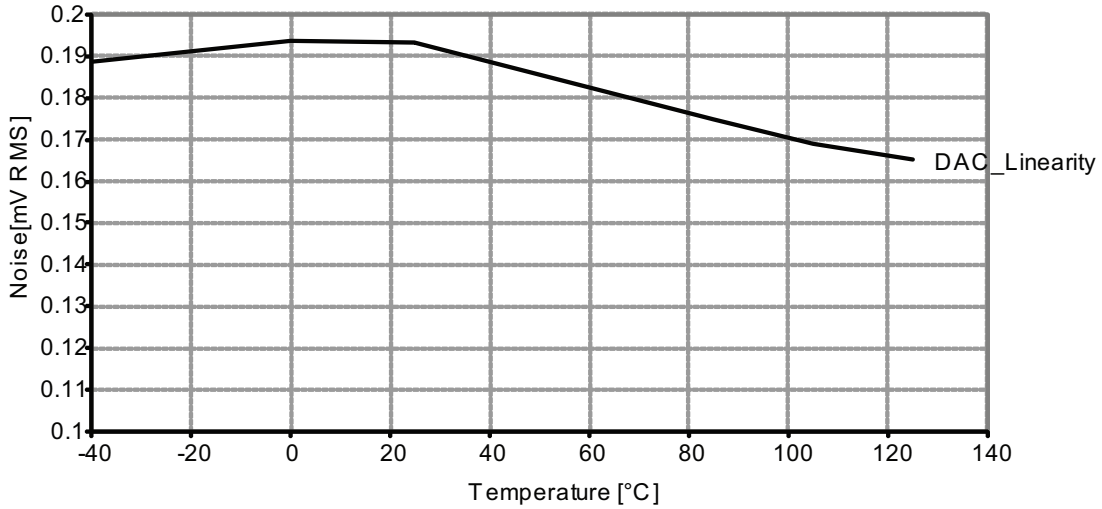


Figure 37-299. DAC noise vs. temperature.

$V_{CC} = 3.0V$, $V_{REF} = 2.4V$.



37.4.10.4 32MHz Internal Oscillator

Figure 37-323. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

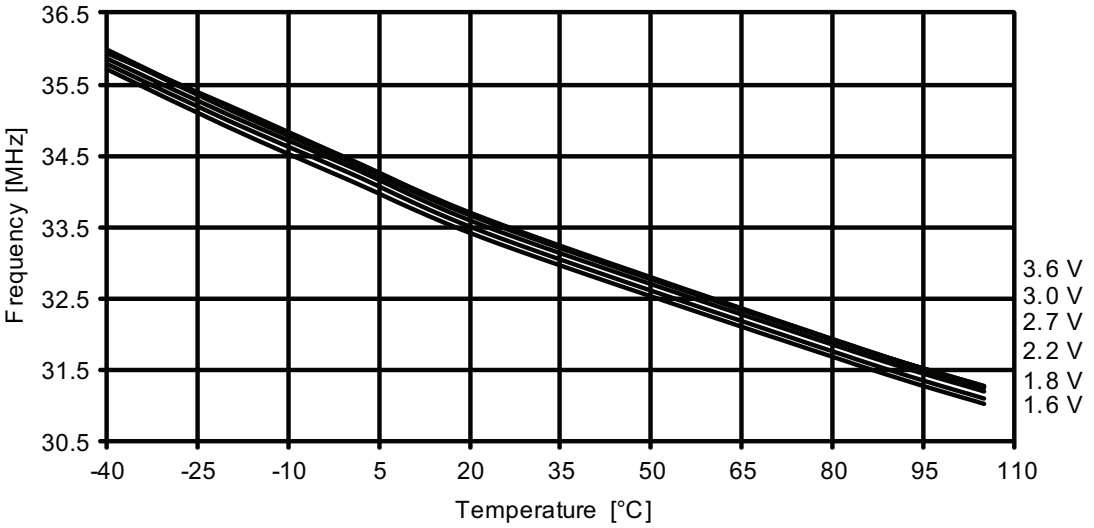


Figure 37-324. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.