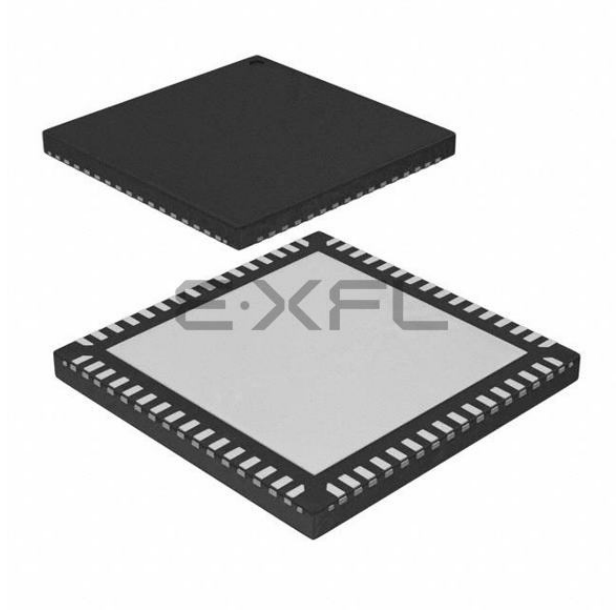

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3u-mh

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Table 7-1. Flash Program Memory (Hexadecimal address).

Word Address				
ATxmega256A3U	ATxmega192A3U	ATxmega128A3U	ATxmega64A3U	
0	0	0	0	Application Section (256K/192K/128K/64K)
				...
1EFFF /	16FFF /	37FF /	77FF	
1F000 /	17000 /	EFFF /	7800	Application Table Section (8K/8K/8K/4K)
1FFFF /	17FFF /	F000 /	7FFF	
20000 /	18000 /	10000 /	8000	Boot Section (8K/8K/8K/4K)
20FFF /	18FFF /	10FFF /	87FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read and DMA controller write, etc.) can access different memory sections at the same time.

7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.11 JTAG Disable

It is possible to disable the JTAG interface from the application software. This will prevent all external JTAG access to the device until the next device reset or until JTAG is enabled again from the application software. As long as JTAG is disabled, the I/O pins required for JTAG can be used as normal I/O pins.

7.12 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.13 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-4 on page 17 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-4. Number of words and pages in the flash.

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega64A3U	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128A3U	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16
ATxmega192A3U	17	192K + 8K	256	Z[8:1]	Z[17:9]	192K	384	8K	16
ATxmega256A3U	18	256K + 8K	256	Z[8:1]	Z[18:9]	256K	512	8K	16

Table 7-5 on page 18 shows EEPROM memory organization for the Atmel AVR XMEGA A3U devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU or DMA controller can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

26. AES and DES Crypto Engine

26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

30. AC – Analog Comparator

30.1 Features

- Four Analog Comparators (AC)
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

30.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

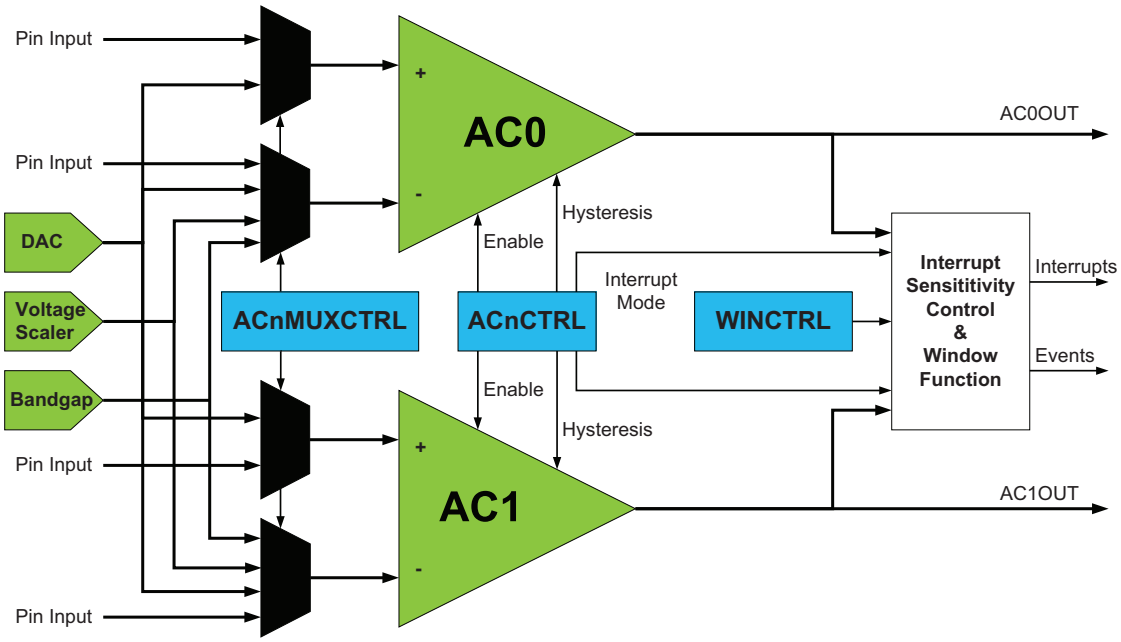
The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

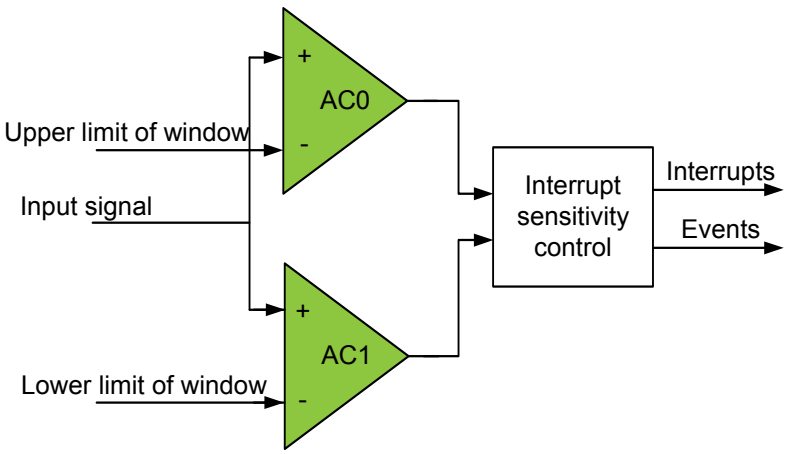
PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

Figure 30-1. Analog comparator overview.



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 30-2.

Figure 30-2. Analog comparator window function.



36. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

Note: For devices that are not available yet, preliminary values in this datasheet are based on simulations, and/or characterization of similar AVR XMEGA microcontrollers. After the device is characterized the final values will be available, hence existing values can change. Missing minimum and maximum values will be available after the device is characterized.

36.1 ATxmega64A3U

36.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-1. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-2. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		1.60		3.6	V
AV_{CC}	Analog Supply Voltage		1.60		3.6	V
T_A	Temperature range	85 °C	-40		85	°C
		105 °C	-40		105	
T_j	Junction temperature	85°C	-40		105	°C
		105°C	-40		125	

36.1.3 Current consumption

Table 36-4. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		125		
		1MHz, Ext. Clk	V_{CC} = 1.8V		250		
			V_{CC} = 3.0V		520		
		2MHz, Ext. Clk	V_{CC} = 1.8V		450	550	
			V_{CC} = 3.0V		0.9	1.4	mA
		32MHz, Ext. Clk			9.5	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.0		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		75		
			V_{CC} = 3.0V		140		
		2MHz, Ext. Clk	V_{CC} = 1.8V		145	250	
			V_{CC} = 3.0V		275	450	
		32MHz, Ext. Clk			4.4	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.6	5.0	
		T = 105°C			1.6	7	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			2.5	7.0	
		WDT and Sampled BOD enabled, T = 105°C			2.5	8	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		150		µA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 36-5. Current consumption for modules and peripherals.

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				26		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		µA
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			220		µA
	Watchdog Timer				1		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				100		µA
	Temperature sensor				95		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low Power mode		1.1		
	AC	High Speed Mode			330		µA
		Low Power Mode			130		
	DMA	615KBps between I/O registers and SRAM			115		µA
	Timer/Counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				4		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Table 36-14. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input Resolution					12	Bits
INL (1)	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4	
			V_{CC} = 3.6V		±1.5	±4	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL (1)	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3	lsb
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4		lsb
	Gain calibration step size				4		lsb
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

36.1.8 Analog Comparator Characteristics

Table 36-15. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input Offset Voltage			<±10		mV
I_{lk}	Input Leakage Current			<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, None			0		mV
V_{hys2}	Hysteresis, Small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, Large	mode = HS		30		mV
		mode = LP		60		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance (1)	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = Safety factor				$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.2		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				6.8		pF
C_{LOAD}	Parasitic capacitance load				2.95		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

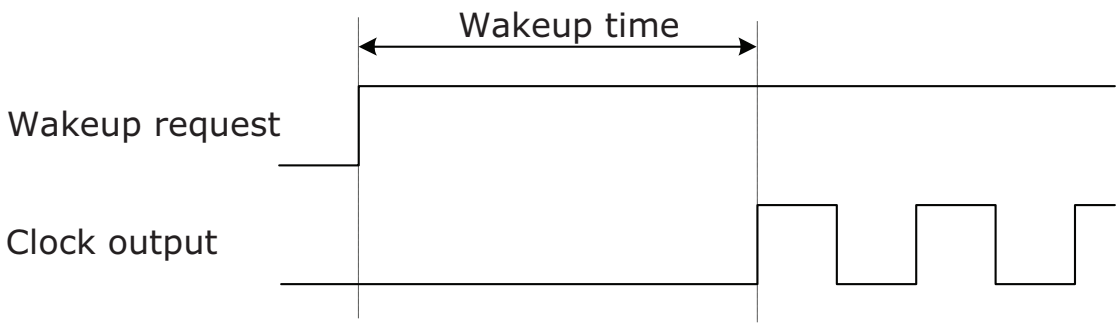
36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.



36.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-56. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.2.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-57. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

36.2.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-58. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

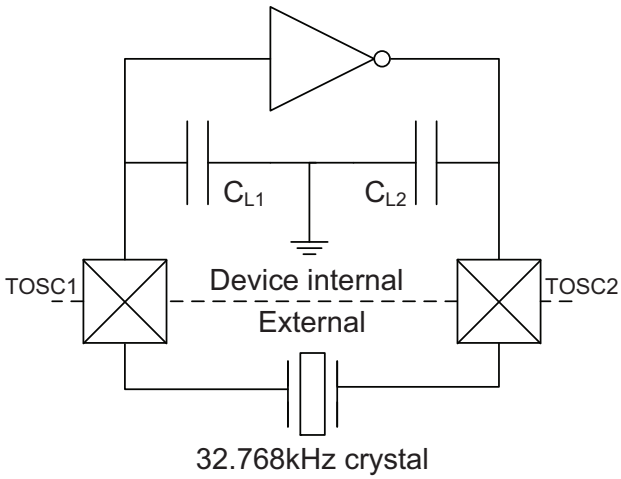
36.2.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-62. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			4.2		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			4.3		pF
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-4 for definition.

Figure 36-11. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

36.4.3 Current consumption

Table 36-100. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		280		
			V_{CC} = 3.0V		600		
		2MHz, Ext. Clk	V_{CC} = 1.8V		510	500	
			V_{CC} = 3.0V		1.1	1.5	mA
		32MHz, Ext. Clk			10.6	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		150		
		2MHz, Ext. Clk	V_{CC} = 1.8V		150	350	
			V_{CC} = 3.0V		290	600	
		32MHz, Ext. Clk			4.7	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.8	5.0	
		T = 105°C			6.5	17	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			3.1	7.0	
		WDT and Sampled BOD enabled, T = 105°C			7.3	20	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		250		µA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Figure 37-29. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

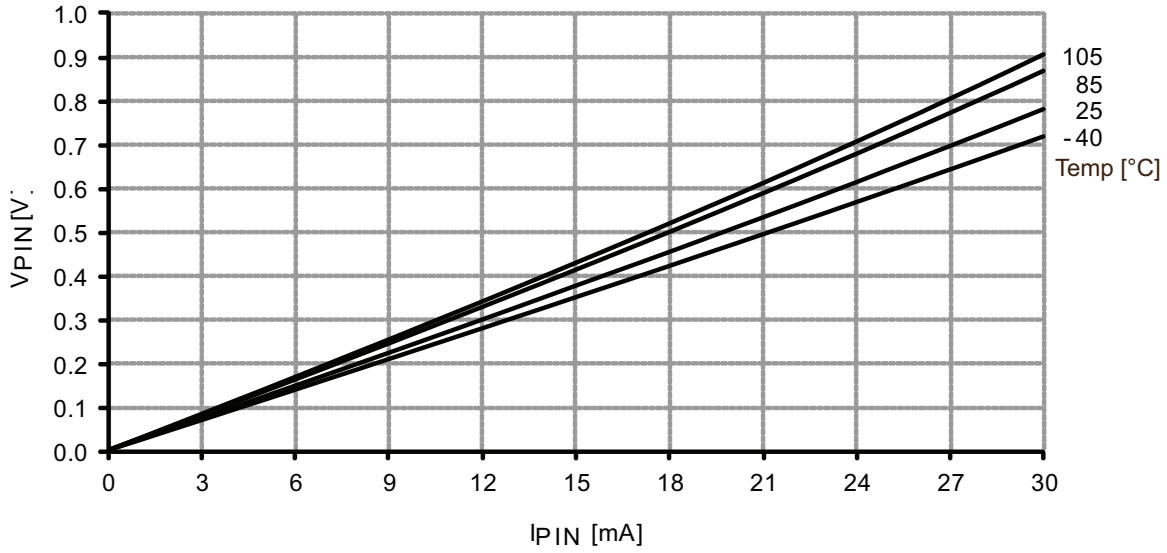
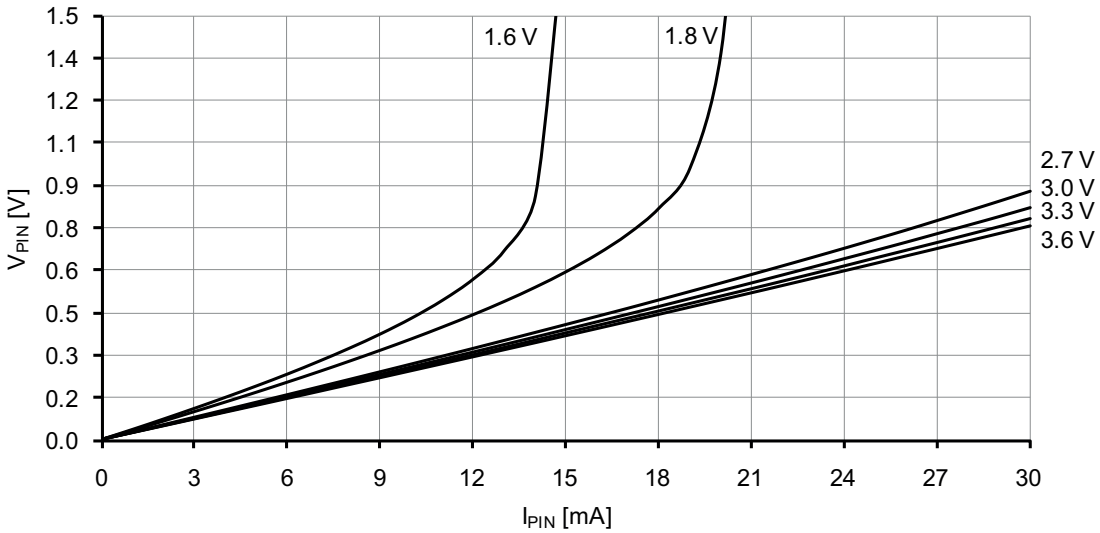


Figure 37-30. I/O pin output voltage vs. sink current.



37.2.10.4 32MHz Internal Oscillator

Figure 37-157. 32MHz internal oscillator frequency vs. temperature.

DFLL disabled.

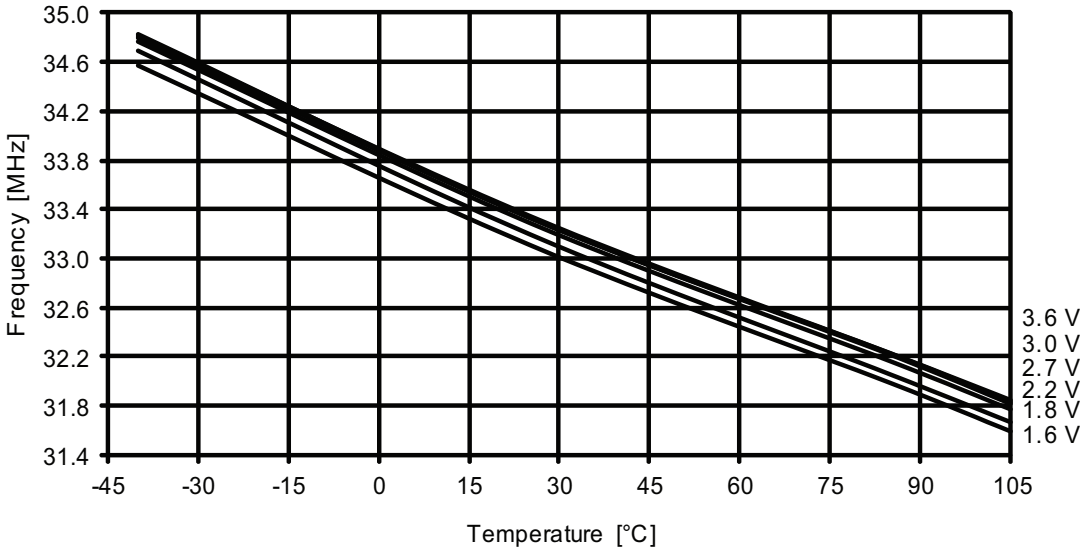
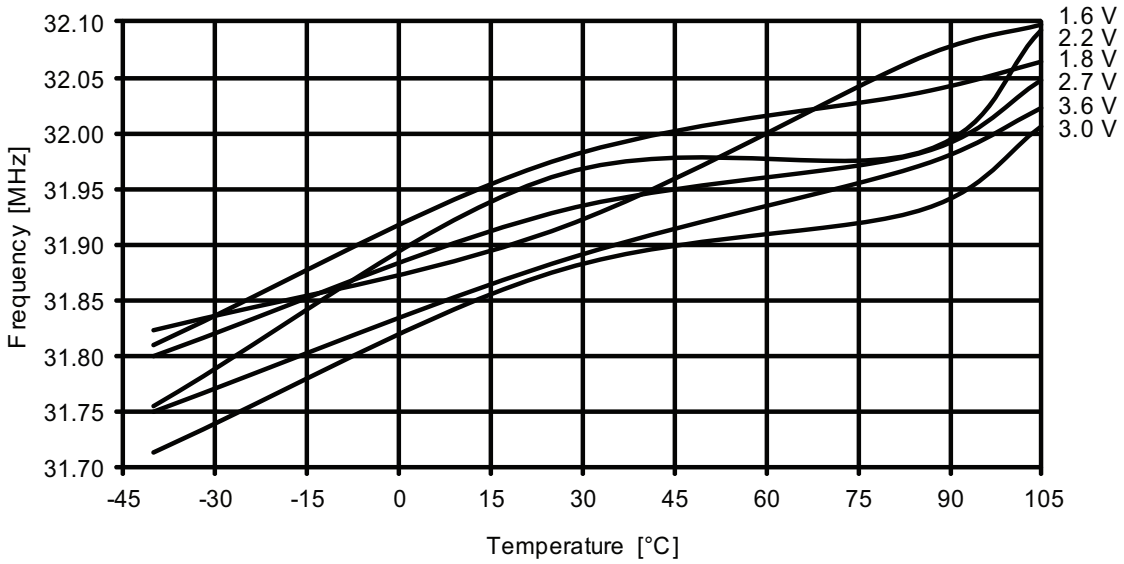


Figure 37-158. 32MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.



38. Errata

38.1 ATxmega64A3U, ATxmega128A3U, ATxmega192A3U, ATxmega256A3U

38.1.1 Rev. G

- The DAC Channel 1 has not been calibrated in the Xmega devices released prior to April 2012.
- AWeX fault protection restore is not done correct in Pattern Generation Mode.

1. **AWeX fault protection restore is not done correct in Pattern Generation Mode**
   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

   Problem fix/Workaround
   Problem fix/Workaround

   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

   For PGM in cycle-by-cycle mode there is no workaround.

38.1.2 Rev. A-F

Not sampled.

39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8386E – 09/2014

1.	Updated "Ordering Information" on page 3: – Added Ordering information for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
	– Updated "Electrical Characteristics" on page 73 and onwards concerning "Power Consumption" and "Endurance and data retention" for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
2.	– Updated "Typical Characteristics" on page 161 and onwards for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
3.	– Corrected values for Active Current Consumption for 192A3U in Table 36-68 on page 119 and for 256A3U in Table 36-100 on page 141.
4	– Updated plots for Active supply current for 192A3U in Figure 37-167 on page 245 and Figure 37-168 on page 245
5	– Updated plots for Active supply current for 256A3U in Figure 37-251 on page 287 and Figure 37-252 on page 288
6.	– Corrected values for Bootloader start and end address for 128A3U in Table 7-1 on page 14.
7.	– Changed Vcc to AVcc in Section 28. "ADC – 12-bit Analog to Digital Converter" on page 52and in Section 30.1 "Features" on page 56.
8.	– Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 93, Table 36-64 on page 115, Table 36-96 on page 137 and Table 36-128 on page 159.
9.	– Added information in Section 38. "Errata" on page 329 on missing calibration of DAC channel 1.

39.2 8386D – 03/2014

1.	Updated "Port A - alternate functions." on page 61: – Removed ACDP POS from the Table 32-1 on page 61
2.	Updated "Port B - alternate functions." on page 61: – ACDB POS changed to ADCB POS/GAINPOS in the Table 32-2 on page 61

39.3 8386C – 02/2013

1.	Updated the datasheet using the Atmel new datasheet template.
2.	Added column for TWI with external driver interface for Port C and E in "Alternate Pin Functions" on page 61.
3.	Removed TWID from Port D and updated pin numbers in"Alternate Pin Functions" on page 61.
4.	Added TOSC and removed AWEXE to/from Port E in "Alternate Pin Functions" on page 61.
5.	Added notes to table for Port D and E in "Alternate Pin Functions" on page 61.