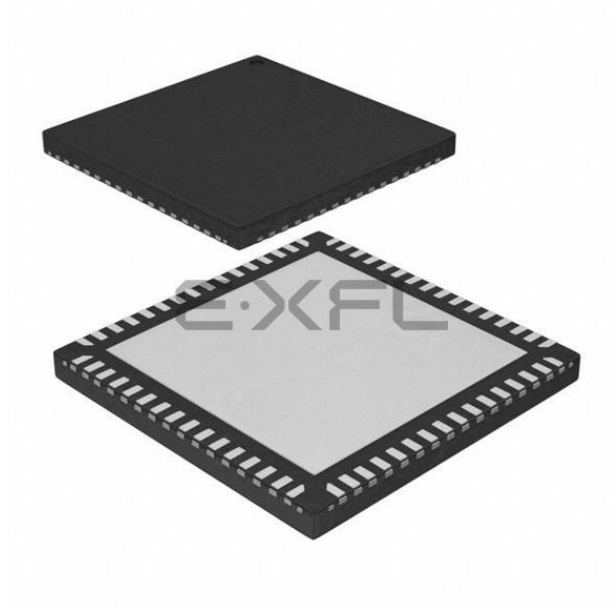

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3u-mhr

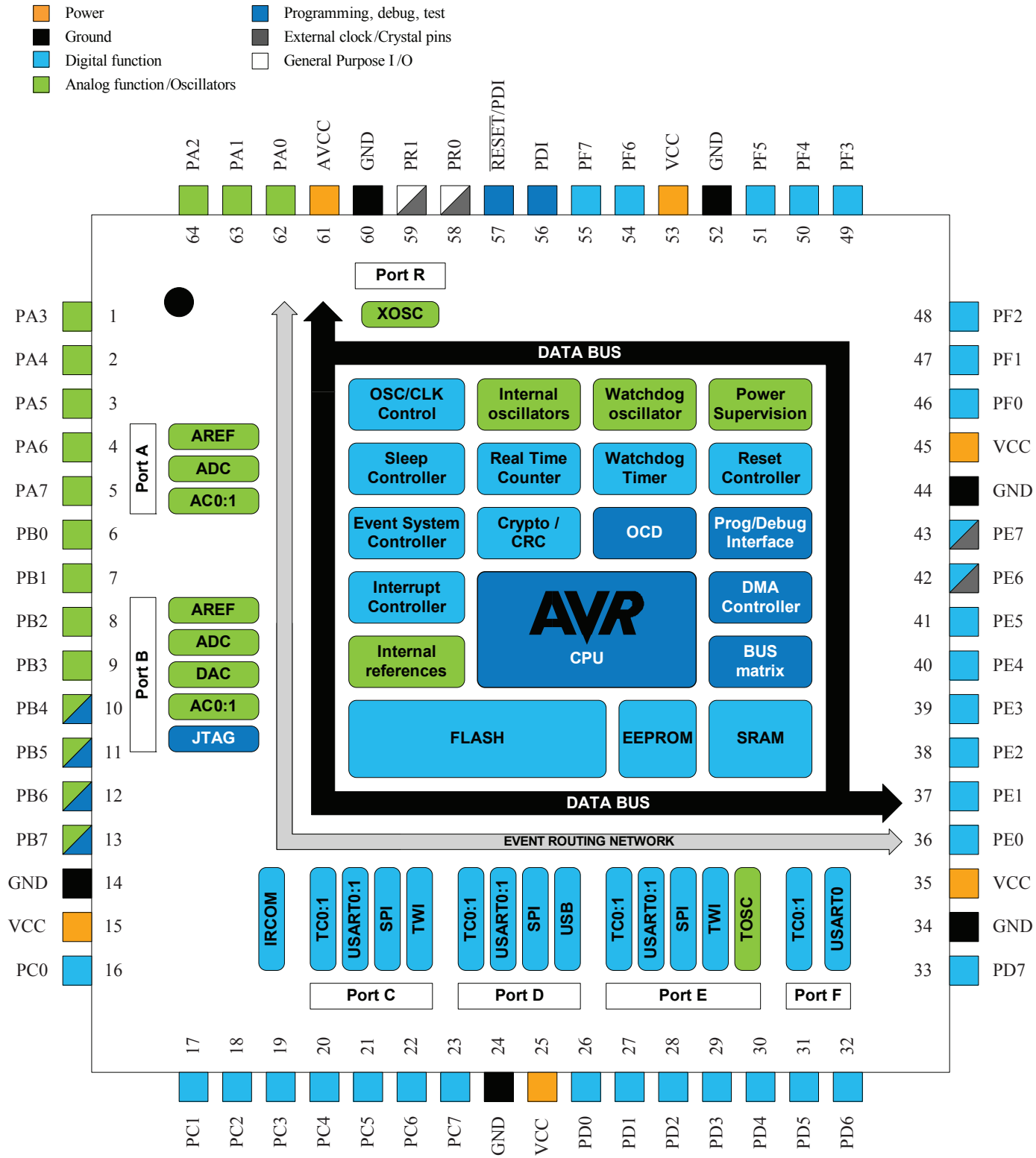
1. Ordering Information

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package (1)(2)(3)	Temp.
ATxmega256A3U-AU	256K + 8K	4K	16K	32	1.6 - 3.6V	64A	-40°C - 85°C
ATxmega256A3U-AUR(4)	256K + 8K	4K	16K				
ATxmega192A3U-AU	192K + 8K	2K	16K				
ATxmega192A3U-AUR(4)	192K + 8K	2K	16K				
ATxmega128A3U-AU	128K + 8K	2K	8K				
ATxmega128A3U-AUR(4)	128K + 8K	2K	8K				
ATxmega64A3U-AU	64K + 4K	2K	4K				
ATxmega64A3U-AUR(4)	64K + 4K	2K	4K				
ATxmega256A3U-MH	256K + 8K	4K	16K			64M2	
ATxmega256A3U-MHR(4)	256K + 8K	4K	16K				
ATxmega192A3U-MH	192K + 8K	2K	16K				
ATxmega192A3U-MHR(4)	192K + 8K	2K	16K				
ATxmega128A3U-MH	128K + 8K	2K	8K				
ATxmega128A3U-MHR(4)	128K + 8K	2K	8K				
ATxmega64A3U-MH	64K + 4K	2K	4K				
ATxmega64A3U-MHR(4)	64K + 4K	2K	4K				
ATxmega256A3U-AN	256K + 8K	4K	16K	32	1.6 - 3.6V	64A	-40°C - 105°C
ATxmega256A3U-ANR(4)	256K + 8K	4K	16K				
ATxmega192A3U-AN	192K + 8K	2K	16K				
ATxmega192A3U-ANR(4)	192K + 8K	2K	16K				
ATxmega128A3U-AN	128K + 8K	2K	8K				
ATxmega128A3U-ANR(4)	128K + 8K	2K	8K				
ATxmega64A3U-AN	64K + 4K	2K	4K				
ATxmega64A3U-ANR(4)	64K + 4K	2K	4K				
ATxmega256A3U-MN	256K + 8K	4K	16K			64M2	
ATxmega256A3U-MNR(4)	256K + 8K	4K	16K				
ATxmega192A3U-MN	192K + 8K	2K	16K				
ATxmega192A3U-MHR(4)	192K + 8K	2K	16K				
ATxmega128A3U-MN	128K + 8K	2K	8K				
ATxmega128A3U-MNR(4)	128K + 8K	2K	8K				
ATxmega64A3U-MN	64K + 4K	2K	4K				
ATxmega64A3U-MNR(4)	64K + 4K	2K	4K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

2. Pinout/Block Diagram

Figure 2-1. Block diagram and pinout.



Note: 1. For full details on pinout and alternate pin functions refer to "Pinout and Pin Functions" on page 59.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 73.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-2.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-2. Device ID bytes for Atmel AVR XMEGA A3U devices.

Device	Device ID bytes		
	Byte 2	**Byte 1**	**Byte 0**
ATxmega64A3U	42	96	1E
ATxmega128A3U	42	97	1E
ATxmega192A3U	44	97	1E
ATxmega256A3U	42	98	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Table 7-3 on page 16. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

that provides a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

10.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

10.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

10.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

10.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

10.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz. The production signature row contains 48MHz calibration values intended used when the oscillator is used a full-speed USB clock source.

10.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

10.3.8 PLL with 1x-31x Multiplication Factor

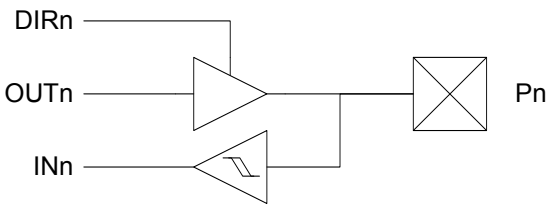
The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

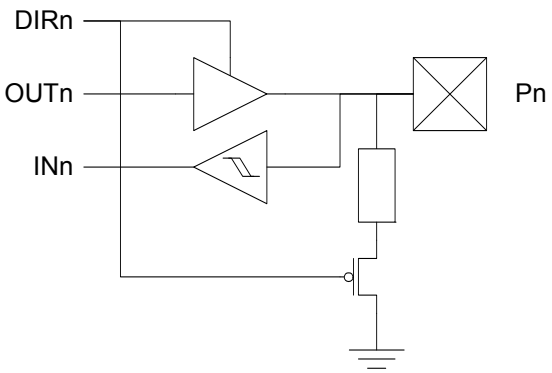
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole.



15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input).



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input).

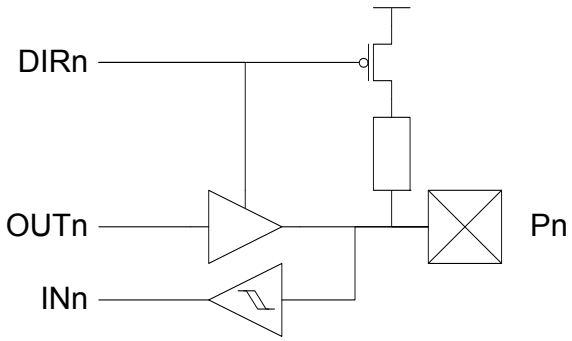
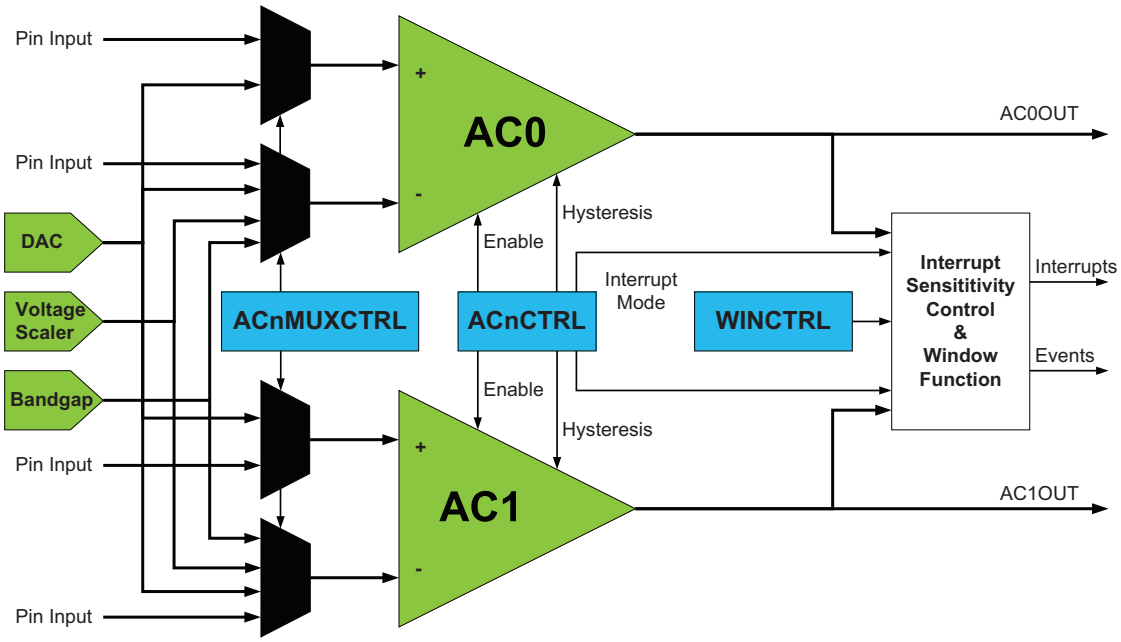
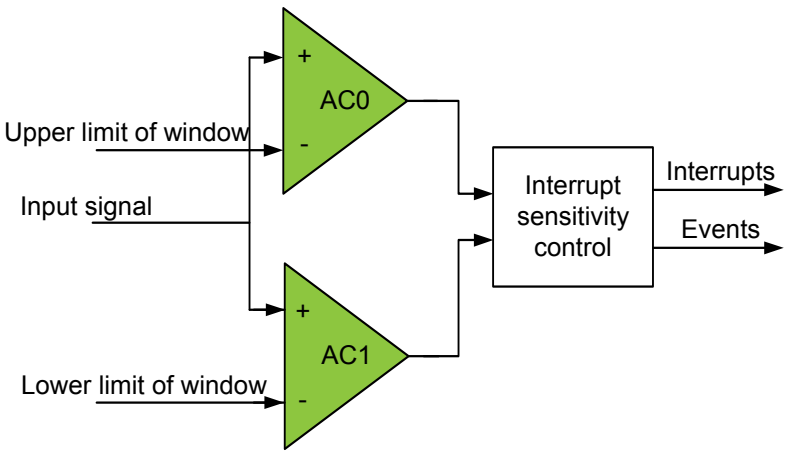


Figure 30-1. Analog comparator overview.



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 30-2.

Figure 30-2. Analog comparator window function.



36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.

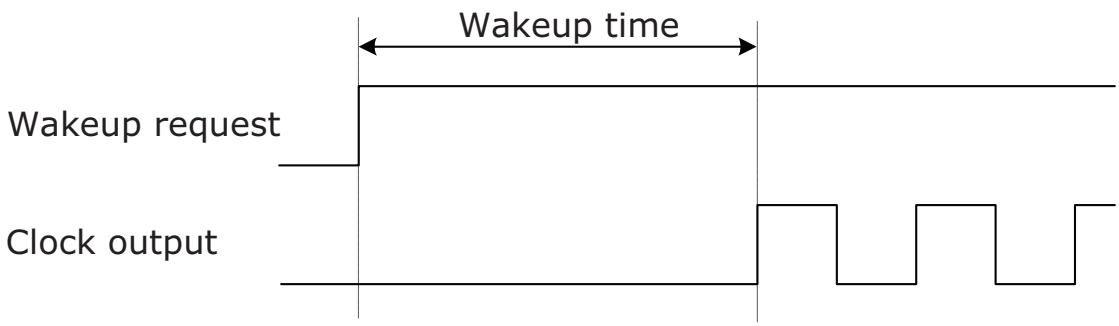


Table 36-42. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL [1]	Integral non-linearity	500ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
DNL [1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	lsb
	Offset Error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain Error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-43. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL [1]	Integral Non-Linearity	500ksps	All gain settings		±1.5	±4	lsb
	Gain Error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

36.4 ATxmega256A3U

36.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-97. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-98. General operating conditions.

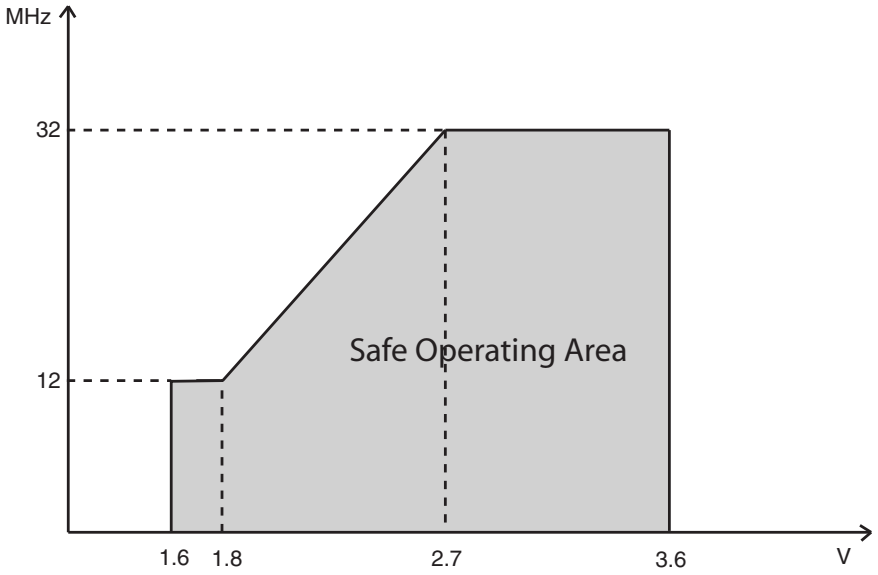
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		1.60		3.6	V
AV_{CC}	Analog Supply Voltage		1.60		3.6	V
T_A	Temperature range	85 °C	-40		85	°C
		105 °C	-40		105	
T_j	Junction temperature	85°C	-40		105	°C
		105°C	-40		125	

Table 36-99. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 36-22. Maximum Frequency vs. V_{CC}.



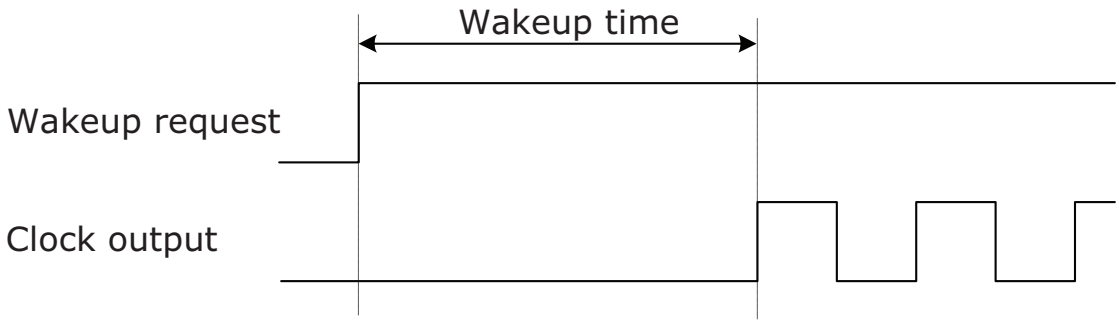
36.4.4 Wake-up time from sleep modes

Table 36-102. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-23. Wake-up time definition.



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance (1)	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = Safety factor				$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.2		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				6.8		pF
C_{LOAD}	Parasitic capacitance load				2.95		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

Figure 37-5. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

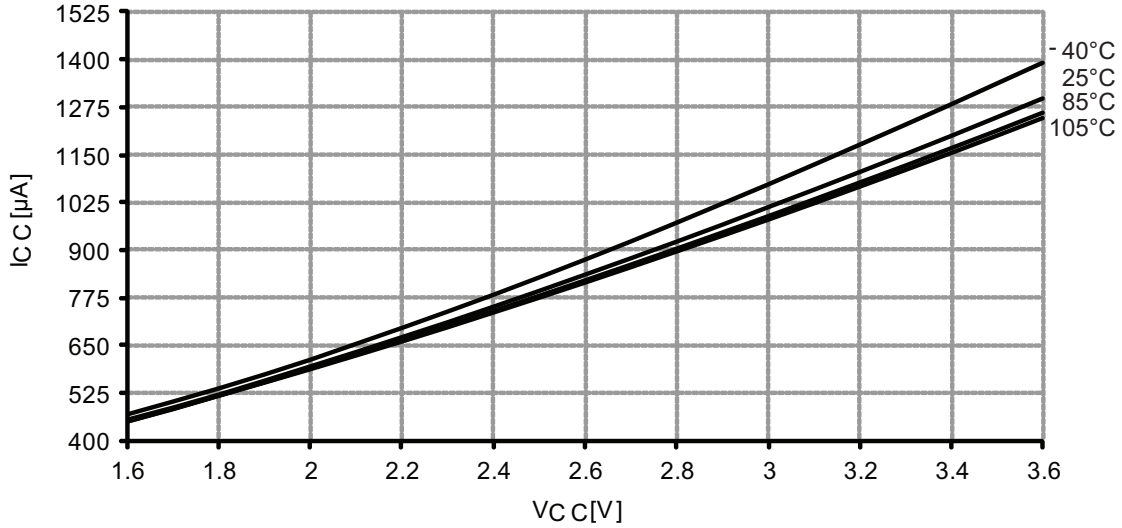


Figure 37-6. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

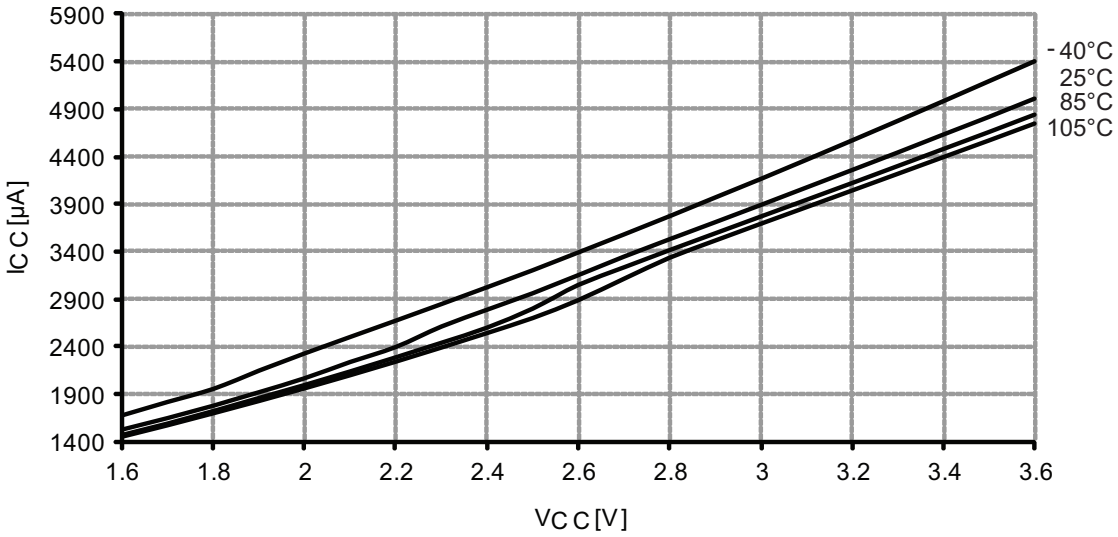


Figure 37-191. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

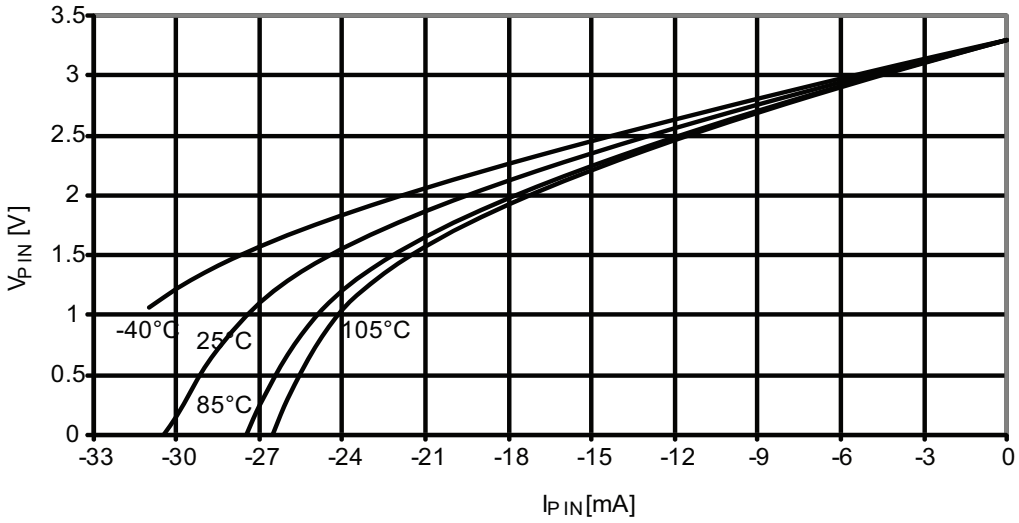


Figure 37-192. I/O pin output voltage vs. source current.

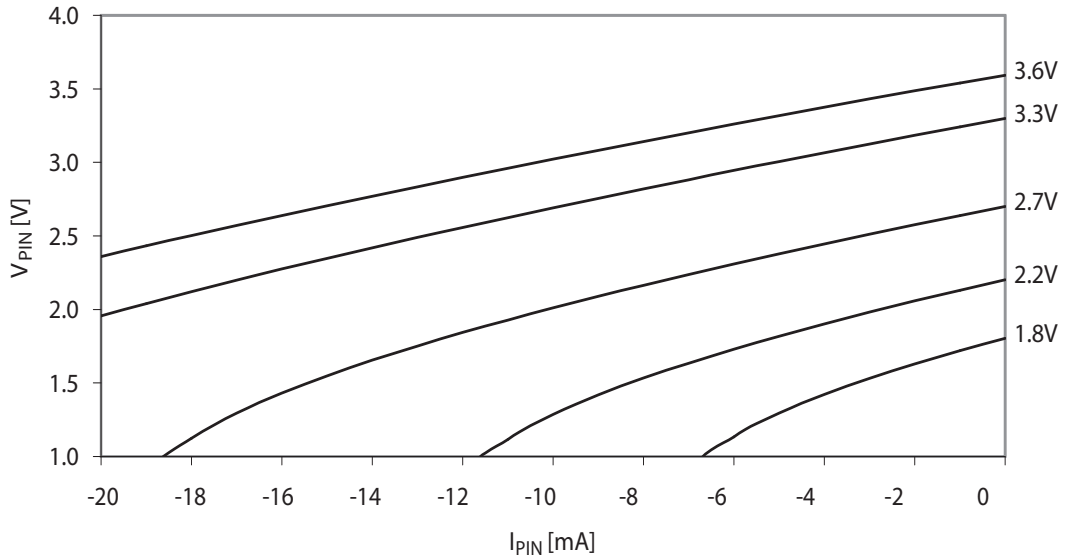


Figure 37-219. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

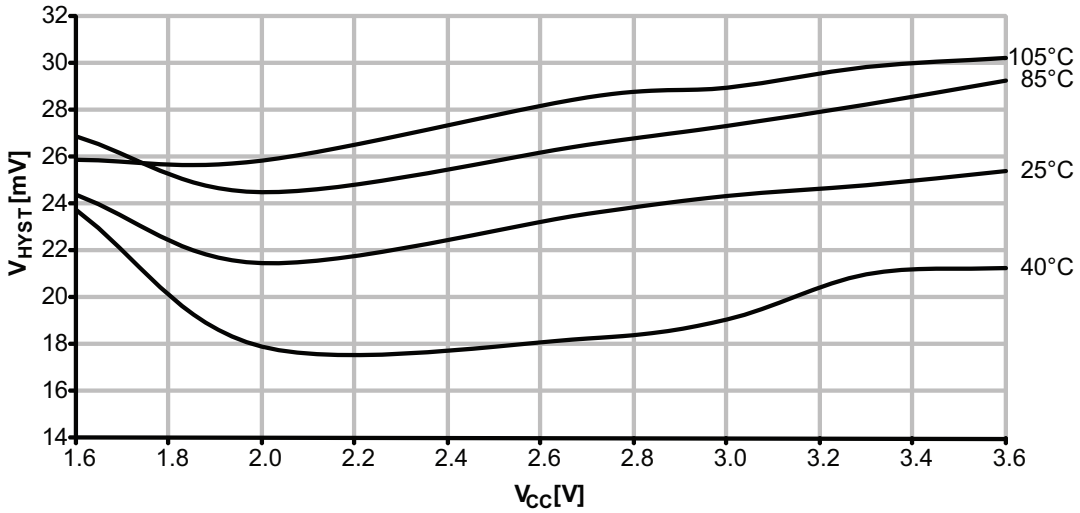


Figure 37-220. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

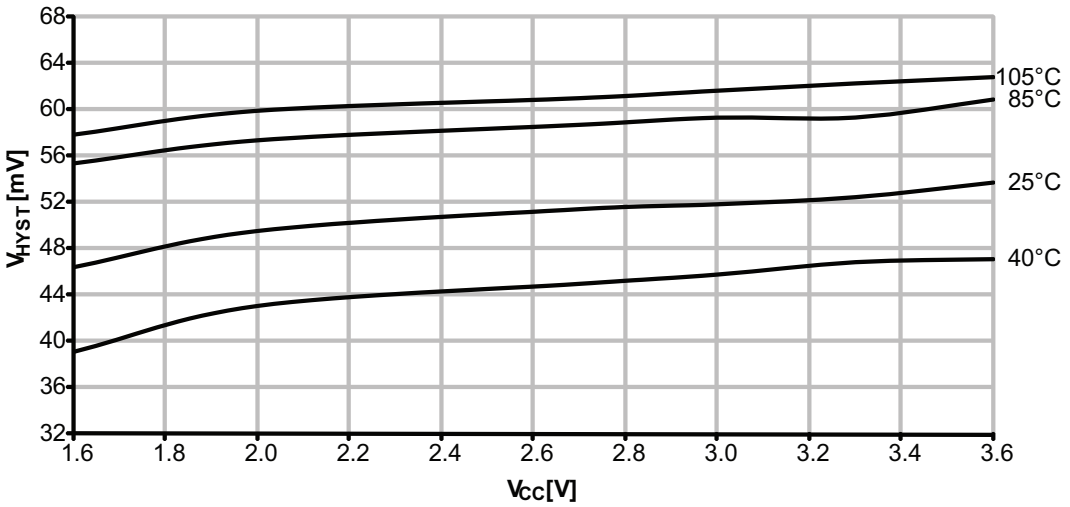


Figure 37-242. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

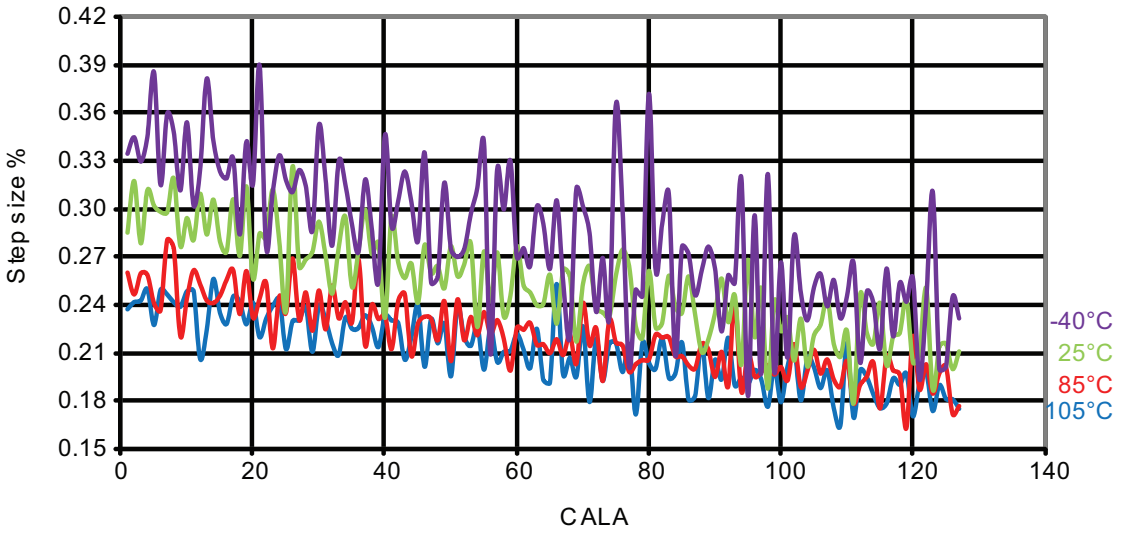


Figure 37-243. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.

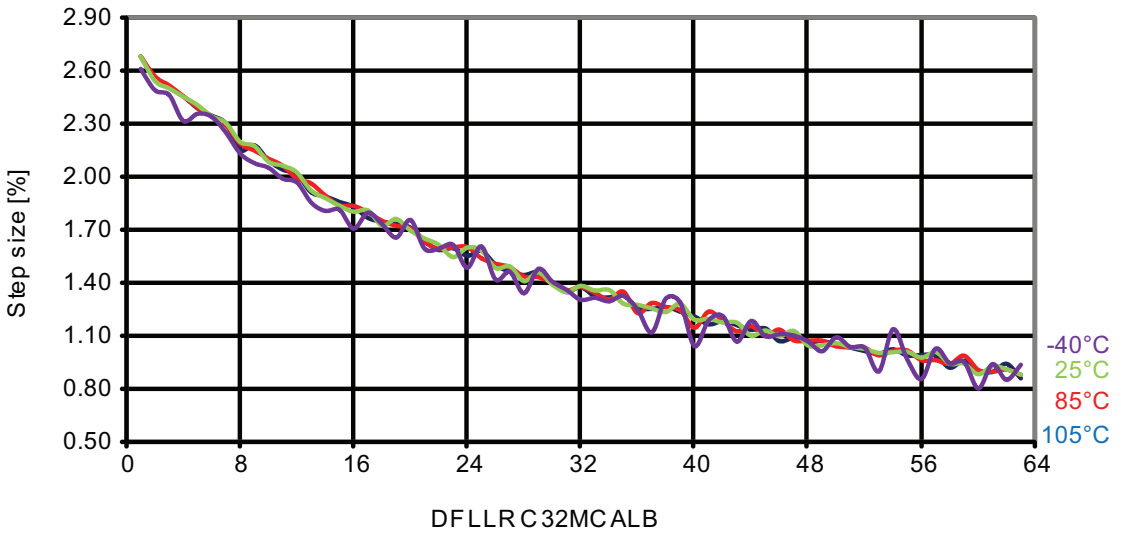


Figure 37-276. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

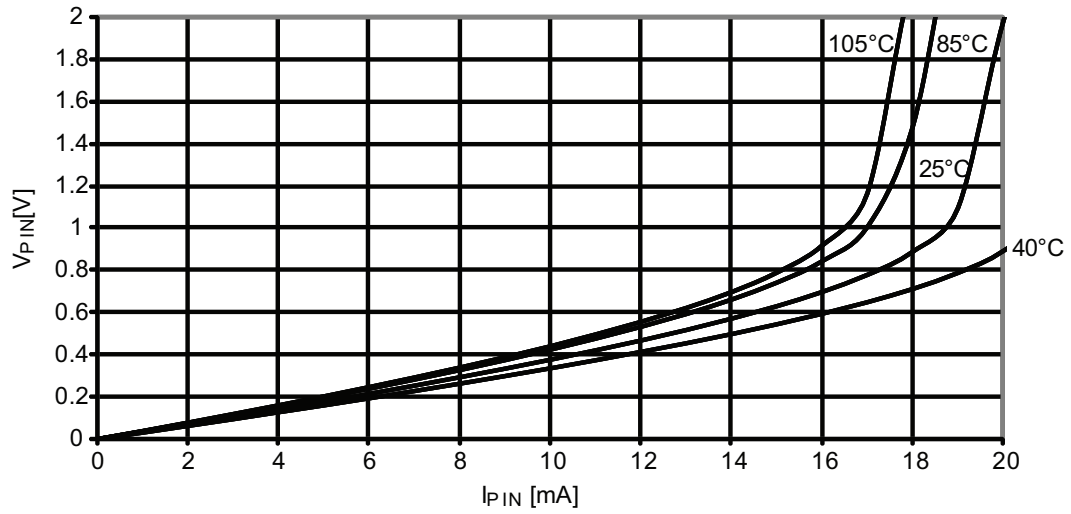
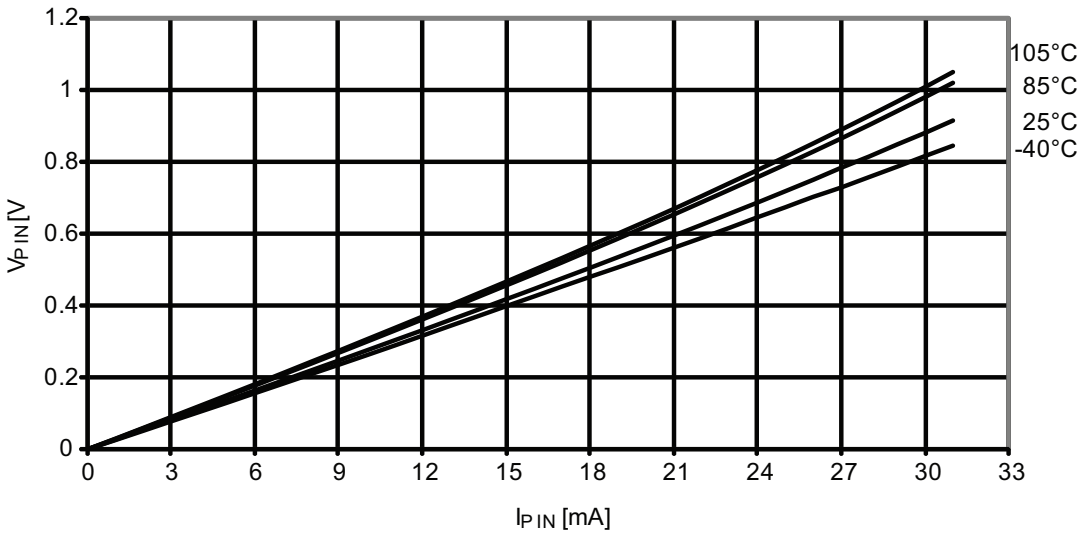


Figure 37-277. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.



37.4.3 ADC Characteristics

Figure 37-284. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

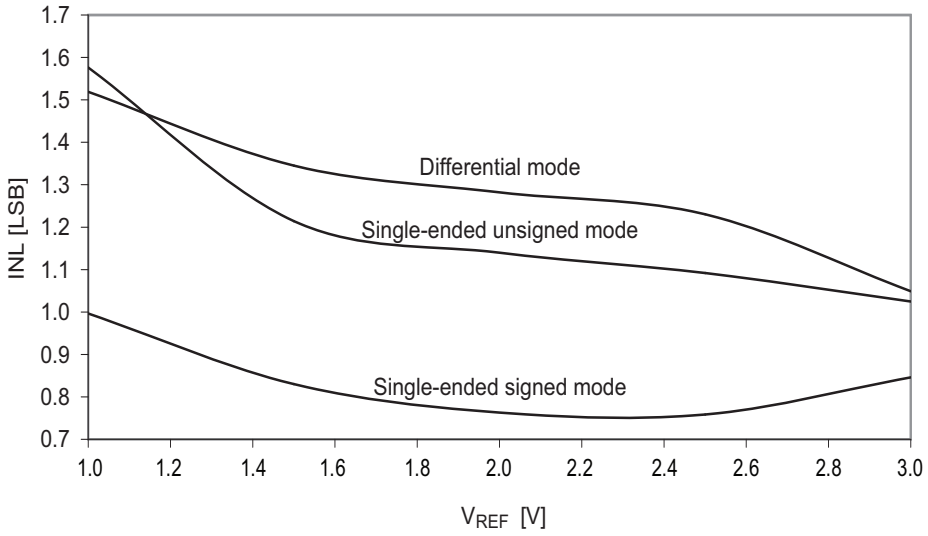
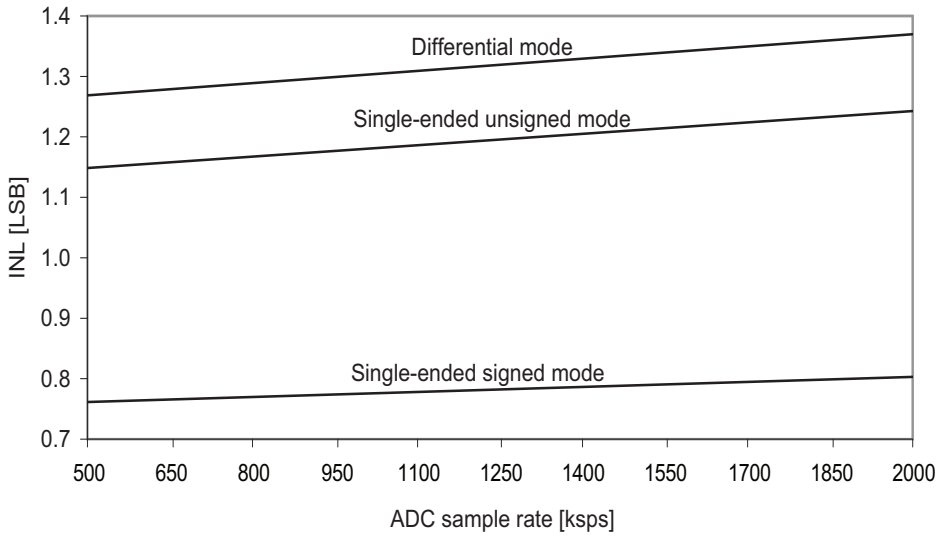


Figure 37-285. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.



37.4.10.4 32MHz Internal Oscillator

Figure 37-323. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

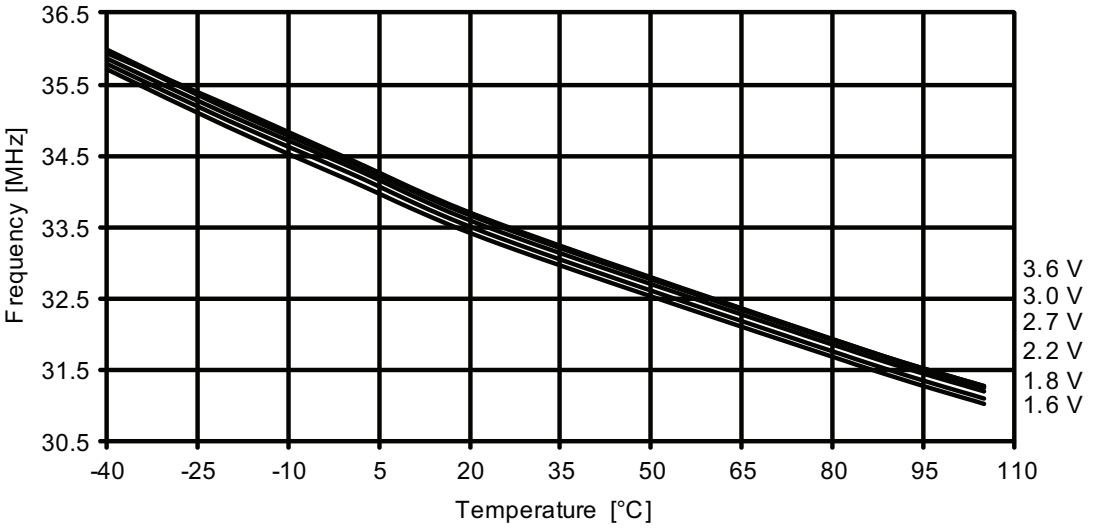
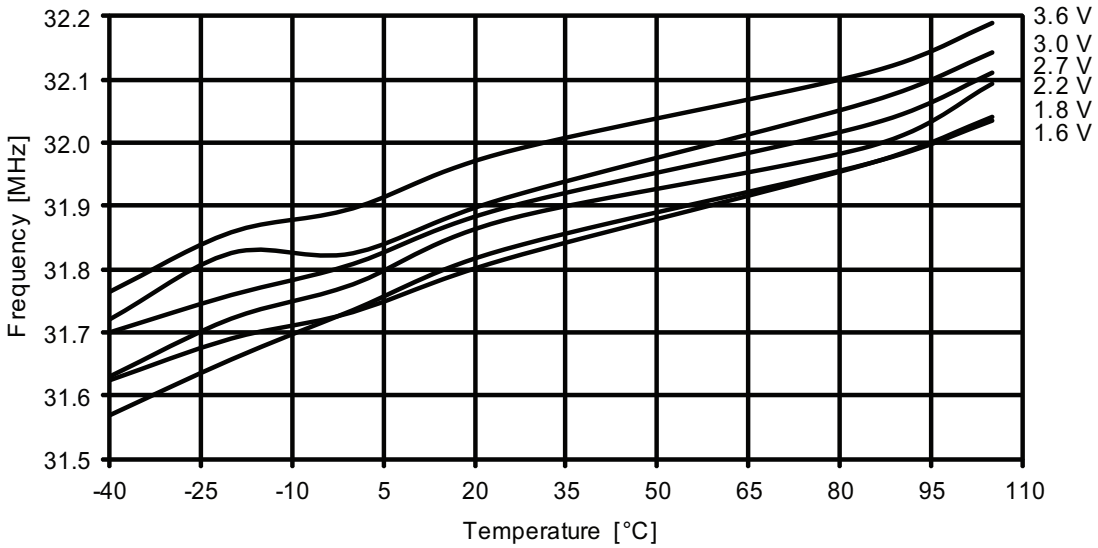


Figure 37-324. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.



39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8386E – 09/2014

1.	Updated "Ordering Information" on page 3: – Added Ordering information for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
	– Updated "Electrical Characteristics" on page 73 and onwards concerning "Power Consumption" and "Endurance and data retention" for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
2.	– Updated "Typical Characteristics" on page 161 and onwards for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
3.	– Corrected values for Active Current Consumption for 192A3U in Table 36-68 on page 119 and for 256A3U in Table 36-100 on page 141.
4	– Updated plots for Active supply current for 192A3U in Figure 37-167 on page 245 and Figure 37-168 on page 245
5	– Updated plots for Active supply current for 256A3U in Figure 37-251 on page 287 and Figure 37-252 on page 288
6.	– Corrected values for Bootloader start and end address for 128A3U in Table 7-1 on page 14.
7.	– Changed Vcc to AVcc in Section 28. "ADC – 12-bit Analog to Digital Converter" on page 52and in Section 30.1 "Features" on page 56.
8.	– Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 93, Table 36-64 on page 115, Table 36-96 on page 137 and Table 36-128 on page 159.
9.	– Added information in Section 38. "Errata" on page 329 on missing calibration of DAC channel 1.

39.2 8386D – 03/2014

1.	Updated "Port A - alternate functions." on page 61: – Removed ACDP POS from the Table 32-1 on page 61
2.	Updated "Port B - alternate functions." on page 61: – ACDB POS changed to ADCB POS/GAINPOS in the Table 32-2 on page 61

39.3 8386C – 02/2013

1.	Updated the datasheet using the Atmel new datasheet template.
2.	Added column for TWI with external driver interface for Port C and E in "Alternate Pin Functions" on page 61.
3.	Removed TWID from Port D and updated pin numbers in"Alternate Pin Functions" on page 61.
4.	Added TOSC and removed AWEXE to/from Port E in "Alternate Pin Functions" on page 61.
5.	Added notes to table for Port D and E in "Alternate Pin Functions" on page 61.