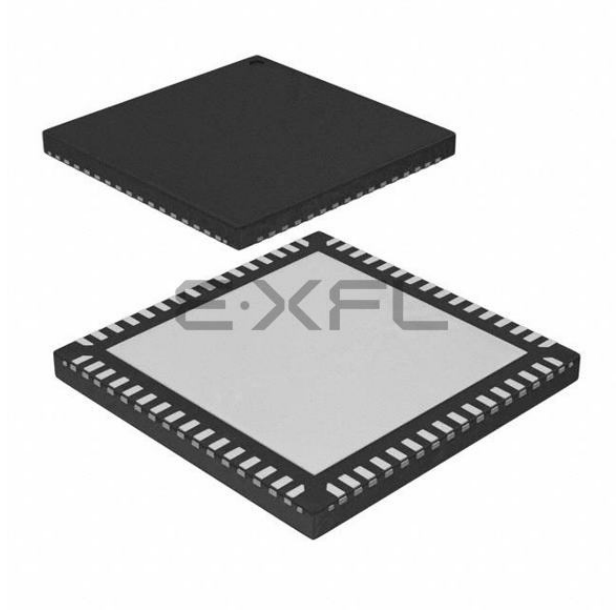

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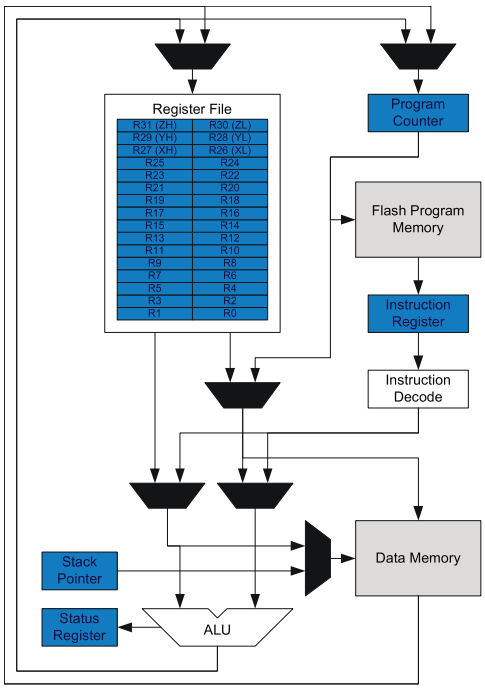
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8/16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 64KB (32K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a3u-mn |

**Figure 6-1. Block diagram of the AVR CPU architecture.**




The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

# 7. Memories

## 7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - 16 bit-accessible general purpose registers for global variables or flags
  - Bus arbitration
    - Deterministic priority handling between CPU, DMA controller, and other bus masters
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU and DMA controller
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

## 7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering Information” on page 3. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

# 16. TC0/1 – 16-bit Timer/Counter Type 0 and 1

## 16.1 Features

- Seven 16-bit timer/counters
  - Four timer/counters of type 0
  - Three timer/counters of type 1
  - Split-mode enabling two 8-bit timer/counter from each timer/counter type 0
- 32-bit Timer/Counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupts/events
- One compare match or input capture interrupt/event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- Can be used with DMA and to trigger DMA transactions
- High-resolution extension
  - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
- Advanced waveform extension:
  - Low- and high-side output with programmable dead-time insertion (DTI)
- Event controlled fault protection for safe disabling of drivers

## 16.2 Overview

Atmel AVR XMEGA devices have a set of seven flexible 16-bit Timer/Counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

### 36.2.6 ADC characteristics

**Table 36-40. Power supply, reference and input range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1 | | $AV_{CC}$- 0.6 | V |
| $R_{in}$ | Input resistance | Switched | | 5.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched | | 5.0 | | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7 | | pF |
| $V_{IN}$ | Input range | | -0.1 | | $AV_{CC}$+0.1 | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | V |
| $V_{IN}$ | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | V |
| ΔV | Fixed offset voltage | | | 190 | | LSB |

**Table 36-41. Clock and timing.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC Clock frequency | Maximum is 1/4 of Peripheral clock frequency | 100 | | 2000 | kHz |
| | | Measuring internal signals | 100 | | 125 | |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | 100 | | 2000 | ksps |
| | | CURRLIMIT = LOW | 100 | | 1500 | |
| | | CURRLIMIT = MEDIUM | 100 | | 1000 | |
| | | CURRLIMIT = HIGH | 100 | | 500 | |
| | Sampling Time | 1/2 $Clk_{ADC}$ cycle | 0.25 | | 5 | µs |
| | Conversion time (latency) | (RES+2)/2+(GAIN !=0)<br>RES (Resolution) = 8 or 12 | 5 | | 8 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | $Clk_{ADC}$ cycles |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | $Clk_{ADC}$ cycles |
| | | After ADC flush | | 1 | 1 | |

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 36-1 the Frequency vs. $V_{CC}$ curve is linear between $1.8V < V_{CC} < 2.7V$.

**Figure 36-15. Maximum Frequency vs. $V_{CC}$.**

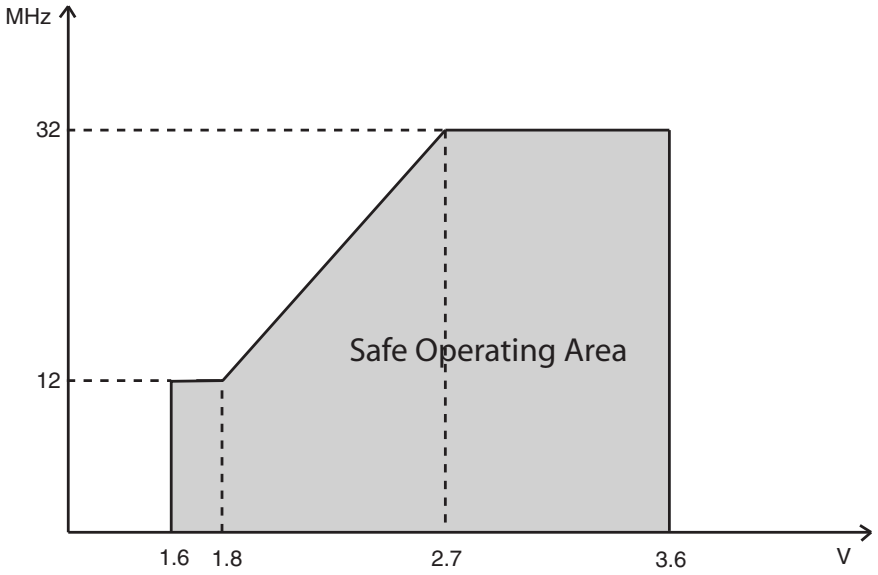


**Table 36-78. Accuracy characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Input Resolution | | | | | 12 | Bits |
| INL (1) | Integral non-linearity | $V_{REF}$= Ext 1.0V | $V_{CC}$ = 1.6V | | ±2.0 | ±3 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±2.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±2.0 | ±4 | |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±4 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±5.0 | | |
| | | | $V_{CC}$ = 3.6V | | ±5.0 | | |
| DNL (1) | Differential non-linearity | $V_{REF}$=Ext 1.0V | $V_{CC}$ = 1.6V | | ±1.5 | 3 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±1.0 | 3.5 | |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±4.5 | | |
| | | | $V_{CC}$ = 3.6V | | ±4.5 | | |
| | Gain error | After calibration | | | <4 | | lsb |
| | Gain calibration step size | | | | 4 | | lsb |
| | Gain calibration drift | $V_{REF}$= Ext 1.0V | | | <0.2 | | mV/K |
| | Offset error | After calibration | | | <1 | | lsb |
| | Offset calibration step size | | | | 1 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

### 36.3.8 Analog Comparator Characteristics

**Table 36-79. Analog Comparator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{off}$ | Input Offset Voltage | | | <±10 | | mV |
| $I_{lk}$ | Input Leakage Current | | | <1 | | nA |
| | Input voltage range | | -0.1 | | $AV_{CC}$ | V |
| | AC startup time | | | 100 | | µs |
| $V_{hys1}$ | Hysteresis, None | | | 0 | | mV |
| $V_{hys2}$ | Hysteresis, Small | mode = High Speed (HS) | | 13 | | mV |
| | | mode = Low Power (LP) | | 30 | | |
| $V_{hys3}$ | Hysteresis, Large | mode = HS | | 30 | | mV |
| | | mode = LP | | 60 | | |

**Table 36-95. SPI timing characteristics and requirements.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK Period | Master | | (See Table 21-4 in XMEGA AU Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5*SCK | | |
| $t_{SCKR}$ | SCK Rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK Fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 10 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 10 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5*SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1 | | |
| $t_{SSCK}$ | Slave SCK Period | Slave | 4*t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2*t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK Rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK Fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | t $Clk_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 21 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_Q$ | Negative impedance (1) | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | 2.4k | | | Ω |
| | | | 1MHz crystal, CL=20pF | 8.7k | | | |
| | | | 2MHz crystal, CL=20pF | 2.1k | | | |
| | | XOSCPWR=0, FRQRANGE=1, CL=20pF | 2MHz crystal | 4.2k | | | |
| | | | 8MHz crystal | 250 | | | |
| | | | 9MHz crystal | 195 | | | |
| | | XOSCPWR=0, FRQRANGE=2, CL=20pF | 8MHz crystal | 360 | | | |
| | | | 9MHz crystal | 285 | | | |
| | | | 12MHz crystal | 155 | | | |
| | | XOSCPWR=0, FRQRANGE=3, CL=20pF | 9MHz crystal | 365 | | | |
| | | | 12MHz crystal | 200 | | | |
| | | | 16MHz crystal | 105 | | | |
| | | XOSCPWR=1, FRQRANGE=0, CL=20pF | 9MHz crystal | 435 | | | |
| | | | 12MHz crystal | 235 | | | |
| | | | 16MHz crystal | 125 | | | |
| | | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | 495 | | | |
| | | | 12MHz crystal | 270 | | | |
| | | | 16MHz crystal | 145 | | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | 305 | | | |
| | | | 16MHz crystal | 160 | | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | 380 | | | |
| | | | 16MHz crystal | 205 | | | |
| | ESR | SF = Safety factor | | | | $\min(R_Q)/SF$ | kΩ |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | | 5.2 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | | 6.8 | | pF |
| $C_{LOAD}$ | Parasitic capacitance load | | | | 2.95 | | pF |

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

### 36.4.16 Two-Wire Interface Characteristics

Table 36-32 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7.

**Figure 36-28. Two-wire interface bus timing.**

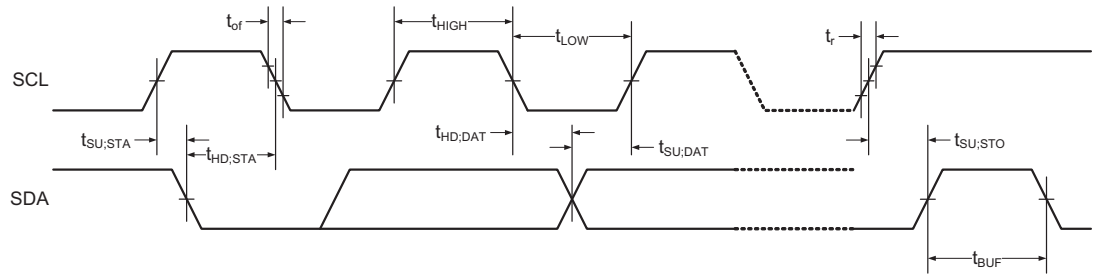



**Table 36-128. Two-wire interface characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 0.7*$V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.3*$V_{CC}$ | V |
| $V_{hys}$ | Hysteresis of Schmitt Trigger Inputs | | 0.05*$V_{CC}$ (1) | | | V |
| $V_{OL}$ | Output Low Voltage | 3mA, sink current | 0 | | 0.4 | V |
| $t_r$ | Rise Time for both SDA and SCL | | 20+0.1$C_b$ (1)(2) | | 300 | ns |
| $t_{of}$ | Output Fall Time from $V_{IHmin}$ to $V_{ILmax}$ | 10pF < $C_b$ < 400pF (2) | 20+0.1$C_b$ (1)(2) | | 250 | ns |
| $t_{SP}$ | Spikes Suppressed by Input Filter | | 0 | | 50 | ns |
| $I_I$ | Input Current for each I/O Pin | 0.1$V_{CC}$ < $V_I$ < 0.9$V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O Pin | | | | 10 | pF |
| $f_{SCL}$ | SCL Clock Frequency | $f_{PER}$ (3)>max(10$f_{SCL}$, 250kHz) | 0 | | 400 | kHz |
| $R_P$ | Value of Pull-up resistor | $f_{SCL} \leq$ 100kHz | $\frac{V_{CC}-0.4V}{3mA}$ | | $\frac{100ns}{C_b}$ | Ω |
| | | $f_{SCL}$ > 100kHz | | | $\frac{300ns}{C_b}$ | |
| $t_{HD;STA}$ | Hold Time (repeated) START condition | $f_{SCL} \leq$ 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ > 100kHz | 0.6 | | | |
| $t_{LOW}$ | Low Period of SCL Clock | $f_{SCL} \leq$ 100kHz | 4.7 | | | µs |
| | | $f_{SCL}$ > 100kHz | 1.3 | | | |
| $t_{HIGH}$ | High Period of SCL Clock | $f_{SCL} \leq$ 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ > 100kHz | 0.6 | | | |

### 37.1.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-23. I/O pin output voltage vs. source current.**
***$V_{CC}$ = 1.8V.***

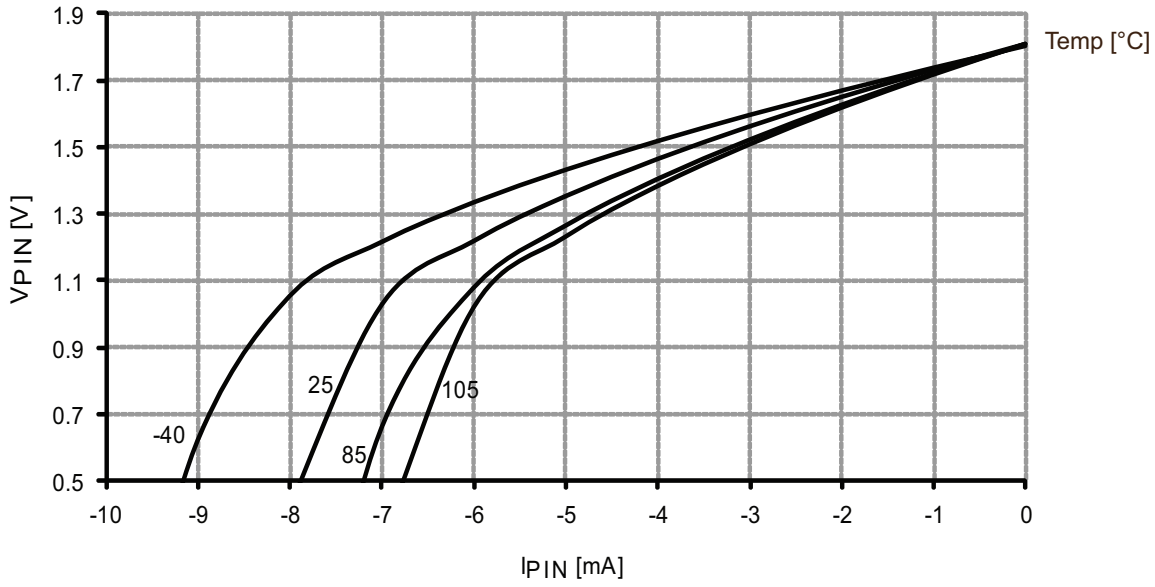



**Figure 37-24. I/O pin output voltage vs. source current.**
***$V_{CC}$ = 3.0V.***

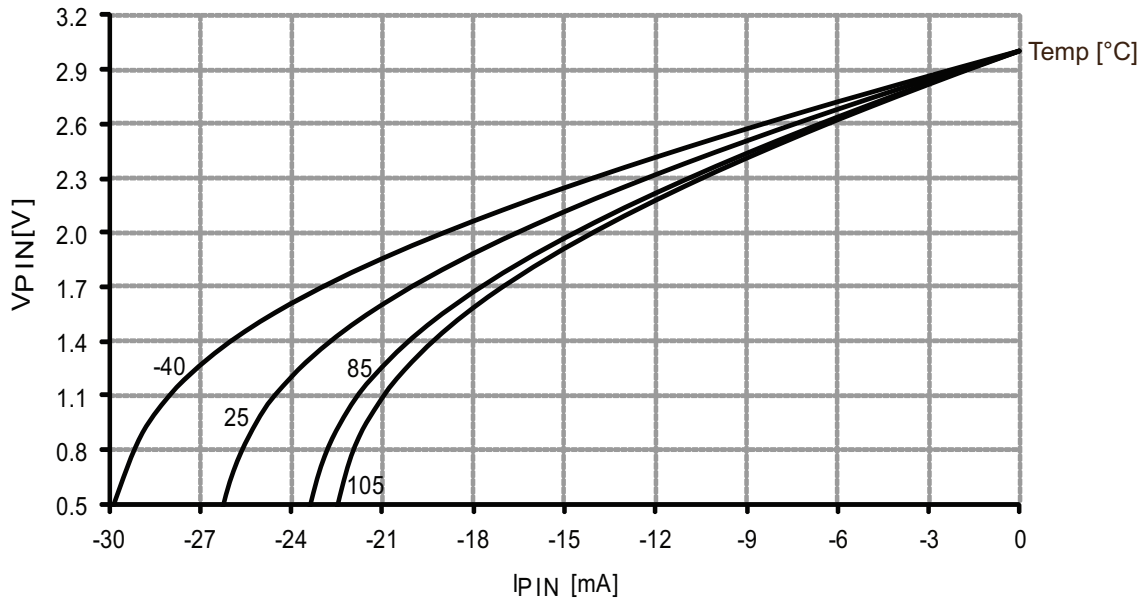


**Figure 37-159. 32MHz internal oscillator CALA calibration step size.**

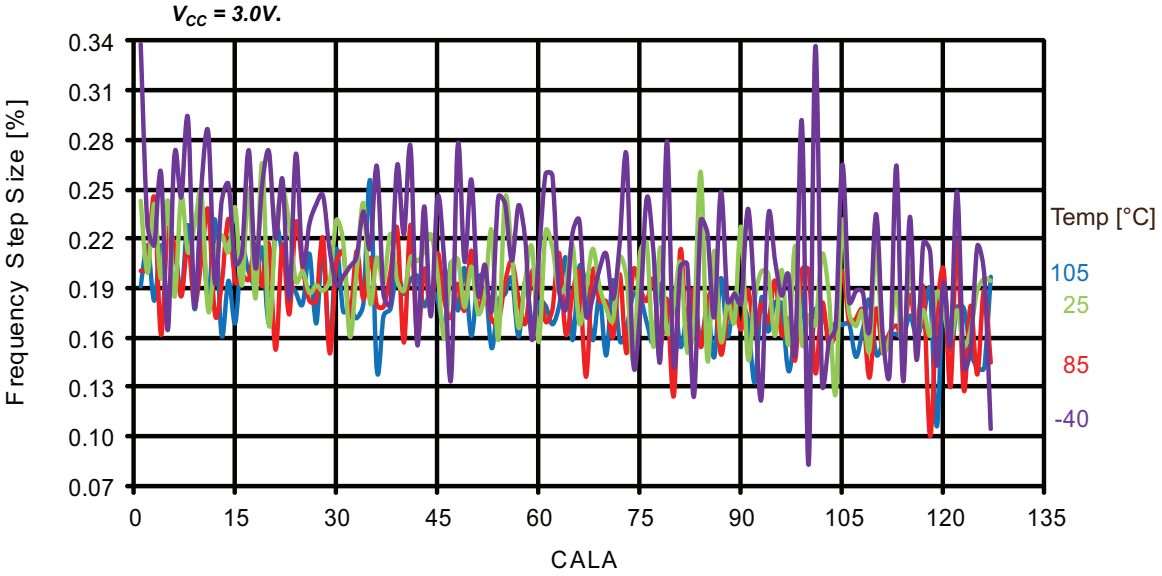
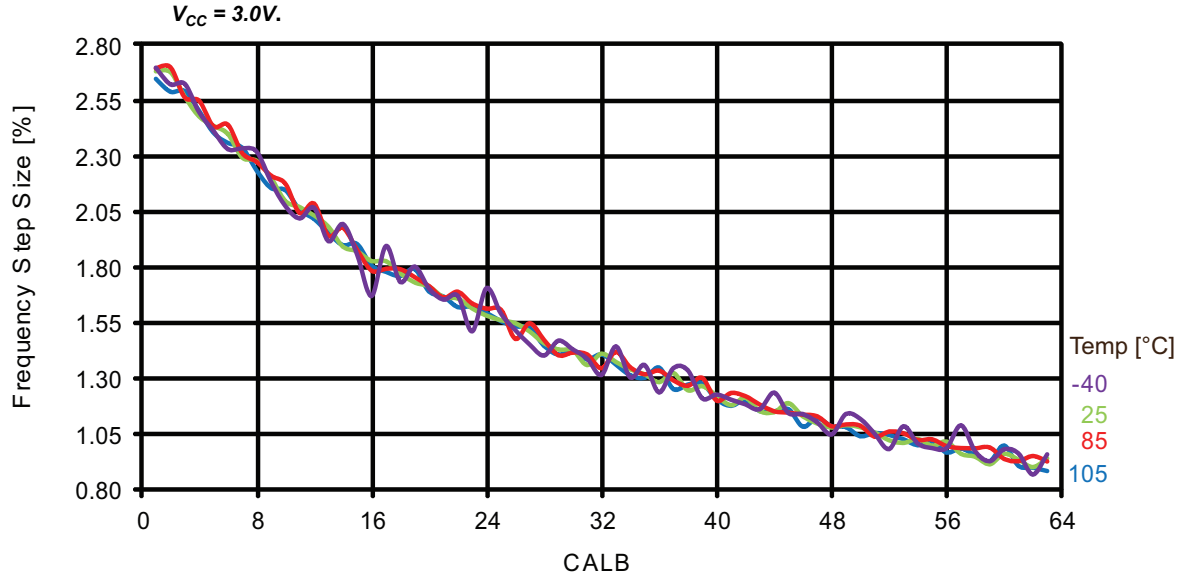



**Figure 37-160. 32MHz internal oscillator frequency vs. CALB calibration value.**



### 37.2.10.5 32MHz internal oscillator calibrated to 48MHz

**Figure 37-161. 48MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

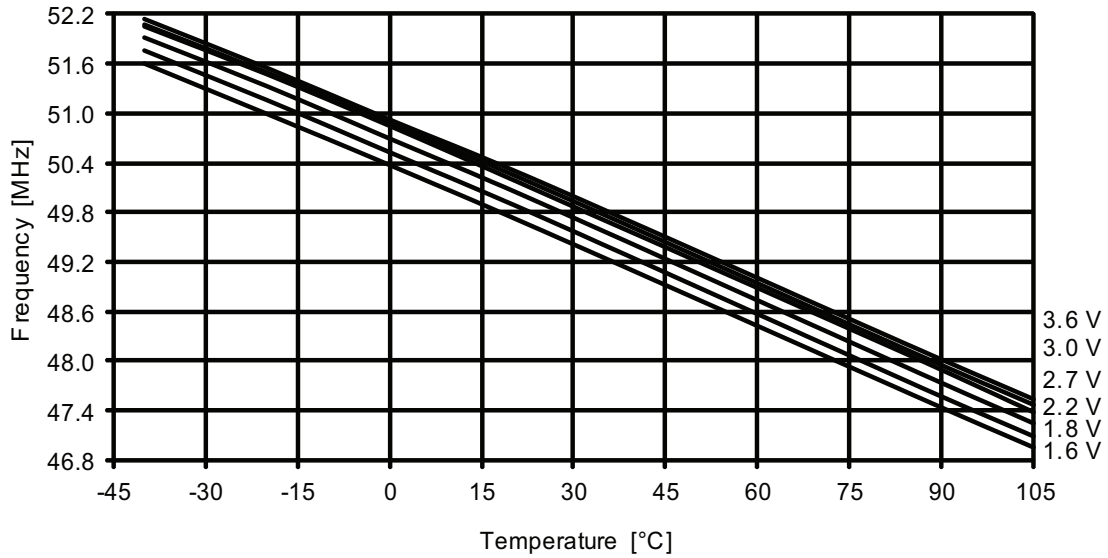
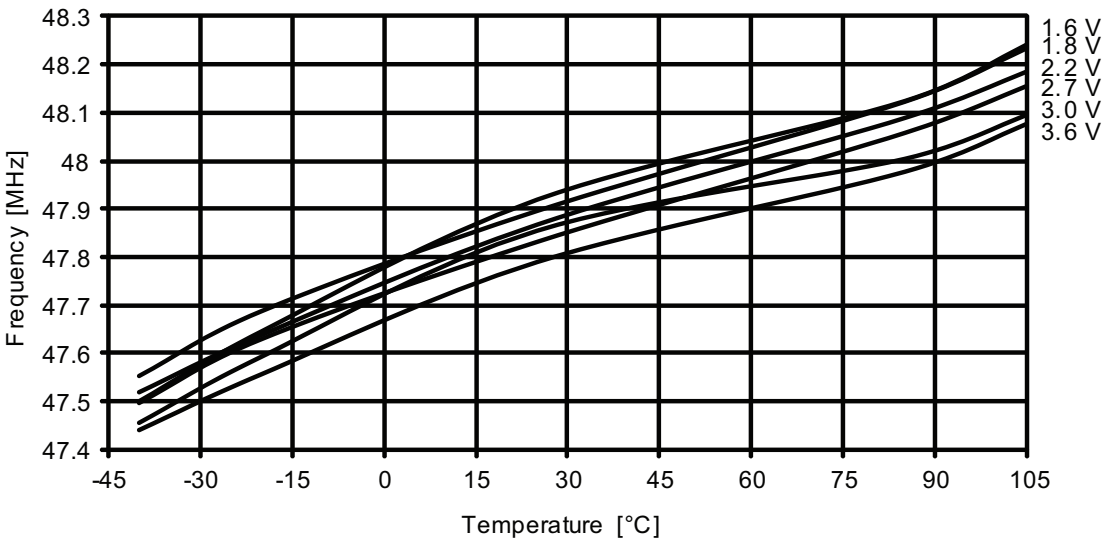



**Figure 37-162. 48MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***



## 37.3 ATxmega192A3U

### 37.3.1 Current consumption

#### 37.3.1.1 Active mode supply current

**Figure 37-167. Active supply current vs. frequency.**
***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

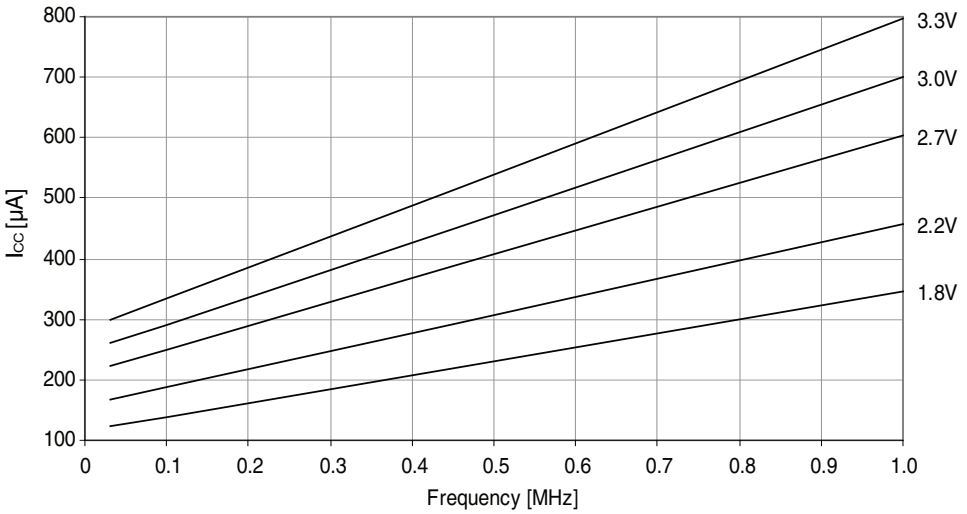



**Figure 37-168. Active supply current vs. frequency.**
***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

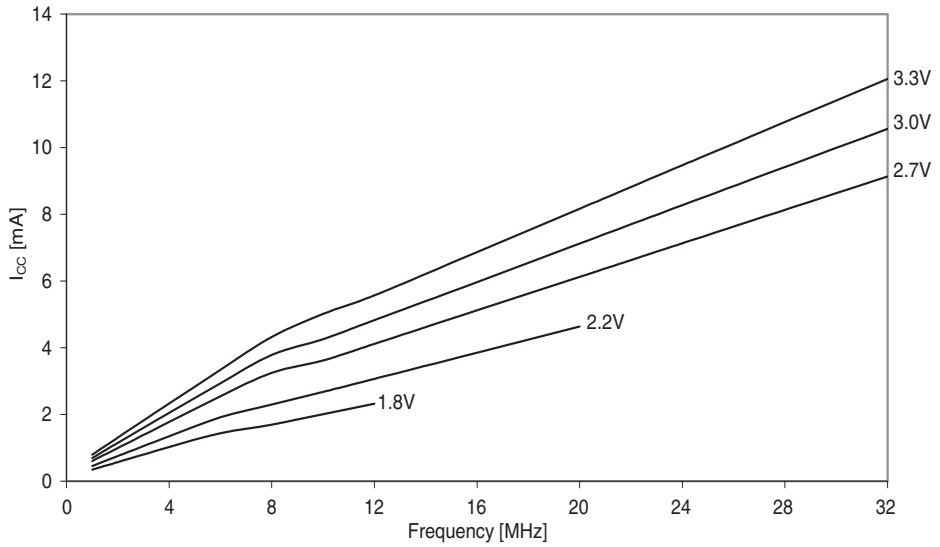


**Figure 37-207. Gain error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

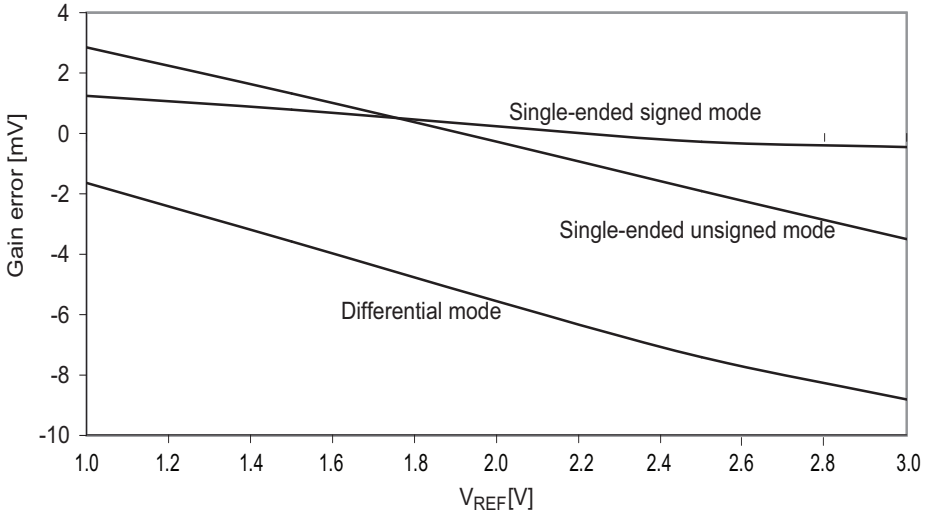
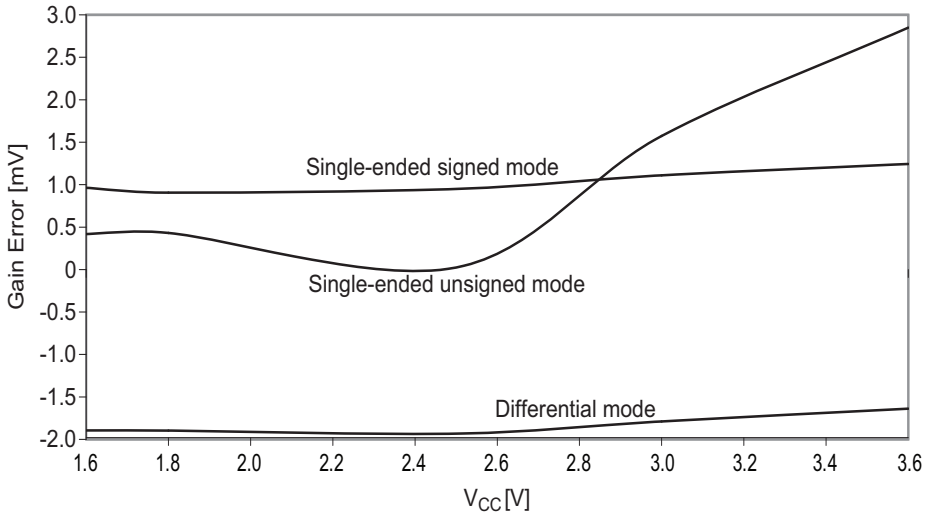



**Figure 37-208. Gain error vs. $V_{CC}$.**

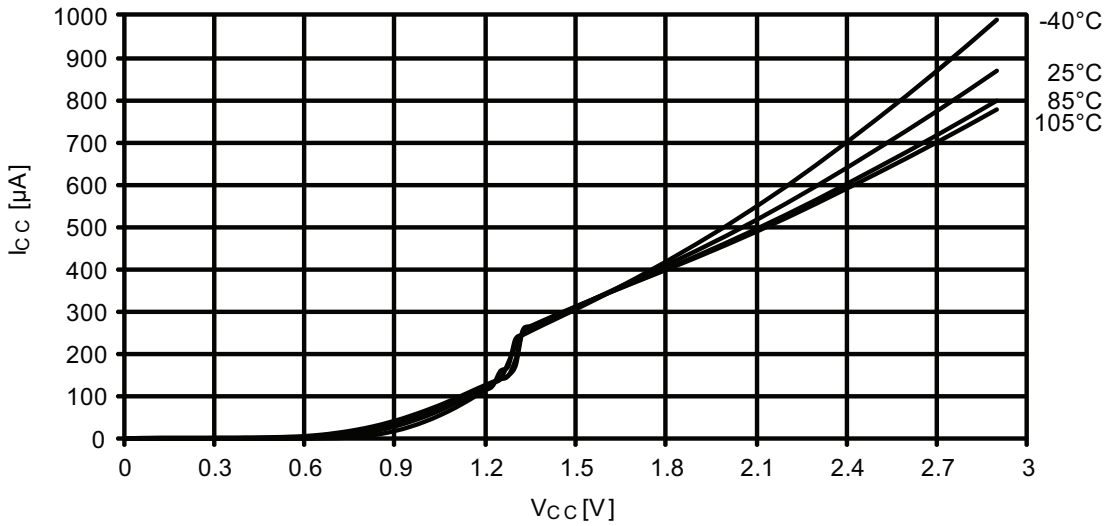
***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***



### 37.3.9 Power-on Reset Characteristics

**Figure 37-233. Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in continuous mode.***



### 37.4.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-272. I/O pin output voltage vs. source current.**
***$V_{CC}$ = 1.8V.***

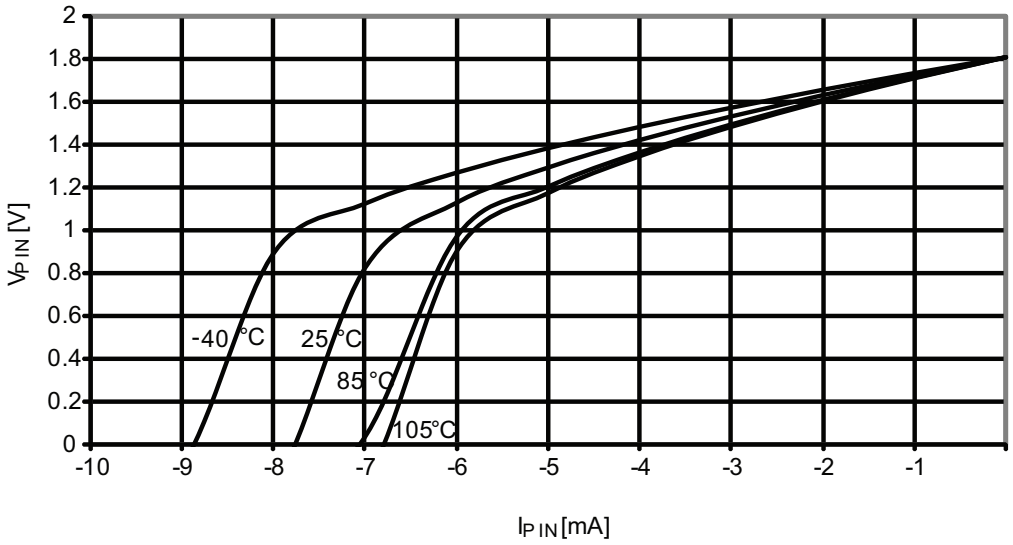
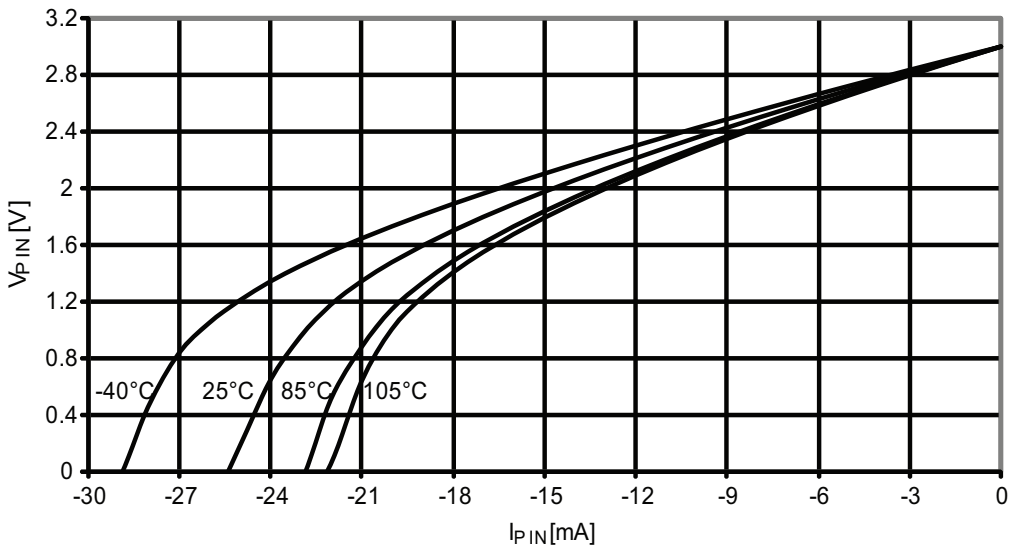



**Figure 37-273. I/O pin output voltage vs. source current.**
***$V_{CC}$ = 3.0V.***



### 37.4.2.3 Thresholds and Hysteresis

**Figure 37-280. I/O pin input threshold voltage vs. $V_{CC}$.**
***T = 25°C.***

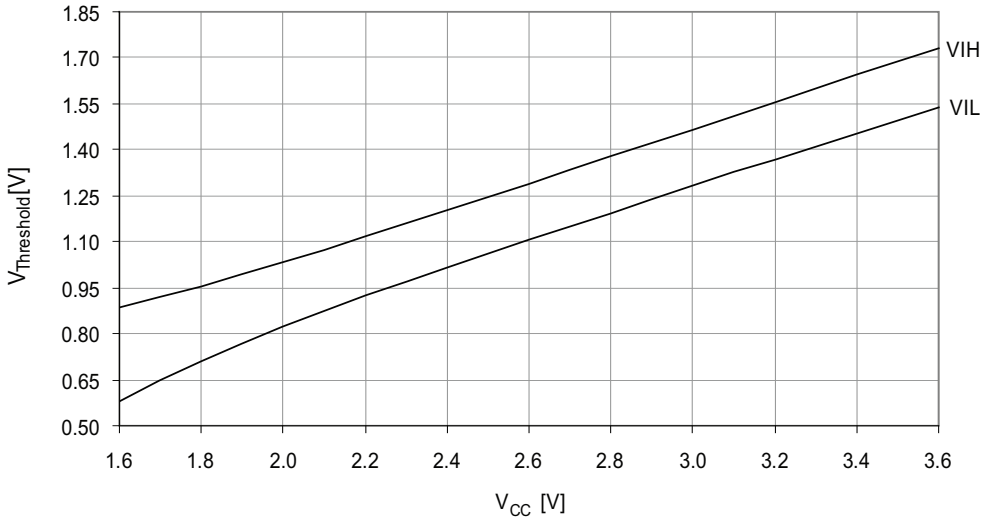



**Figure 37-281. I/O pin input threshold voltage vs. $V_{CC}$.**
***$V_{IH}$ I/O pin read as "1".***

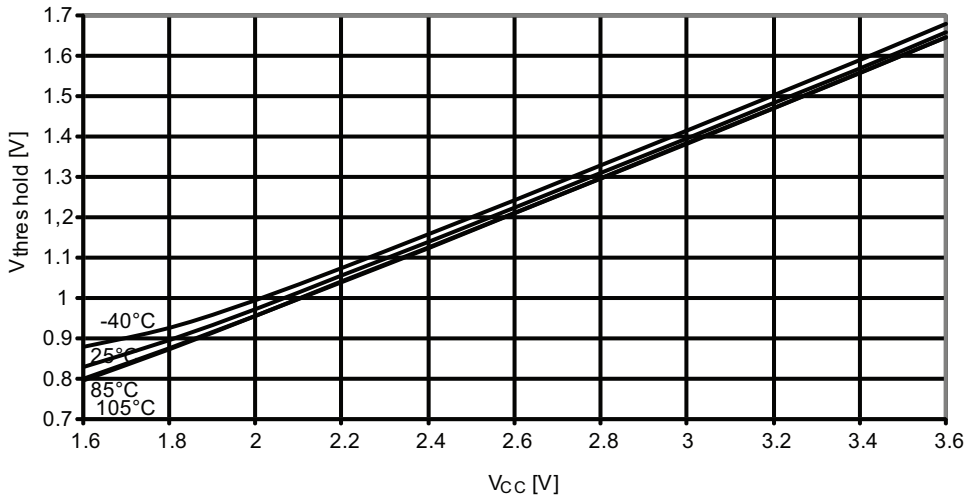
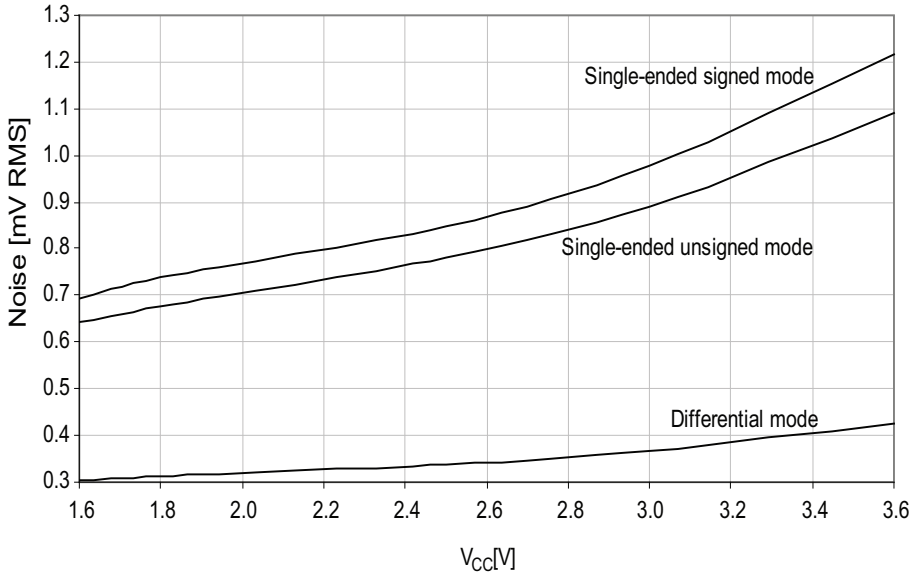


**Figure 37-296. Noise vs. $V_{CC}$.**

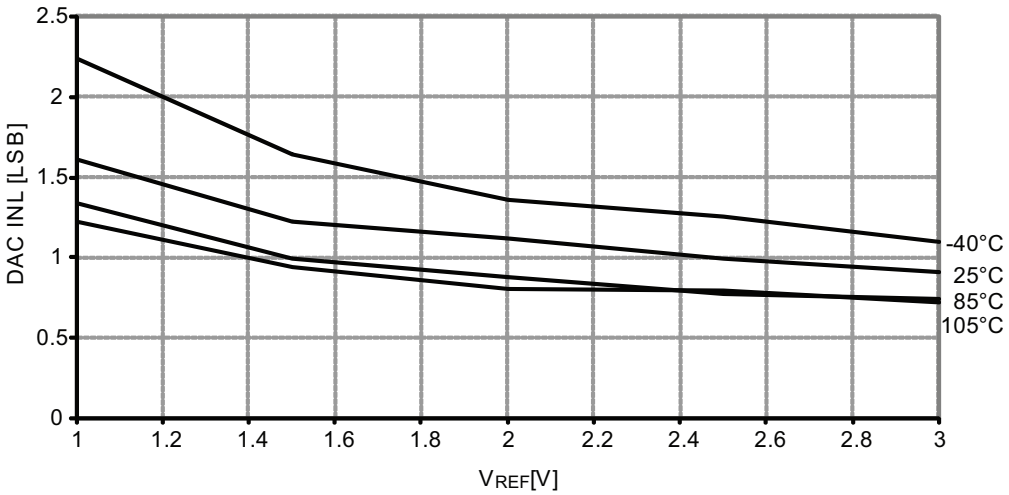
*T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.*




### 37.4.4 DAC Characteristics

**Figure 37-297. DAC INL error vs. $V_{REF}$.**

*$V_{CC}$ = 3.6V.*

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