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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53010cqt240

1 MCF5301*x* Family Comparison

The following table compares the various device derivatives available within the MCF5301*x* family.

Table 1. MCF5301*x* Family Configurations

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
Version 3 ColdFire Core with EMAC (enhanced multiply-accumulate unit)	•	•	•	•	•	•	•	•
Core (system) clock	up to 240 MHz							
Peripheral and external bus clock (Core clock ÷ 3)	up to 80 MHz							
Performance (Dhrystone/2.1 MIPS)	up to 211							
Unified data/instruction cache	16 Kbytes							
Static RAM (SRAM)	128 Kbytes							
Voice-over-IP software	—	—	•	•	—	—	•	•
Cryptography acceleration unit (CAU)	—	•	—	•	—	•	—	•
Random number generator	—	•	—	•	—	•	—	•
Smart card interface (SIM)	1 port				2 ports			
Voice-band audio codec	•	•	•	•	•	•	•	•
Integrated audio amplifiers	—	—	—	—	•	•	•	•
IC identification module (IIM)	2 Kbits							
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•	•	•	•
SDR/DDR SDRAM controller	•	•	•	•	•	•	•	•
FlexBus external interface	•	•	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•	•	•
USB 2.0 Host	—	—	—	—	•	•	•	•
Synchronous serial interface (SSI)	•	•	•	•	•	•	•	•
Fast Ethernet controller (FEC)	2	2	2	2	2	2	2	2
UARTs	3	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•	•
DSPI	•	•	•	•	•	•	•	•
Real-time clock	•	•	•	•	•	•	•	•
32-bit DMA timers	4	4	4	4	4	4	4	4
Watchdog timer (WDT)	•	•	•	•	•	•	•	•
Periodic interrupt timers (PIT)	4	4	4	4	4	4	4	4
Edge port module (EPORT)	•	•	•	•	•	•	•	•
Interrupt controllers (INTC)	2	2	2	2	2	2	2	2

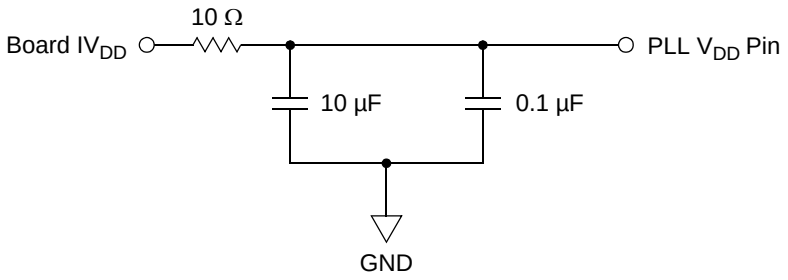


Figure 1. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

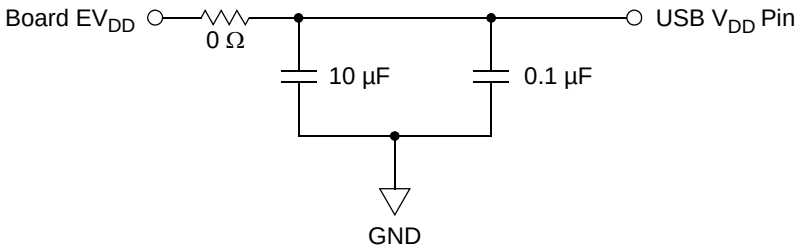


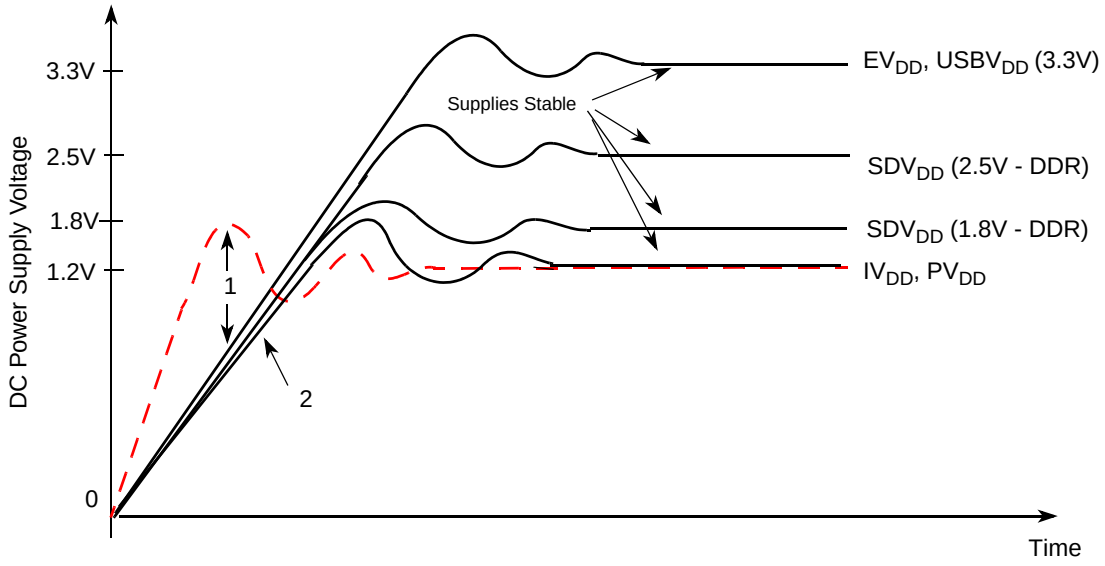
Figure 2. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing

Figure 3 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic / core V_{DD} (IV_{DD}). The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.



Notes:
1. IV_{DD} should not exceed EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V at any time, including power-up.
2. Recommended that IV_{DD}/PV_{DD} should track EV_{DD}/SDV_{DD} up to 0.9V then separate for completion of ramps
3. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PV_{DD} and EV_{DD}/SDV_{DD} should track up to 0.9V and then separate for the completion of ramps with EV_{DD}/SDV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.3.2 Power Down Sequence

If IV_{DD}/PV_{DD} are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or PV_{DD} going low by more than 0.4V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0V.
2. Drop EVDD/SDVDD supplies.

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	154	D15
SD_CKE	—	—	—	—	O	SDVDD	151	B15
SD_CLK	—	—	—	—	O	SDVDD	190	A7
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	191	A6
$\overline{\text{SD\_CS0}}$	—	—	—	—	O	SDVDD	155	A15
SD_DQS[1:0]	—	—	—	—	O	SDVDD	196, 167	C12, A5
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	152	C15
SD_SDR_DQS	—	—	—	—	I	SDVDD	207	D5
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	150	D14
External Interrupts Port 1[4,5]								
$\overline{\text{IRQ1DEBUG}}$[7:4]	PIRQ1DEBUG [7:4]	DDATA[3:0]	—	—	I	EVDD	—	H1, H4-2
$\overline{\text{IRQ1DEBUG}}$[3:0]	PIRQ1DEBUG [3:0]	PST[3:0]	—	—	I	EVDD	—	K14, H14, K15, J13
$\overline{\text{IRQ1FEC7}}$	PIRQ1FEC7	RMII1_CRS_DV	MII0_CRS	—	I	EVDD	29	J1
$\overline{\text{IRQ1FEC6}}$	PIRQ1FEC6	RMII1_RXER	MII0_RXCLK	—	I	EVDD	30	J2
$\overline{\text{IRQ1FEC5}}$	PIRQ1FEC5	RMII1_TXEN	MII0_TXCLK	—	I	EVDD	31	K4
$\overline{\text{IRQ1FEC4}}$	PIRQ1FEC4	RMII1_REF_CLK	—	D	I	EVDD	32	J3
$\overline{\text{IRQ1FEC}}$[3:2]	PIRQ1FEC[3:2]	RMII1_RXD[1:0]	MII0_RXD[3:2]	—	I	EVDD	33, 34	J4, K1
$\overline{\text{IRQ1FEC}}$[1:0]	PIRQ1FEC[1:0]	RMII1_TXD[1:0]	MII0_TXD[3:2]	—	I	EVDD	35, 36	K2, L1
External Interrupts Port 0[5]								
$\overline{\text{IRQ07}}$	PIRQ07	—	—	U	I	EVDD	10	E4
$\overline{\text{IRQ06}}$	PIRQ06	—	USB_CLKIN	U	I	EVDD	—	L13
$\overline{\text{IRQ04}}$	PIRQ04	$\overline{\text{DREQ0}}$	—	U	I	EVDD	19	D1
$\overline{\text{IRQ01}}$	PIRQ01	$\overline{\text{DREQ1}}$	—	U	I	EVDD	11	F4
Enhanced Secure Digital Host Controller								
SDHC_DAT3	PSDHC5	—	—	UD	I/O	EVDD	60	N4
SDHC_DAT[2:0]	PSDHC[4:2]	—	—	U	I/O	EVDD	61–63	R5, N6, N5
SDHC_CMD	PSDHC1	—	—	U	I/O	EVDD	59	R4
SDHC_CLK	PSDHC0	—	—	—	O	EVDD	58	R3

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
USB Host								
USBH_DM	—	—	—	—	O	USB VDD	—	B1
USBH_DP	—	—	—	—	O	USB VDD	—	C1
FEC 1								
RMII1_MDC	PFECI2C5	—	MII0_TXER	—		EVDD	22	E1
RMII1_MDIO	PFECI2C4	—	MII0_COL	—		EVDD	23	F1
FEC 0								
RMII0_CRS_DV	PFEC06	—	MII0_RXDV	—		EVDD	131	G16
RMII0_RXD[1:0]	PFEC0[5:4]	—	MII0_RXD[1:0]	—		EVDD	130, 129	H15, H16
RMII0_RXER	PFEC03	—	MII0_RXER	—		EVDD	127	J16
RMII0_TXD[1:0]	PFEC0[2:1]	—	MII0_TXD[1:0]	—		EVDD	125, 124	J15, J14
RMII0_TXEN	PFEC00	—	MII0_TXEN	D		EVDD	123	K16
RMII0_MDC	PFECI2C3	—	MII0_MDC	—		EVDD	133	G14
RMII0_MDIO	PFECI2C2	—	MII0_MDIO	—		EVDD	132	G15
Real Time Clock								
RTC_EXTAL	—	—	—	—	I	EVDD	—	P1
RTC_XTAL	—	—	—	—	O	EVDD	—	R1
Synchronous Serial Interface								
SSI_RXD	PSSI4	—	U1RXD	UD	I	EVDD	—	N3
SSI_TXD	PSSI3	—	U1TXD	UD	O	EVDD	—	P3
SSI_FS	PSSI2	—	$\overline{\text{U1RTS}}$	—	I/O	EVDD	—	R2
SSI_MCLK	PSSI1	—	SSI_CLKIN	—	O	EVDD	—	P4
SSI_BCLK	PSSI0	—	$\overline{\text{U1CTS}}$	—	I/O	EVDD	—	P5
I^2C								
I2C_SCL	PFECI2C1	U2RXD	RMII1_MDC	U	I/O	EVDD	37	M1
I2C_SDA	PFECI2C0	U2TXD	RMII1_MDIO	U	I/O	EVDD	38	K3
DSPI								
DSPI_PCS3	PDSPI6	USBH_VBUS_EN	—	—	I/O	EVDD	—	P2
DSPI_PCS2	PDSPI5	USBH_VBUS_OC	—	—	I/O	EVDD	—	N2

4.2 Pinout—208 LQFP

The pinout for the 208 LQFP devices is shown in Figure 5 and Figure 6.

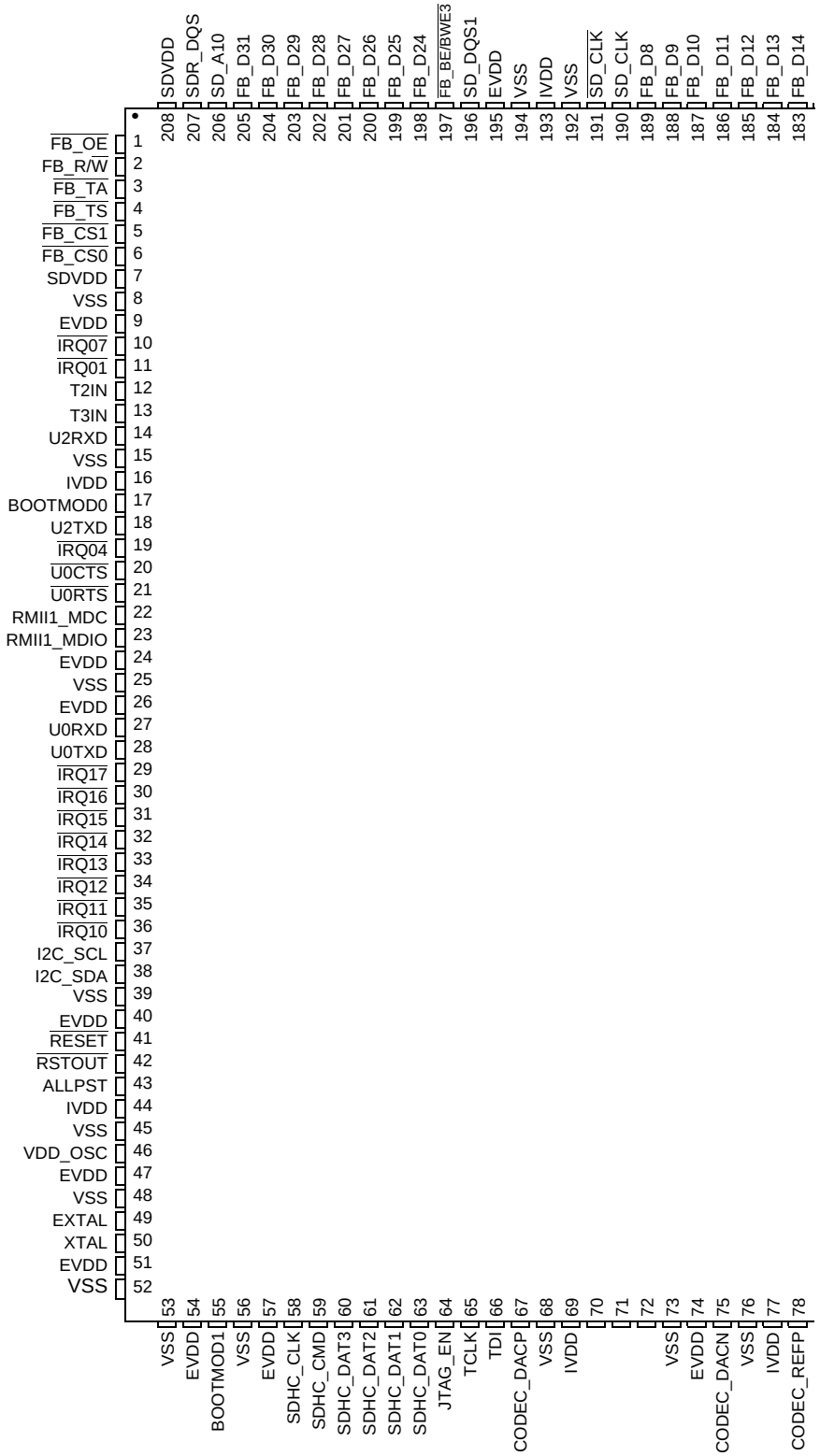


Figure 5. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Left (208 QFP)

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	208 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	36[1,2]	38[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	32[1,2]	33[1,2]	°C/W
Junction to board		θ_{JB}	25[3]	29[3]	°C/W
Junction to case		θ_{JC}	14[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	^{0}C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

Chip-select, $\overline{\text{FB\_CS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is 1‘compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	80	Mhz	$f_{sys/3}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	12.5	—	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0] and $\overline{\text{OE}}$)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0], and $\overline{\text{OE}}$)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	t_{CIFBCH}	0	—	ns	

1 Timing for chip selects only applies to the $\overline{\text{FB\_CS}}$[5:0] signals. Please see Section 5.7.2, “DDR SDRAM AC Timing Characteristics” for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *MCF5301x Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

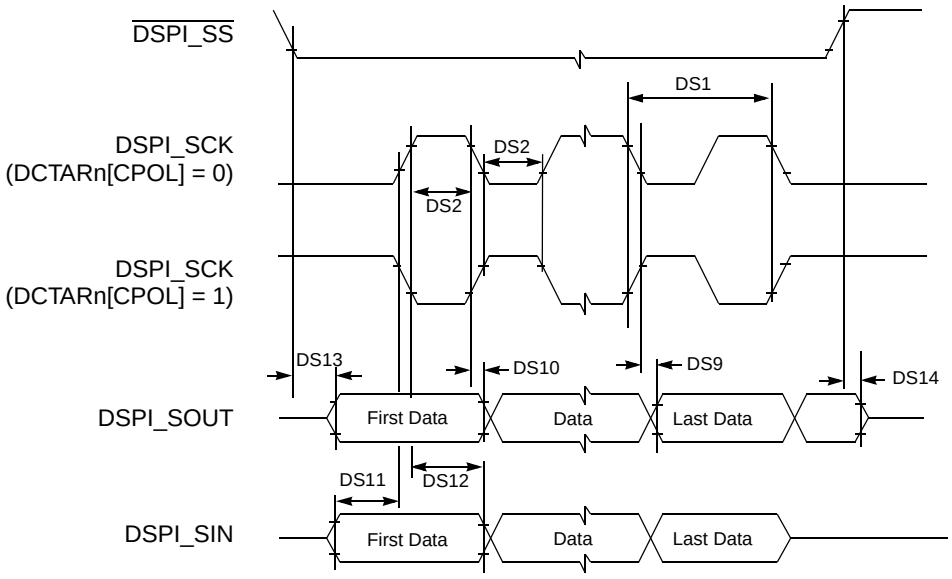


Figure 28. DSPI Classic SPI Timing — Slave Mode

5.16 eSDHC Electrical Specifications

This section describes the electrical information of the eSDHC.

5.16.1 eSDHC Timing

Figure 29 depicts the timing of eSDHC, and Table 29 lists the eSDHC timing characteristics.

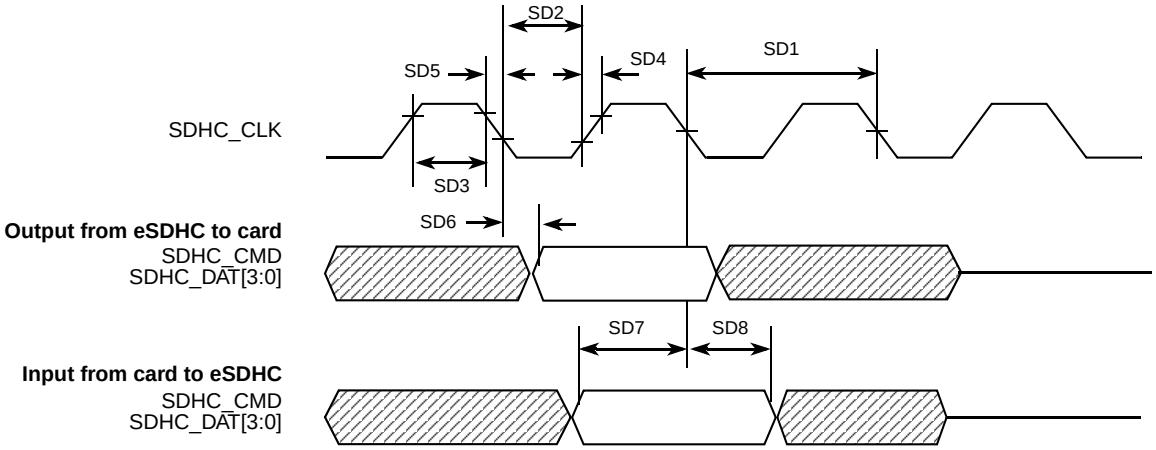


Figure 29. eSDHC Timing

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCIHPF=logic high CODEC_CLK=26MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	260 155 57 15 95 135 190	µS µS µS µS µS µS µS
Filter Group Delay VCIHPF=logic low CODEC_CLK=26MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 150 200	µS µS µS µS
Filter Absolute Group Delay VCIHPF=logic high	f=1.6kHz	—	—	300	µS
Filter Absolute Group Delay VCIHPF=logic low	f=1.6kHz	—	—	235	µS
Out of Band input fold-in spurious	with 0dBm0 input signal from 4.6 kHz to 8.4 kHz	—	—	–50	dB

1 All analog signals are referenced to VAG unless otherwise noted.

2 Power Supply Rejection Ratio is for Longjing IC only. Total PSRR from battery to output is obtained by summing the PSRR from Neptune to the one from the Regulator in Seaweed. It is assumed that the regulators in Seaweed will have a minimum PSRR of 45 dB.

3 For A/D differential input (ADC_P - ADC_M) 0dBm0 = 340mV$_{rms}$.
The codec output will not “foldback” or oscillate if overdriven, but clip.

4 The digital word corresponding to +3dBm0 is ‘0111111111111’b. Therefore if the audio level is set to +3dBm0, any variation in gain could cause large distortion if the digital number exceeds ‘0111111111111’b. For this reason the maximum recommended signal for low distortion is +3dBm0 – (Absolute Gain Error) = +2dBm0.

5 GSM Spec = –64 0dB.

6 This value is a preliminary target. The final number will be specified after obtaining the production statistical data.

7 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

8 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

9 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

Figure 34 and Figure 35 show the filter frequency response for the audio signal for voice coding path. (All filter frequencies increase by 8.1/8.0 if VCLK is selected to generate f_{SYNC}=8.1kHz).

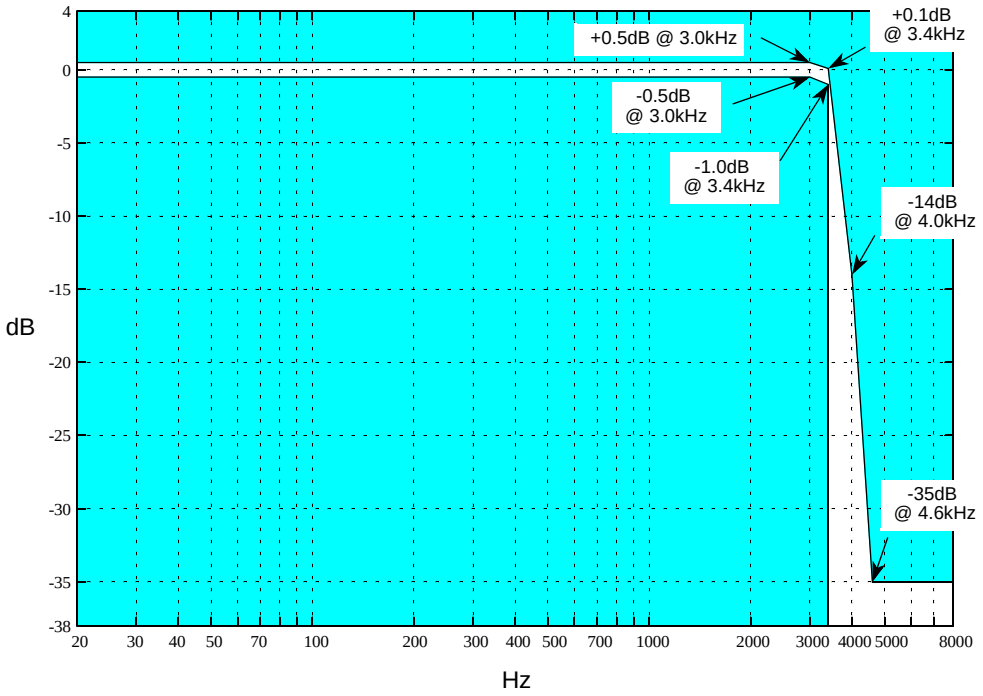


Figure 34. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=0, LPF Alone Without HPF)

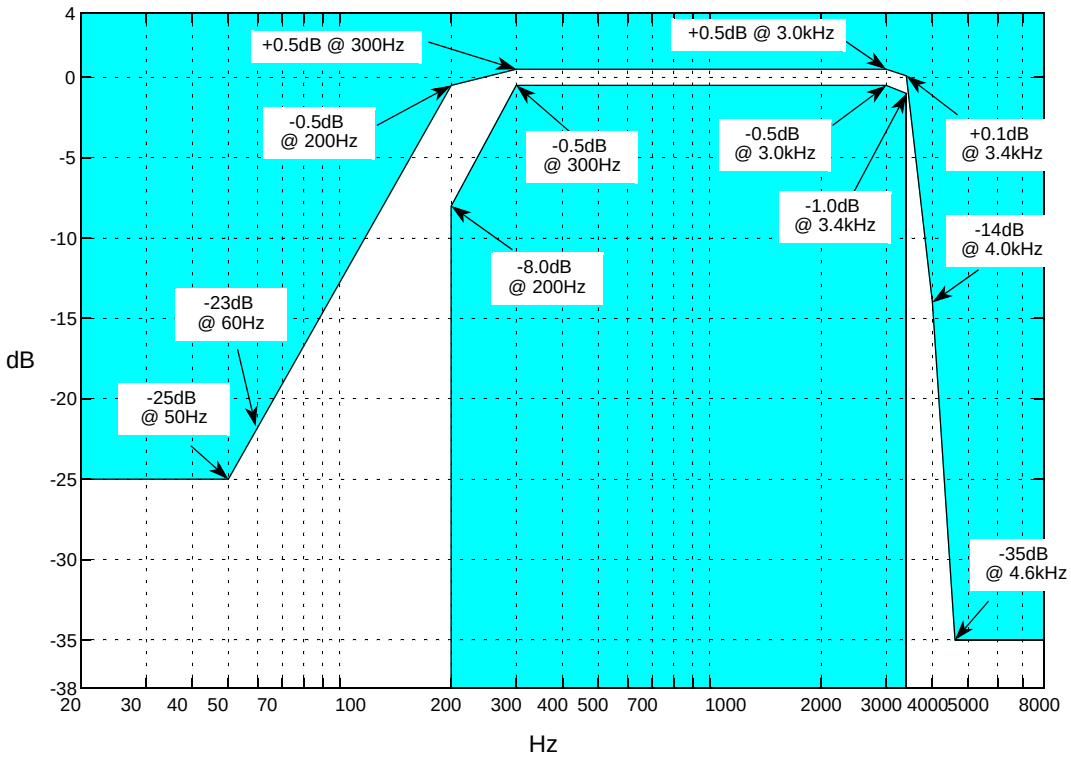


Figure 35. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=1, HPF and LPF Together)

5.19.2 Voice Codec DAC Specifications

Voice-decoding function includes frequency ripple compensation, interpolation, digital-to-analog conversion, and anti-imaging filter. The input signal for the voice-decoding function is in linear 16-bit two's compliment PCM words at an 8 kHz or 8.1 kHz rate. Table 34 shows the voice decoding specifications.

Table 34. Voice Codec DAC Specifications[1]

Parameter	Condition	Min	Typ	Max	Units
Output Level	+3dbm0[2] (clipping level) on an individual differential output pin (CODEC_DACP or CODEC_DACN)	VAG–0.5	—	VAG+0.5	V
Output Source Impedance	10kΩ Load	—	100	—	Ω
Output Power Supply Rejection Ratio	20Hz to 100kHz with 100 mVrms, noise applied to AVDD (CODEC_REGBYP)	50	60	—	dBa
Absolute Gain	0dBm0@1.02kHz	–1.0	—	1.0	dB
Gain vs. Signal	–10dBm0@1.02kHz +3 to –40dBm0 –40 to –50dB –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCOHPF = logic high CODEC_CLK=26 MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	300 200 70 30 95 135 190	µs µs µs µs µs µs µs
Filter Group Delay VCOHPF = logic low CODEC_CLK=26 MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 160 200	µs µs µs µs
Filter Absolute Group Delay VCOHPF = logic high	f=1.6kHz	—	—	350	µs
Filter Absolute Group Delay VCOHPF = logic low	f=1.6kHz	—	—	320	µs

1 All analog signals are referenced to VAG unless otherwise noted. Output is 0dbm0 unless noted.

2 For D/A differential output (CODEC_DACP - CODEC_DACN) 0dBm0 = 500 mV_{rms}.

3 GSM Spec = –64.

4 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

5 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

6 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

Figure 36 and Figure 37 show the filter frequency response for the audio signal for voice decoding. The requirements for the decoding path at 3.4 kHz are slightly different from the coding path. (All filter frequencies increase by 8.1/8.0 if VCLK is selected to generate f_{SYNC} = 8.1 kHz).

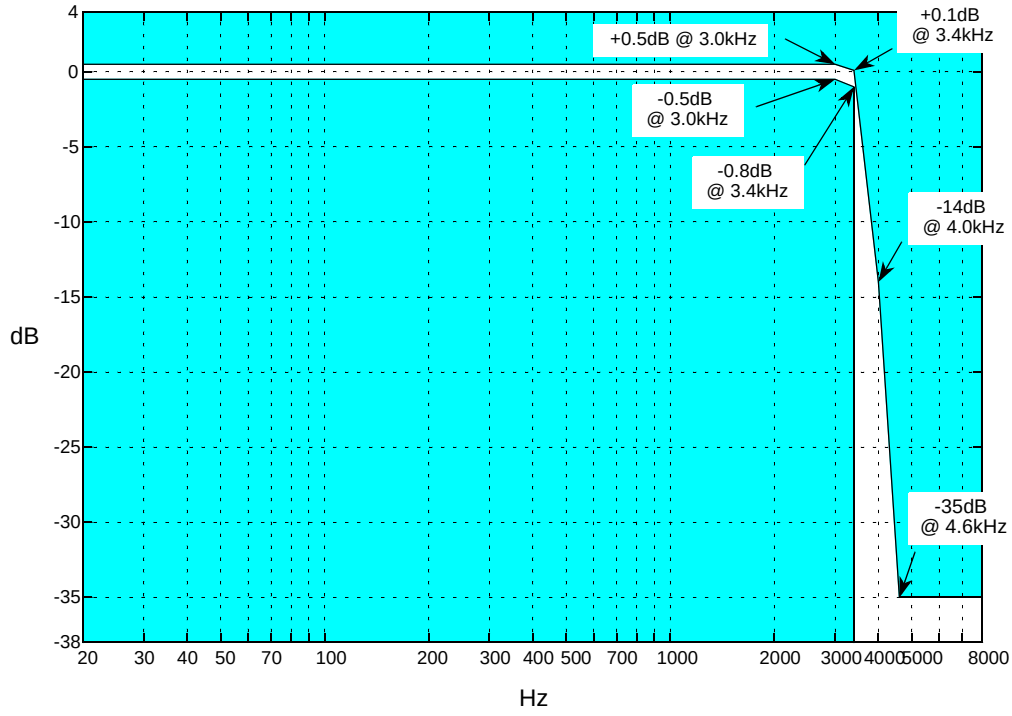


Figure 36. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=0, LPF Alone Without HPF)

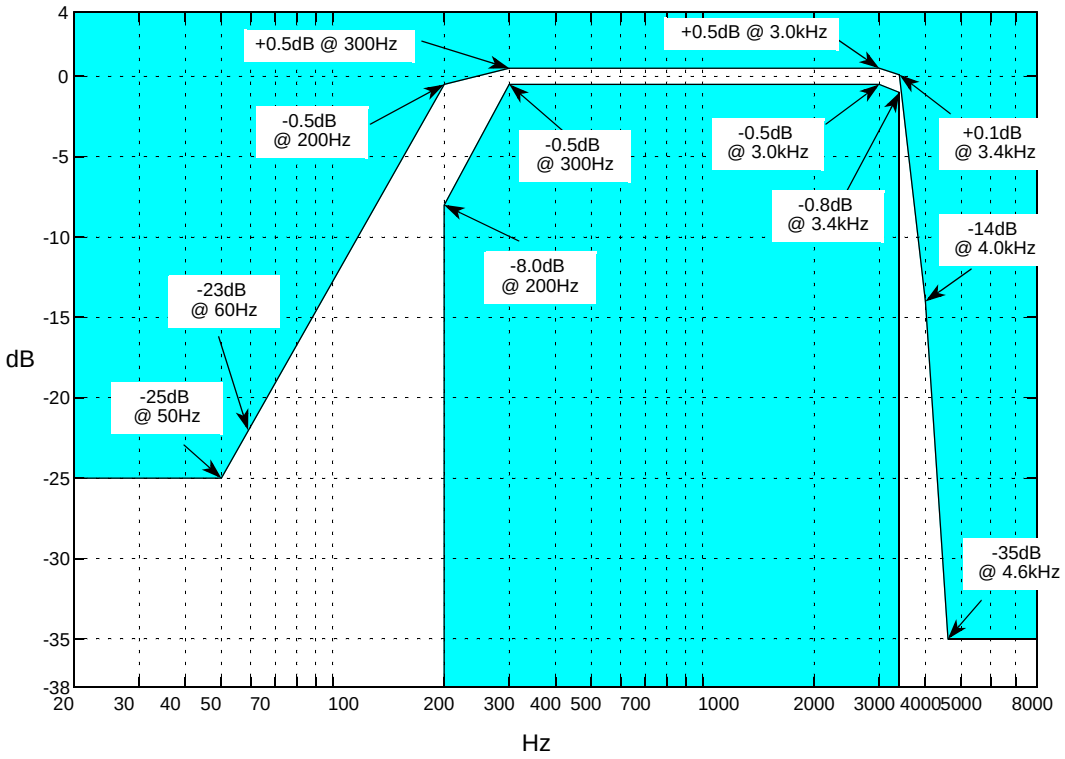


Figure 37. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=1, HPF and LPF Together)

5.20 Integrated Amplifiers

5.20.1 Speaker Amplifier

The speaker amplifier boosts the power from the DAC and drives the speaker. It also provides analog volume control to optimize the noise performance of the entire channel. Table 35 shows the specifications for the speaker amplifier.

Table 35. Speaker Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	μA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 4Ω		—	600	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 4Ω, F_{in} = 1kHz	Full Power, 500mW	—	0.050	—	%
		Half Power, 250mW	—	0.050	—	
	Gain = 0dB, R_L = 4Ω, F_{in} = 4kHz	Full Power, 500mW	—	0.1	—	
		Half Power, 250mW	—	0.1	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	μV

5.20.3 Headphone Amplifier

The headphone amplifier boosts the power from the DAC and drives the headphone. It also provides analog volume control to optimize the noise performance of the entire channel. Table 37 shows the specifications for the microphone amplifier.

Table 37. Headphone Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	600	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 16Ω		—	40	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 16Ω, BW = 200Hz – 4kHz	Full Power, 31.25mW	—	0.05	—	%
		Half Power, 16.5mW	—	0.05	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 0.7V_{RMS} , BW = 20Hz – 20kHz		—	93	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	150	—	mA
Gain Error	Gain = –45, –21, –12, –6, –2, 0 dB		—	±0.5	—	dB

5.20.4 Microphone Amplifier

The microphone amplifier boosts the signal from the microphone and provides it to the ADC. The gain control present in the microphone amplifier helps in optimizing the noise performance of the entire channel. Table 38 shows the specifications for the microphone amplifier.

Table 38. Microphone Amplifier Specifications

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current		—	500	—	µA
Shutdown Current		—	TBD	—	
Input Reference Offset		—	2	5	mV

Table 38. Microphone Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Total Harmonic Distortion (THD)	Gain = 0dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	%
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 0dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
Integrated Output Noise	BW = 20Hz – 20kHz	Gain = 0dB	—	12	—	µV
		Gain = 20dB	—	40	—	
Signal to Noise Ratio (SNR)	V_{OUT} = 0.5V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	92.4	—	dB
		Gain = 20dB	—	81.9	—	
THD plus Noise	V_{OUT} = 0.35V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	80	—	dB
		Gain = 20dB	—	80	—	
Power Supply Rejection Ratio	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 1kHz	—	60	—	dB
		f = 4kHz	—	60	—	
Commom Mode Rejection Ratio	Gain = 0dB, V_{ripple} = 100mV_{pp}	f = 1kHz	—	50	—	dB
		f = 4kHz	—	50	—	
Gain Error	Gain = 0, 6, 9.56, 15.56, 20, 24, 29.56, 39.9 dB		—	±0.5	—	dB
Input Impedance	Depends on the Gain Setting		1.5	—	24.0	kΩ

5.21 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns

Table 39. JTAG and Boundary Scan Timing (continued)

Num	Characteristics[1]	Symbol	Min	Max	Unit
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

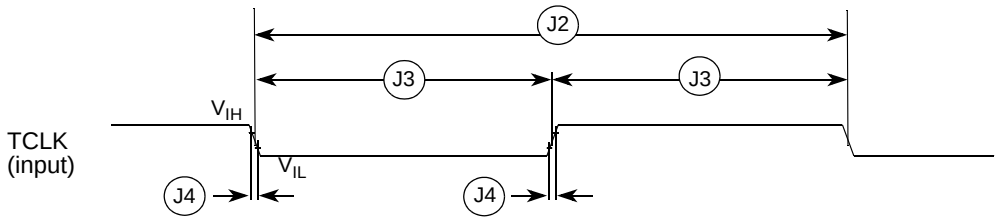


Figure 38. Test Clock Input Timing

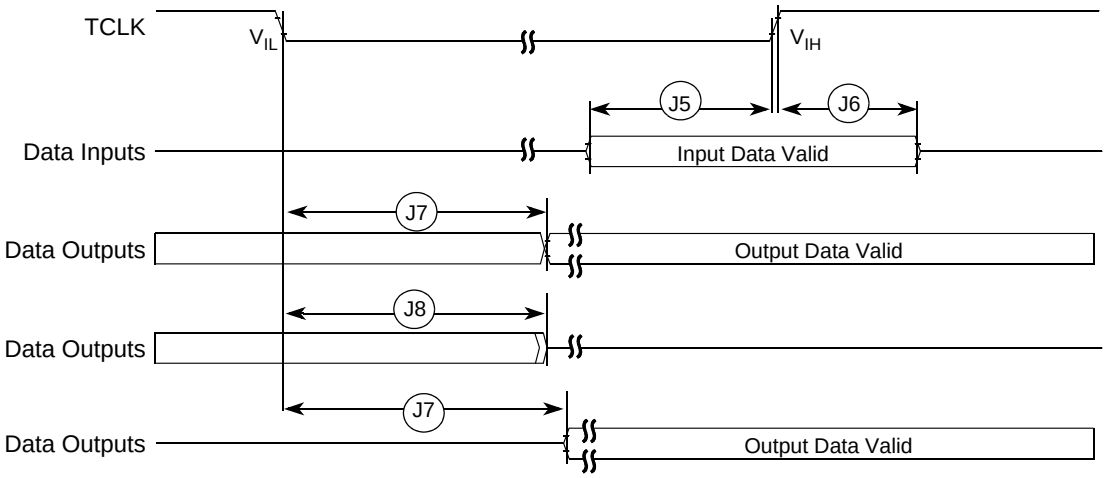


Figure 39. Boundary Scan (JTAG) Timing

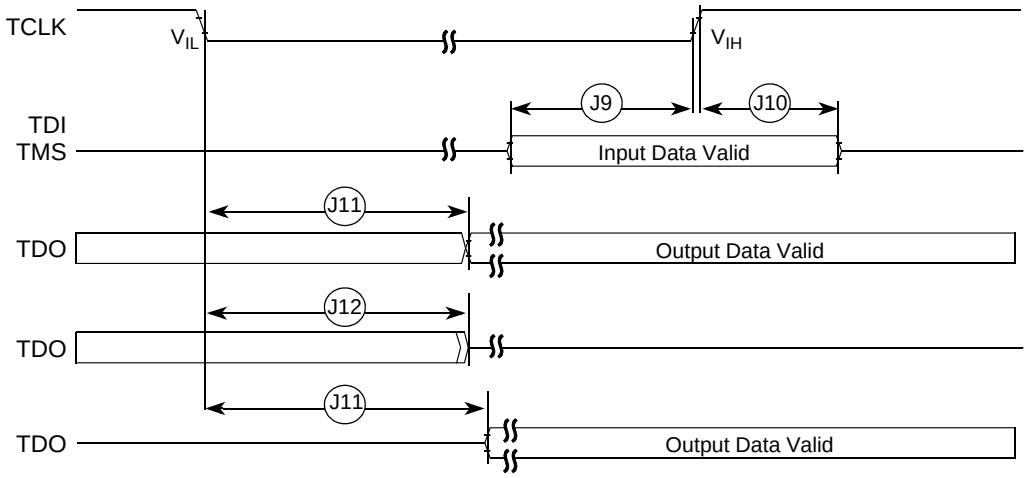


Figure 40. Test Access Port Timing

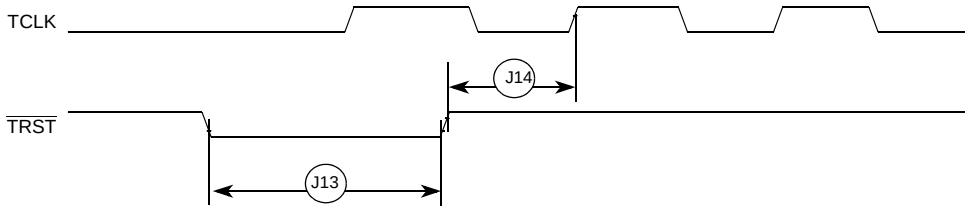


Figure 41. TRST Timing

5.22 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 42.

Table 40. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1.5	1.5	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

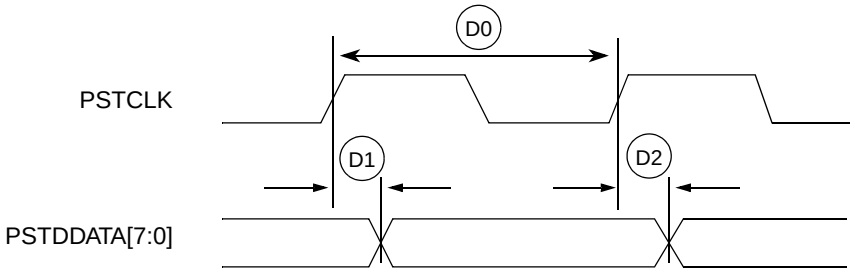


Figure 42. Real-Time Trace AC Timing

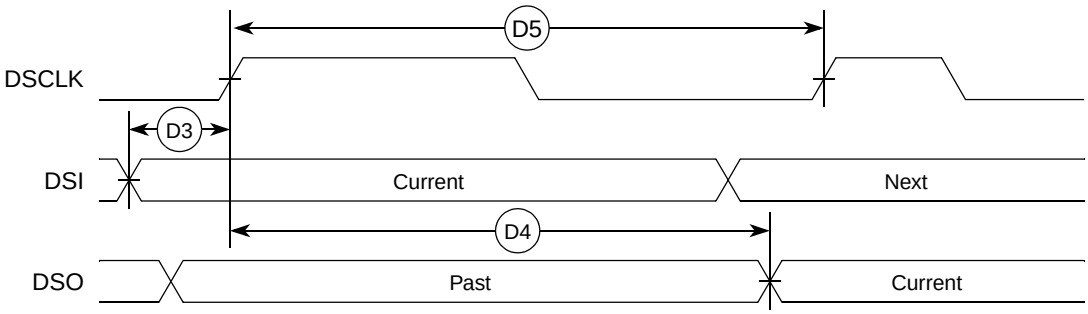


Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.