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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53011cqt240

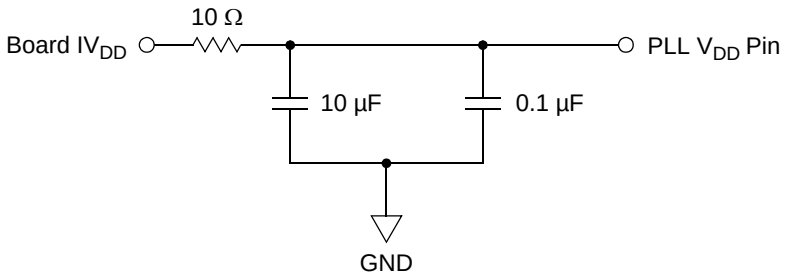

Figure 1. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

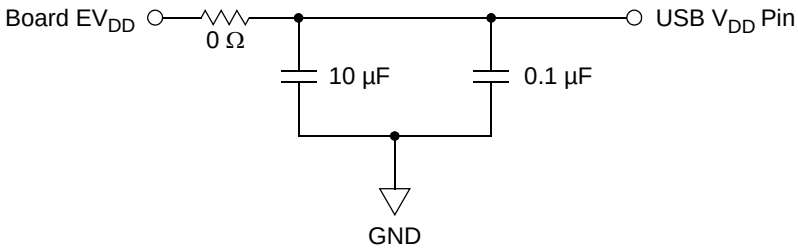

Figure 2. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing

Figure 3 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic / core V_{DD} (IV_{DD}). The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

3.4 Power Consumption Specifications

Estimated maximum RUN mode power consumption measurements are shown in the below figure.

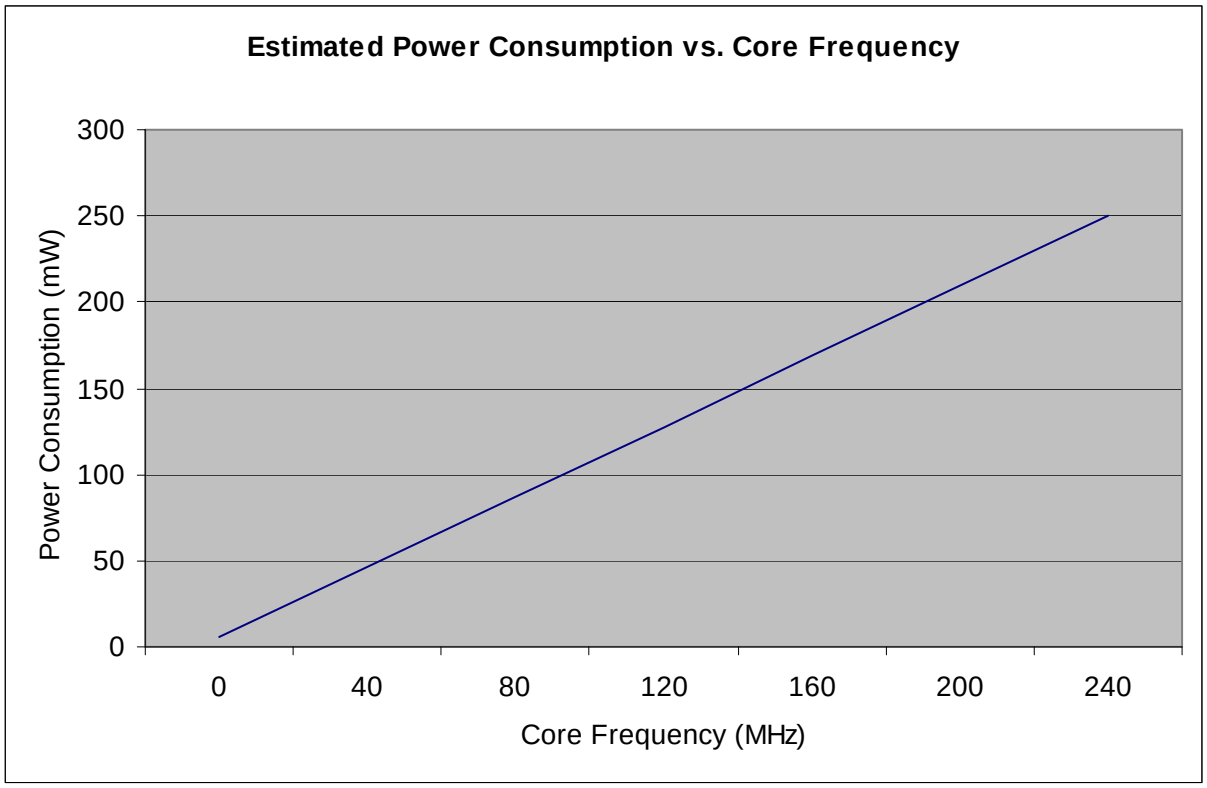

Figure 4. Estimated Maximum RUN Mode Power Consumption

Table 3 lists estimated maximum power and current consumption for the device in various operating modes.

Table 3. Estimated Maximum Power Consumption Specifications

Characteristic	Symbol	Typical	Max	Unit
Run Mode — Total Power Dissipation Static Dynamic		— — —	TBD TBD TBD	mW mW mW
Core Operating Supply Current [1] Run Mode	I_{DD}	—	82.9	mA
Pad Operating Supply Current Run Mode (application dependent) Wait Mode Stop Mode	EI_{DD}	— — —	TBD TBD TBD	mA mA mA

1 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

Table 4. Current Measurementas at Different VCO vs. Core Frequencies

Stop Mode	480VCO, 240MHz core	240VCO, 120MHz core	480VCO, 120MHz core	480VCO, 48MHz core	Limp Mode, 20HMHz crystal
Executing	55.3mA	28.36mA	30.00mA	13.6mA	5.90mA
Run	39.5mA	20.3mA	22.02mA	10.29mA	4.42mA
Wait	16.28mA	8.53mA	10.23mA	5.53mA	2.43mA
Doze	16.19mA	8.53mA	10.18mA	5.55mA	2.41mA
Stop(0)	8.41mA	4.60mA	6.29mA	3.90mA	1.78mA
Stop(1)	8.13mA	4.48mA	6.15mA	3.88mA	1.77mA
Stop(2)	1.83mA	1.86mA	1.87mA	1.82mA	1.76mA
Stop(3)	0.65mA	0.66mA	0.67mA	0.67mA	0.65mA

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5301*x* pins grouped by function. The “Dir” column is the direction for the primary function of the pin only. Refer to Section 4.2, “Pinout—208 LQFP,” and Section 4.3, “Pinout–256 MAPBGA,” for package diagrams. For a more detailed discussion of the MCF3xx*x* signals, consult the *MCF5301x Reference Manual* (MCF53017RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5301*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	41	M3
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	42	N1
Clock								
EXTAL	—	—	—	—	I	EVDD	49	T2
XTAL	—	—	—	U[3]	O	EVDD	50	T3
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	55, 17	J5, G5
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[3:2]	—	—	O	SDVDD	115, 114	P16, N16
FB_A[21:16]	—	—	—	—	O	SDVDD	113–108	R16, N14, N15, P15-13
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	107, 106	R15, R14
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	105–103	N13, R12, R13
FB_A10	—	—	—	—	O	SDVDD	100	N12
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	99–97 95–89	P12, T14, T15, R11, P11, N11, T13, R10, T11, T12
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	208–198, 57–62, 64, 65	B3, A2, D6, C5, B4, A3, B5, C6, D12, C14, B14, C13, D11, B13, A14, A13
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	182–189, 177–170	B9, A9, A8, D7, B8, C8, D8, B7, C10, A10, B10, D10, C11, A11, B11, A12
FB_CLK	—	—	—	—	O	SDVDD	153	D13
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	197, 166, 179, 178	A4, B12, C9, D9
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	—	O	SDVDD	—	B6, C7
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	5	D2
$\overline{\text{FB\_CS0}}$	PCS0	$\overline{\text{FB\_CS4}}$	—	—	O	SDVDD	6	C2
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	1	D4
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	3	B2
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	2	C3
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	4	D3
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	206	C4

4.3 Pinout–256 MAPBGA

The pinout for the MCF53014, MCF53015, MCF53016, and MCF53017 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_D 30	FB_D 26	FB_BE/ BWE3	SD_ DQS1	SD_ CLK	SD_ CLK	FB_D 13	FB_D 14	FB_D 6	FB_D 2	FB_D 0	FB_D 16	FB_D 17	SD_CS	VSS	A
B	USBH_ DM	FB_TA	FB_D 31	FB_D 27	FB_D 25	FB_CS5	FB_D 8	FB_D 11	FB_D 15	FB_D 5	FB_D 1	FB_BE/ BWE2	FB_D 18	FB_D 21	SD_ CKE	USBO_ DP	B
C	USBH_ DP	FB_CS0	FB_R/W	SD_A10	FB_D 28	FB_D 24	FB_CS4	FB_D 10	FB_BE/ BWE1	FB_D 7	FB_D 3	SD_ DQS2	FB_D 20	FB_D 22	SD_ RAS	USBO_ DM	C
D	IRQ04	FB_CS1	FB_TS	FB_OE	SD_SDR _DQS	FB_D 29	FB_D 12	FB_D 9	FB_BE/ BWE0	FB_D 4	FB_D 19	FB_D 23	FB_CLK	SD_ WE	SD_ CAS	SIM1_ VEN	D
E	RMII1_ MDC	U2RXD	T2IN	IRQ07	SDVDD	SDVDD	VDD_ USBO	VDD_ USBH	IVDD	SDVDD	SDVDD	SDVDD	SIM1_ RST	SIM1_ DATA	SIM1_ PD	DSPI_ SIN	E
F	RMII1_ MDIO	U2TXD	T3IN	IRQ01	EVDD	SDVDD	SDVDD	IVDD	IVDD	SDVDD	SDVDD	TEST	SIM1_ CLK	DSPI_ PCS1	DSPI_ SOUT	SIM0_ RST	F
G	U0TXD	U0RXD	U0RTS	U0CTS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	DSPI_ PCS0	RMII0_ MDC	RMII0_ MDIO	RMII0_ CRSDV	G
H	IRQ1 DEBUG7	IRQ1 DEBUG4	IRQ1 DEBUG5	IRQ1 DEBUG6	IVDD	IVDD	VSS	VSS	VSS	VSS	IVDD	IVDD	DSPI_ SCK	IRQ1 DEBUG2	RMII0_ RXD1	RMII0_ RXD0	H
J	IRQ1 FEC7	IRQ1 FEC6	IRQ1 FEC4	IRQ1 FEC3	BOOT MOD1	IVDD	VSS	VSS	VSS	VSS	IVDD	EVDD	IRQ1 DEBUG0	RMII0_ TXD0	RMII0_ TXD1	RMII0_ RXER	J
K	IRQ1 FEC2	IRQ1 FEC1	I2C_ SDA	IRQ1 FEC5	NC	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	T1IN	IRQ1 DEBUG3	IRQ1 DEBUG1	RMII0_ TXEN	K
L	IRQ1 FEC0	VSTBY_ SRAM	SIM0_ DATA	VSTBY_ RTC	EVDD	EVDD	EVDD	IVDD	IVDD	EVDD	EVDD	EVDD	IRQ06	SIM0_ PD	TRST	T0IN	L
M	I2C_ SCL	SIM0_ VEN	RESET	VDD_ OSC_A_ PLL	EVDD	EVDD	EVDD	JTAG_ EN	VDD_ EPM	NC	NC	EVDD	NC	TMS	TDO	SIM0_ CLK	M
N	RST OUT	DSPI_ PCS2	SSI_ RXD	SDHC_ DAT3	SDHC_ DAT0	SDHC_ DAT1	CODEC _VAG	AVDD_ CODEC	CODEC _BGR VREF	VSS_ CODEC	FB_A4	FB_A10	FB_A13	FB_A20	FB_A19	FB_A22	N
P	RTC_ EXTAL	DSPI_ PCS3	SSI_ TXD	SSI_ MCLK	SSI_ BCLK	CODEC _REG BYP	CODEC _REFP	CODEC _REFN	CODEC _ADCP	CODEC _ADCN	FB_A5	FB_A9	FB_A16	FB_A17	FB_A18	FB_A23	P
R	RTC_ XTAL	SSI_FS	SDHC_ CLK	SDHC_ CMD	SDHC_ DAT2	CODEC _DACP	CODEC _DACN	AMP_ HP OUT	AMP_ HP DUMMY	FB_A2	FB_A6	FB_A12	FB_A11	FB_A14	FB_A15	FB_A21	R
T	VSS	EXTAL	XTAL	TDI	TCLK	AVSS_ SPKR_ HDST	AMP_ SPKRP	AVDD_ SPKR	AMP_ SPKRN	AVSS_ SPKR_ HP	FB_A1	FB_A0	FB_A3	FB_A8	FB_A7	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7. MCF53014, MCF53015, MCF53016, and MCF53017 Pinout (256 MAPBGA)

5 Preliminary Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5301*x* microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	–0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	–0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	–0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	–0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	–0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L – T_H)	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	208 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	36[1,2]	38[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	32[1,2]	33[1,2]	°C/W
Junction to board		θ_{JB}	25[3]	29[3]	°C/W
Junction to case		θ_{JC}	14[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	^{0}C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

Chip-select, $\overline{\text{FB\_CS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is 1‘compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	80	Mhz	$f_{sys/3}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	12.5	—	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0] and $\overline{\text{OE}}$)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0], and $\overline{\text{OE}}$)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	t_{CIFBCH}	0	—	ns	

1 Timing for chip selects only applies to the $\overline{\text{FB\_CS}}$[5:0] signals. Please see Section 5.7.2, “DDR SDRAM AC Timing Characteristics” for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *MCF5301x Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

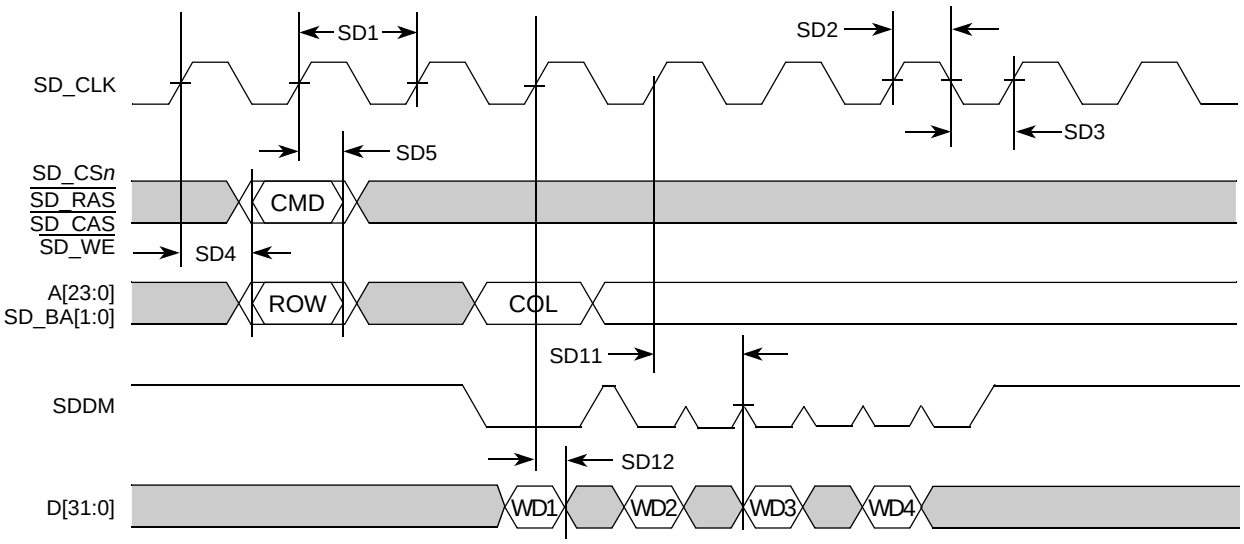

Figure 13. SDR Write Timing

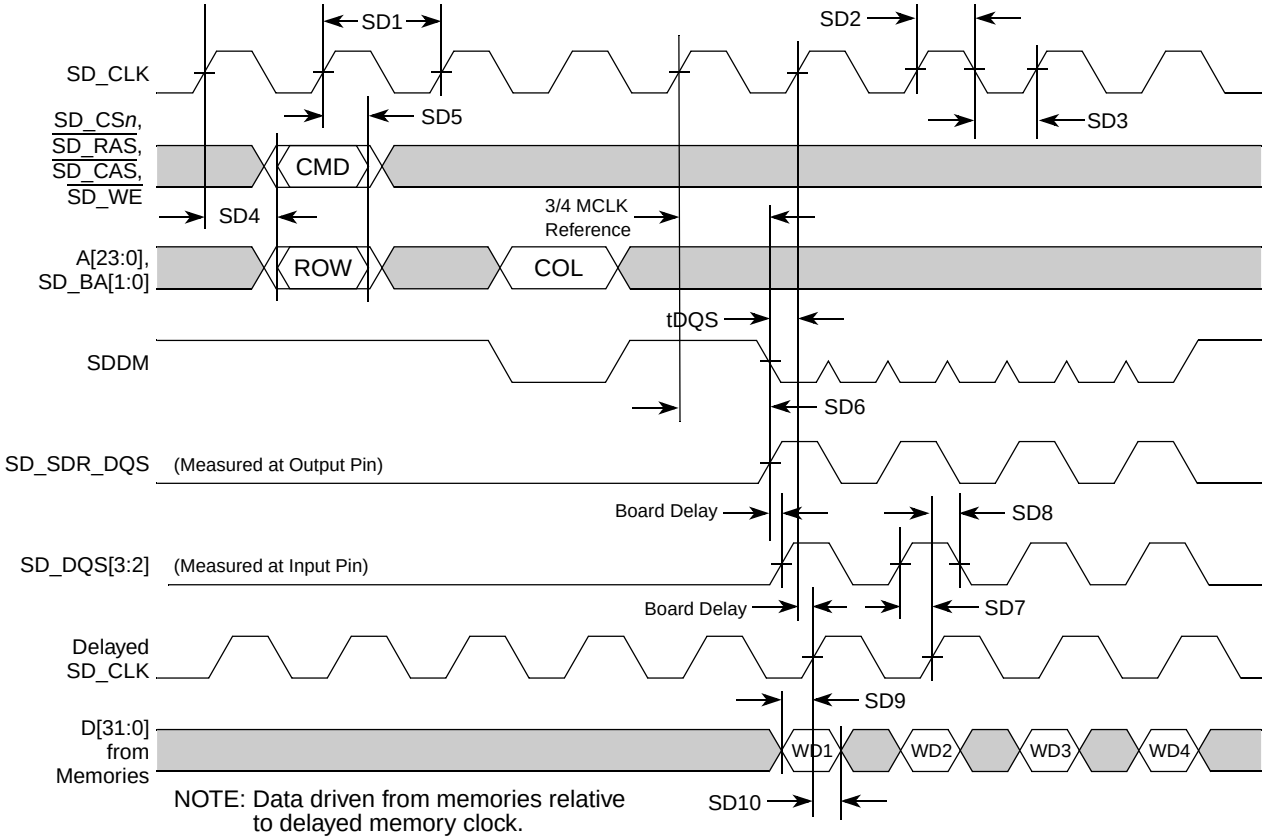

Figure 14. SDR Read Timing

5.7.2 DDR SDRAM AC Timing Characteristics

When the SDRAM controller is configured for DDR SDRAM, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design.

Table 14. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation	t_{DDCK}	50	80	Mhz	1
DD1	Clock Period	t_{DDSK}	12.5	20	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] Output Hold	$t_{SDCHACI}$	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}	—	1.25	SD_CLK	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK	
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK	
DD14	DQS output write preamble width	t_{DQWPRE}	0.25	—	SD_CLK	
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK	

1 The frequency of operation is either 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.

2 SD_CLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

5 This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. SD_D[31:24] is relative to SD_DQS3, SD_D[23:16] is relative to SD_DQS2, SD_D[15:8] is relative to SD_DQS1, and SD_D[7:0] is relative SD_DQS0.

6 The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.

7 This specification relates to the required hold time of today's DDR memories. SD_D[31:24] is relative to SD_DQS3, SD_D[23:16] is relative to SD_DQS2, SD_D[15:8] is relative to SD_DQS1, and SD_D[7:0] is relative SD_DQS0.

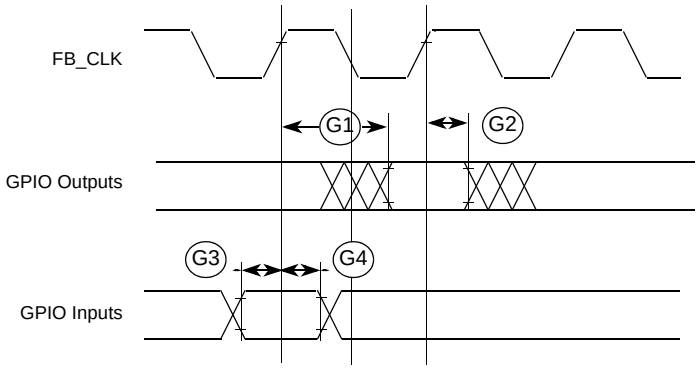

Figure 18. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 16. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

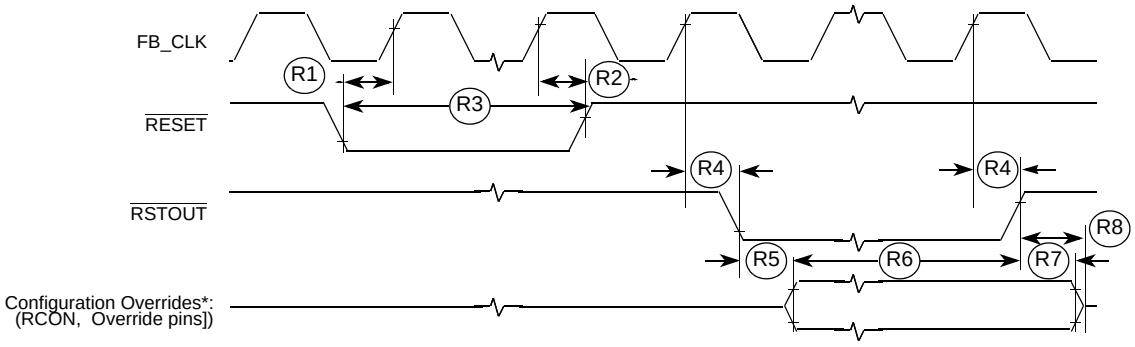

Figure 19. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5301x Reference Manual* for more information.

5.10 USB On-The-Go

The MCF53017 device is compliant with industry standard USB 2.0 specification.

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 17. SSI Timing - Master Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$8 \times t_{SYS}$	—	ns	[2]
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	[3]
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		–2	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 18. SSI Timing — Slave Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25pF.

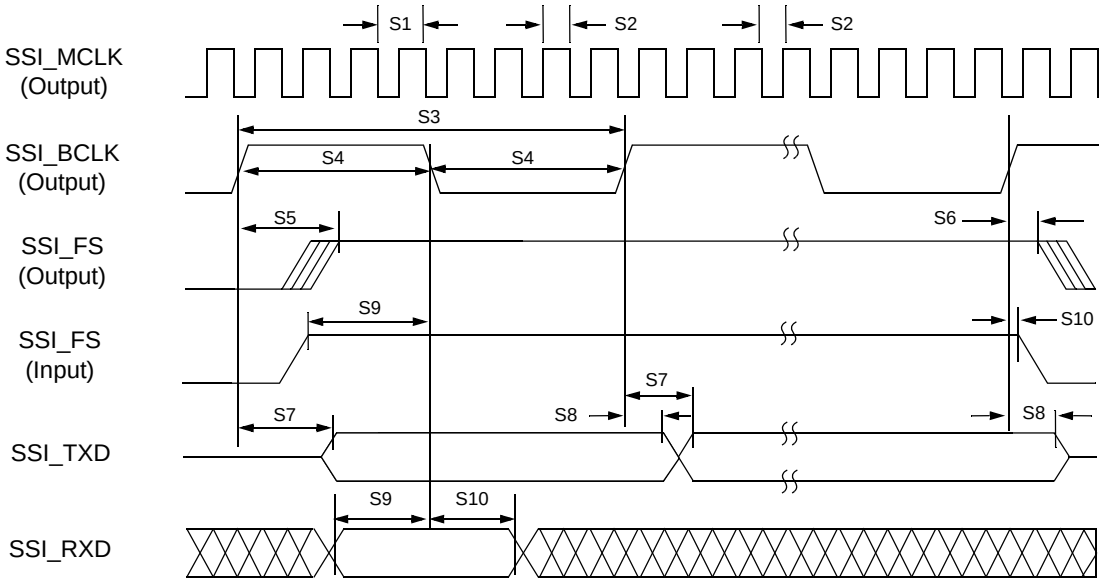

Figure 20. SSI Timing — Master Modes

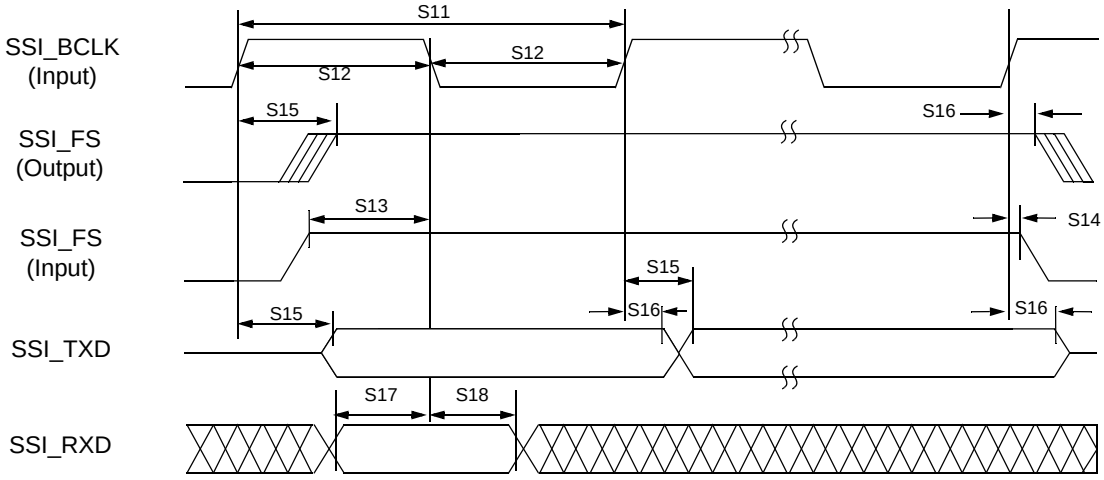

Figure 21. SSI Timing — Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 19 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 19. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 19. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 20 lists specifications for the I²C output timing parameters shown in Figure 22.

Table 20. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 20. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 20 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 22 shows timing for the values in Table 20 and Table 19.

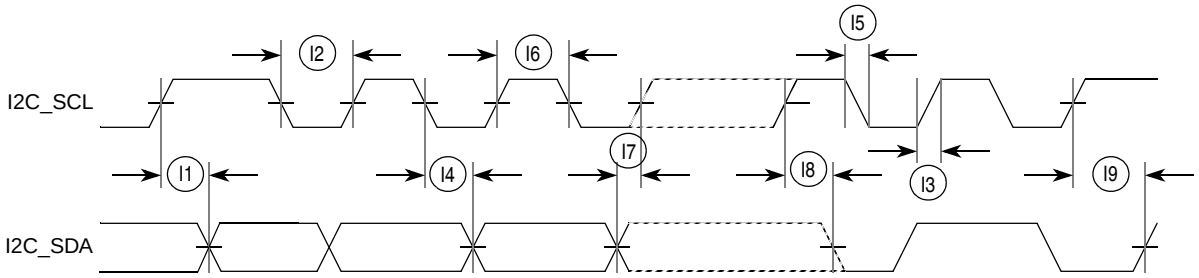

Figure 22. I²C Input/Output Timings

Table 27. eSDHC Interfacde Timing Specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input / Card Outputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	4	—	ns
SD8	eSDHC Input Hold Time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.

4 In card identification mode, card clock must be 100 kHz – 400 kHz, voltage ranges from 2.7 to 3.6 V.

5.16.2 eSDHC Electrical DC Characterisics

Table 28 lists the eSDHC electrical DC characteristics.

Table 28. MMC/SD Interface Electrical Specifications

Num	Parameter	Design Value	Min	Max	Unit	Condition/Remark
General						
1	Peak Voltage on All Lines	—	–0.3	V_{DD} + 0.3	V	
All Inputs						
2	Input Leakage Current	—	–10	10	uA	
All Outputs						
3	Output Leakage Current	—	–10	10	uA	
Power Supply						
4	Supply Voltage (HV card)	3.1	2.7	3.6	V	for high voltage cards, must provide this voltage for card initialization
5	Supply Voltage (LV card)	1.8	1.65	1.95	V	for low voltage cards

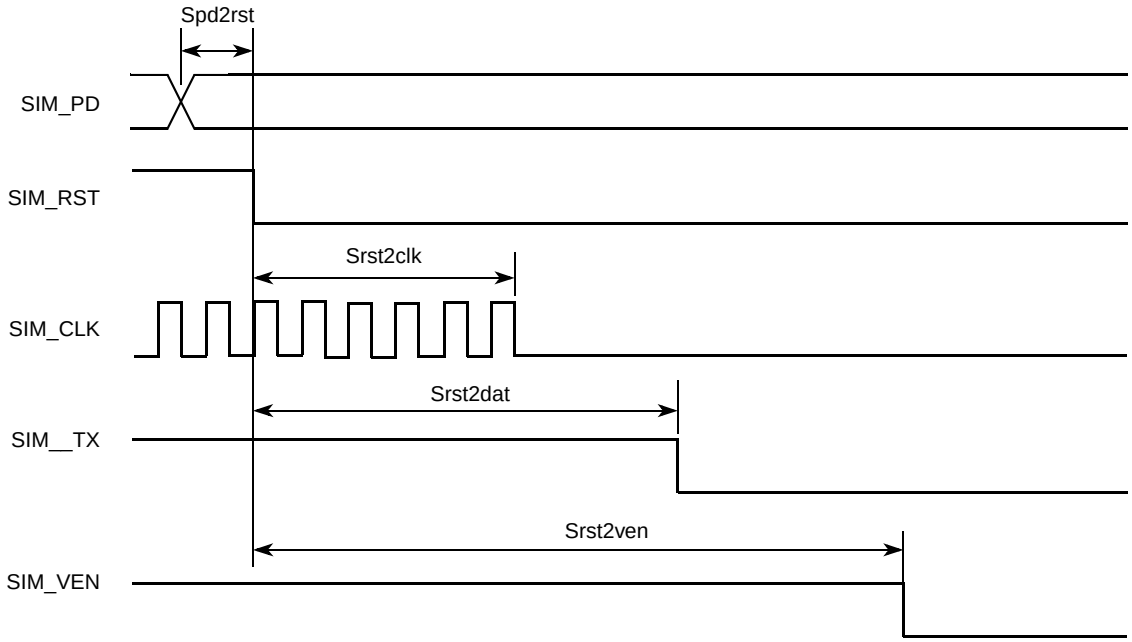

Figure 33. SmartCard Interface Power-Down AC Timing

5.18 IIM/Fusebox Electrical Specifications

Table 31. IIM/Fusebox Timing Characteristics

Num	Description	Symbol	Min	Max	Unit
1	Program time for eFuse[1]	$t_{program}$	125	—	µs

[1] The program length is defined by the value defined in IIM_FCR[PRG_LENGTH] of the IIM module. The value to program is based on a 32 kHz clock source (4 ÷ 32 kHz = 125 µs)

5.19 Voice Codec

The voice codec function is analog-to-digital and digital-to-analog conversion of the voice signal. The following section contains detailed electrical specifications for the analog and digital parts' performance. The voice codec is powered down when not enabled for power consumption.

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCIHPF=logic high CODEC_CLK=26MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	260 155 57 15 95 135 190	µS µS µS µS µS µS µS
Filter Group Delay VCIHPF=logic low CODEC_CLK=26MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 150 200	µS µS µS µS
Filter Absolute Group Delay VCIHPF=logic high	f=1.6kHz	—	—	300	µS
Filter Absolute Group Delay VCIHPF=logic low	f=1.6kHz	—	—	235	µS
Out of Band input fold-in spurious	with 0dBm0 input signal from 4.6 kHz to 8.4 kHz	—	—	–50	dB

1 All analog signals are referenced to VAG unless otherwise noted.

2 Power Supply Rejection Ratio is for Longjing IC only. Total PSRR from battery to output is obtained by summing the PSRR from Neptune to the one from the Regulator in Seaweed. It is assumed that the regulators in Seaweed will have a minimum PSRR of 45 dB.

3 For A/D differential input (ADC_P - ADC_M) 0dBm0 = 340mV$_{rms}$.
The codec output will not “foldback” or oscillate if overdriven, but clip.

4 The digital word corresponding to +3dBm0 is ‘0111111111111’b. Therefore if the audio level is set to +3dBm0, any variation in gain could cause large distortion if the digital number exceeds ‘0111111111111’b. For this reason the maximum recommended signal for low distortion is +3dBm0 – (Absolute Gain Error) = +2dBm0.

5 GSM Spec = –64 0dB.

6 This value is a preliminary target. The final number will be specified after obtaining the production statistical data.

7 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

8 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

9 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

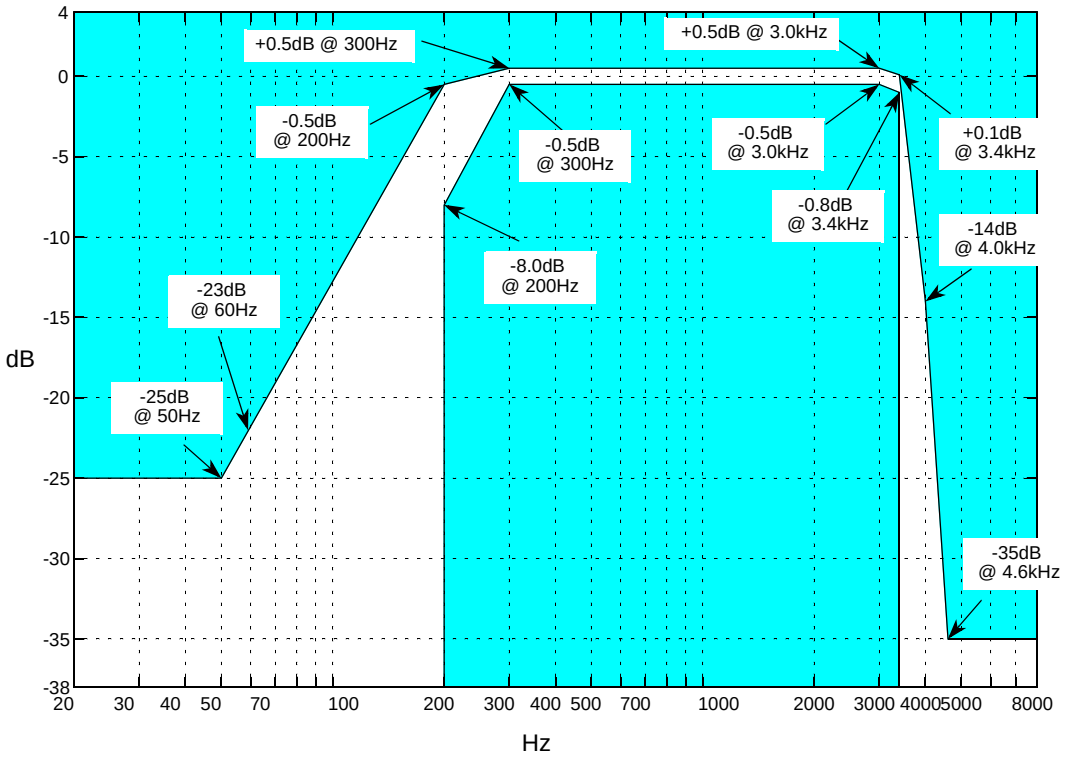

Figure 37. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=1, HPF and LPF Together)

5.20 Integrated Amplifiers

5.20.1 Speaker Amplifier

The speaker amplifier boosts the power from the DAC and drives the speaker. It also provides analog volume control to optimize the noise performance of the entire channel. Table 35 shows the specifications for the speaker amplifier.

Table 35. Speaker Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	μA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 4Ω		—	600	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 4Ω, F_{in} = 1kHz	Full Power, 500mW	—	0.050	—	%
		Half Power, 250mW	—	0.050	—	
	Gain = 0dB, R_L = 4Ω, F_{in} = 4kHz	Full Power, 500mW	—	0.1	—	
		Half Power, 250mW	—	0.1	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	μV

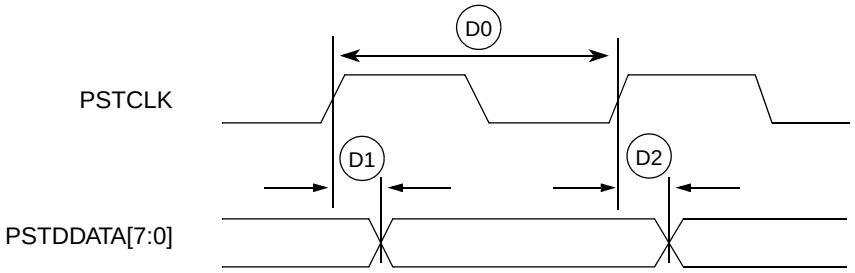

Figure 42. Real-Time Trace AC Timing

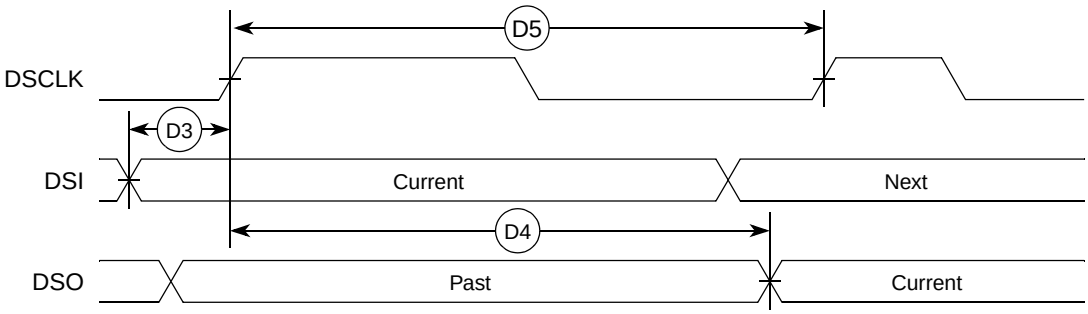

Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

8 Revision History

Table 42 summarizes revisions to this document.

Table 42. Revision History

Revision	Date	Location	Changes
3	12 Aug 2009	—	Initial public revision
4	10 Feb 2010	Table 8 Table 41	Added thermal characteristics for 208LQFP package Added 208LQFP case outline number
5	3 Mar 2010	Table 2	Added non-J suffixed part numbers for the 256MAPBGA package

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