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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	61
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53012cqt240

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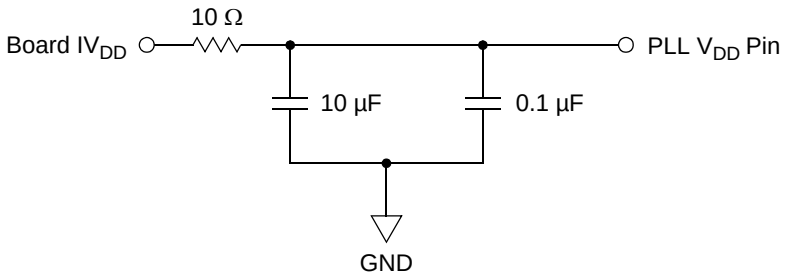

Figure 1. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

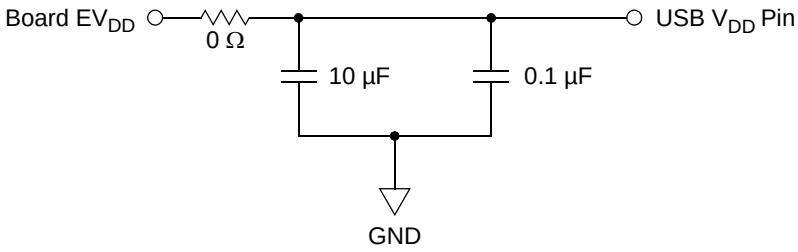

Figure 2. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing

Figure 3 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic / core V_{DD} (IV_{DD}). The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	154	D15
SD_CKE	—	—	—	—	O	SDVDD	151	B15
SD_CLK	—	—	—	—	O	SDVDD	190	A7
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	191	A6
$\overline{\text{SD\_CS0}}$	—	—	—	—	O	SDVDD	155	A15
SD_DQS[1:0]	—	—	—	—	O	SDVDD	196, 167	C12, A5
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	152	C15
SD_SDR_DQS	—	—	—	—	I	SDVDD	207	D5
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	150	D14
External Interrupts Port 1[4,5]								
$\overline{\text{IRQ1DEBUG}}$[7:4]	PIRQ1DEBUG [7:4]	DDATA[3:0]	—	—	I	EVDD	—	H1, H4-2
$\overline{\text{IRQ1DEBUG}}$[3:0]	PIRQ1DEBUG [3:0]	PST[3:0]	—	—	I	EVDD	—	K14, H14, K15, J13
$\overline{\text{IRQ1FEC7}}$	PIRQ1FEC7	RMII1_CRS_DV	MII0_CRS	—	I	EVDD	29	J1
$\overline{\text{IRQ1FEC6}}$	PIRQ1FEC6	RMII1_RXER	MII0_RXCLK	—	I	EVDD	30	J2
$\overline{\text{IRQ1FEC5}}$	PIRQ1FEC5	RMII1_TXEN	MII0_TXCLK	—	I	EVDD	31	K4
$\overline{\text{IRQ1FEC4}}$	PIRQ1FEC4	RMII1_REF_CLK	—	D	I	EVDD	32	J3
$\overline{\text{IRQ1FEC}}$[3:2]	PIRQ1FEC[3:2]	RMII1_RXD[1:0]	MII0_RXD[3:2]	—	I	EVDD	33, 34	J4, K1
$\overline{\text{IRQ1FEC}}$[1:0]	PIRQ1FEC[1:0]	RMII1_TXD[1:0]	MII0_TXD[3:2]	—	I	EVDD	35, 36	K2, L1
External Interrupts Port 0[5]								
$\overline{\text{IRQ07}}$	PIRQ07	—	—	U	I	EVDD	10	E4
$\overline{\text{IRQ06}}$	PIRQ06	—	USB_CLKIN	U	I	EVDD	—	L13
$\overline{\text{IRQ04}}$	PIRQ04	$\overline{\text{DREQ0}}$	—	U	I	EVDD	19	D1
$\overline{\text{IRQ01}}$	PIRQ01	$\overline{\text{DREQ1}}$	—	U	I	EVDD	11	F4
Enhanced Secure Digital Host Controller								
SDHC_DAT3	PSDHC5	—	—	UD	I/O	EVDD	60	N4
SDHC_DAT[2:0]	PSDHC[4:2]	—	—	U	I/O	EVDD	61–63	R5, N6, N5
SDHC_CMD	PSDHC1	—	—	U	I/O	EVDD	59	R4
SDHC_CLK	PSDHC0	—	—	—	O	EVDD	58	R3

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Codec								
CODEC_ADCN	—	AMP_MICN	—	—	I		85	P10
CODEC_ADCP	—	AMP_MICP	—	—	I		84	P9
CODEC_BGRVREF	—	—	—	—	I		86	N9
CODEC_DACN	—	AMP_HSN	—	—	O		75	R7
CODEC_DACP	—	AMP_HSP	—	—	O		67	R6
CODEC_REGBYP	—	—	—	—	I		81	P6
CODEC_REFN	—	—	—	—	I		79	P8
CODEC_REFP	—	—	—	—	I		78	P7
CODEC_VAG	—	—	—	—	I		82	N7
Amplifiers								
AMP_HPDUMMY	—	—	—	—	O		—	R9
AMP_HPOUT	—	—	—	—	O		—	R8
AMP_SPKRN	—	—	—	—	O		—	T9
AMP_SPKRP	—	—	—	—	O		—	T7
Smart Card interface 1								
SIM1_DATA	PSIM14	SSI_TXD	U1TXD	UD	I/O	EVDD	141	E14
SIM1_VEN	PSIM13	SSI_RXD	U1RXD	UD	O	EVDD	142	D16
SIM1_RST	PSIM12	SSI_FS	$\overline{\text{U1RTS}}$	—	O	EVDD	144	E13
SIM1_PD	PSIM11	SSI_BCLK	$\overline{\text{U1CTS}}$	—	O	EVDD	145	E15
SIM1_CLK	PSIM10	SSI_MCLK	—	—	O	EVDD	143	F13
Smart Card interface 0								
SIM0_DATA	PSIM04	—	—	—	I/O	EVDD	—	L3
SIM0_VEN	PSIM03	—	—	—	O	EVDD	—	M2
SIM0_RST	PSIM02	—	—	—	O	EVDD	—	F16
SIM0_PD	PSIM01	—	—	—	O	EVDD	—	L14
SIM0_CLK	PSIM00	—	—	—	O	EVDD	—	M16
USB On-the-Go								
USBO_DM	—	—	—	—	O	USB VDD	148	C16
USBO_DP	—	—	—	—	O	USB VDD	149	B16

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
DSPI_PCS1	PDSPI4	—	—	—	I/O	EVDD	140	F14
DSPI_PCS0/$\overline{SS}$	PDSPI3	$\overline{U2RTS}$	—	U	I/O	EVDD	137	G13
DSPI_SCK	PDSPI2	$\overline{U2CTS}$	—	—	I/O	EVDD	134	H13
DSPI_SIN	PDSPI1	U2RXD	—	—	I	EVDD	136	E16
DSPI_SOUT	PDSPI0	U2TXD	—	—	O	EVDD	135	F15
UARTs								
U2RXD	PUART5	—	—	—	I	EVDD	14	E2
U2TXD	PUART4	—	—	—	O	EVDD	18	F2
$\overline{U0CTS}$	PUART3	USBO_VBUS_EN	USB_PULLUP	—	I	EVDD	20	G4
$\overline{U0RTS}$	PUART2	USBO_VBUS_OC	—	—	O	EVDD	21	G3
U0RXD	PUART1	—	—	—	I	EVDD	27	G2
U0TXD	PUART0	—	—	—	O	EVDD	28	G1
DMA Timers								
T3IN	PTIMER3	T3OUT	IRQ03	—	I	EVDD	13	F3
T2IN	PTIMER2	T2OUT	IRQ02	—	I	EVDD	12	E3
T1IN	PTIMER1	T1OUT	$\overline{DACK1}$	—	I	EVDD	122	K13
T0IN	PTIMER0	T0OUT	CODEC_ALTCLK	—	I	EVDD	121	L16
BDM/JTAG[6]								
ALLPST	PDEBUG	—	—	—	O	EVDD	43	—
JTAG_EN	—	—	—	D	I	EVDD	64	M8
PSTCLK	—	TCLK	—	—	I	EVDD	65	T5
DSI	—	TDI	—	U	I	EVDD	66	T4
DSO	—	TDO	—	—	O	EVDD	120	M15
$\overline{BKPT}$	—	TMS	—	U	I	EVDD	119	M14
DSCLK	—	$\overline{TRST}$	—	U	I	EVDD	118	L15

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Test								
TEST	—	—	—	D	I	EVDD	146	F12
Power Supplies								
IVDD	—	—	—	—	—	—	16, 44, 69, 77, 128, 169, 193	E9, F8, F9, H5, H6, H11, H12, J6, J11, L8, L9
EVDD	—	—	—	—	—	—	9, 24, 26, 40, 47, 51, 54, 57, 74, 126, 139, 195	F5, G6, G11, G12, J12, K6, K11, K12, L5-7, L10-12, M5-7, M12
SD_VDD	—	—	—	—	—	—	7, 102, 116, 156, 163, 181, 208	E5, E6, E10-12, F6, F7, F10, F11
VDD_OSC_A_PLL	—	—	—	—	—	—	46	M4
VDD_USBO	—	—	—	—	—	—	147	E7
VDD_USBH	—	—	—	—	—	—	—	E8
VDD_RTC	—	—	—	—	—	—	—	
AVDD_CODEC	—	—	—	—	—	—	80	N8
AVDD_SPKR	—	—	—	—	—	—	—	T8
VDD_EPM	—	—	—	—	—	—	96	M9
VSTBY_SRAM	—	—	—	—	—	—	—	L2
VSTBY_RTC	—	—	—	—	—	—	—	L4
VSS	—	—	—	—	—	—	8, 15, 25, 39, 45, 48, 52, 53, 56, 68, 73, 76, 101, 117, 138, 168, 180, 192, 194	A1, A16, G7-10, H7-10, J7-10, K7-10, T1, T16
VSS_CODEC	—	—	—	—	—	—	83	N10
AVSS_SPKR_HDST	—	—	—	—	—	—	—	T6
AVSS_SPKR_HP	—	—	—	—	—	—	—	T10

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 The edge port 1 signals are the primary functions on two sets of pins (IRQ1FEC*n* and IRQ1DEBUG*n*). If an IRQ1 function is configured on both pins, the IRQ1FEC*n* pin takes priority. The corresponding IRQ1DEBUG*n* pin is disconnected internally from the edge port 1 module.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

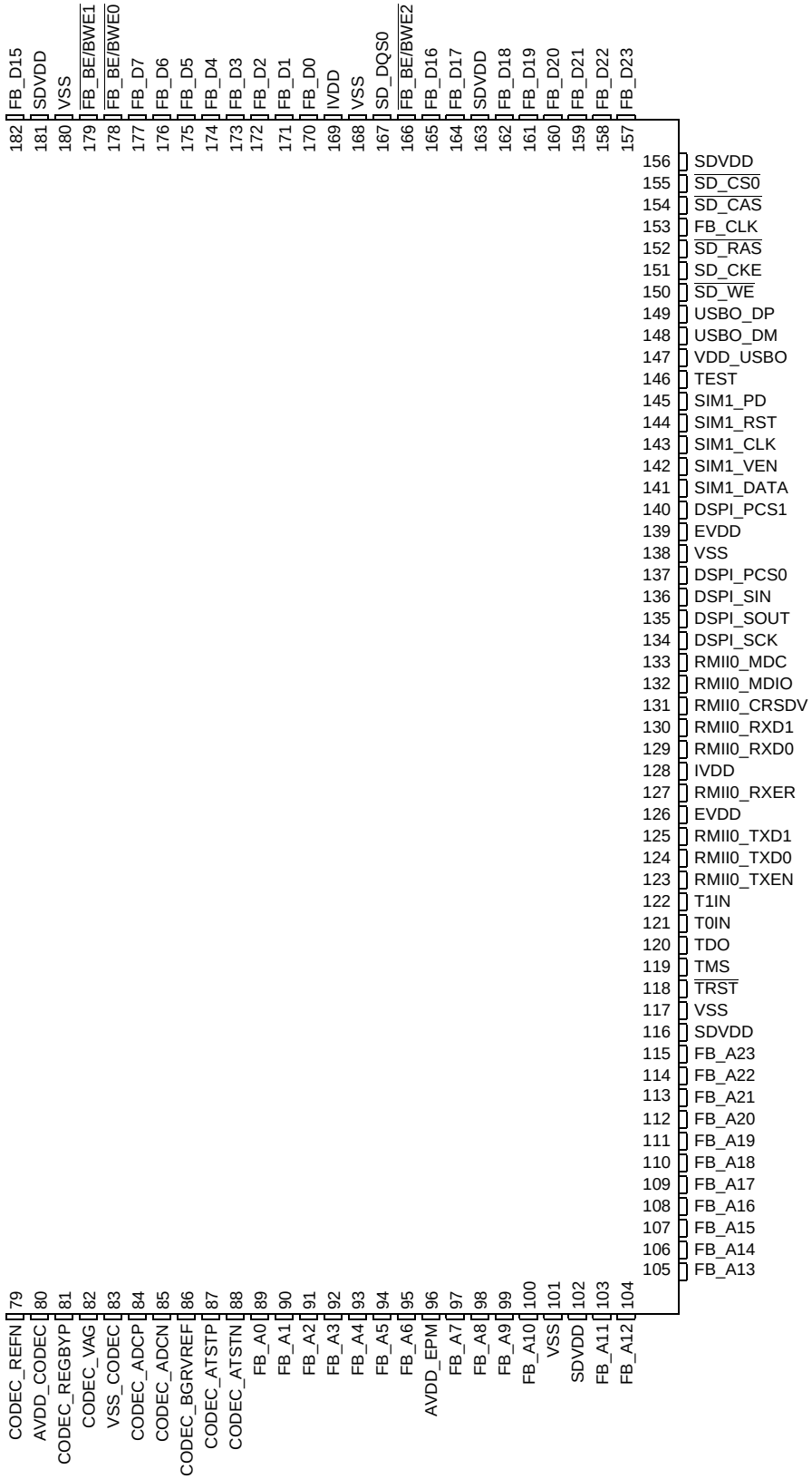

Figure 6. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Right (208 QFP)

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	208 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	36[1,2]	38[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	32[1,2]	33[1,2]	°C/W
Junction to board		θ_{JB}	25[3]	29[3]	°C/W
Junction to case		θ_{JC}	14[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	^{0}C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JEDEC JESD22-A114 specification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.08	1.32	V
SRAM Standby Voltage	$SRAMV_{STBY}$	1.08	1.32	V
RTC Standby Voltage	$RTCV_{STBY}$	3.0	3.6	V
PLL Supply Voltage	$PLLV_{DD}$	3.0	3.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	$0.51 \times EV_{DD}$	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	EV_{IL}	$V_{SS} - 0.3$	$0.42 \times EV_{DD}$	V
CMOS Output High Voltage I_{OH} = –2.0 mA	EV_{OH}	$0.8 \times EV_{DD}$	—	V
CMOS Output Low Voltage I_{OL} = 2.0 mA	EV_{OL}	—	$0.2 \times EV_{DD}$	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 $SDV_{DD} \times 0.7$ Vref+0.15 2	 SDV_{DD}+0.3 SDV_{DD}+0.3 $SDV_{DD} + 0.3$	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 –0.3 –0.3 $V_{SS} - 0.3$	 $SDV_{DD} \times 0.3$ Vref+0.15 0.8	V

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100kHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 12 are shown in Figure 11 and Figure 12.

* The timings are also valid for inputs sampled on the negative clock edge.

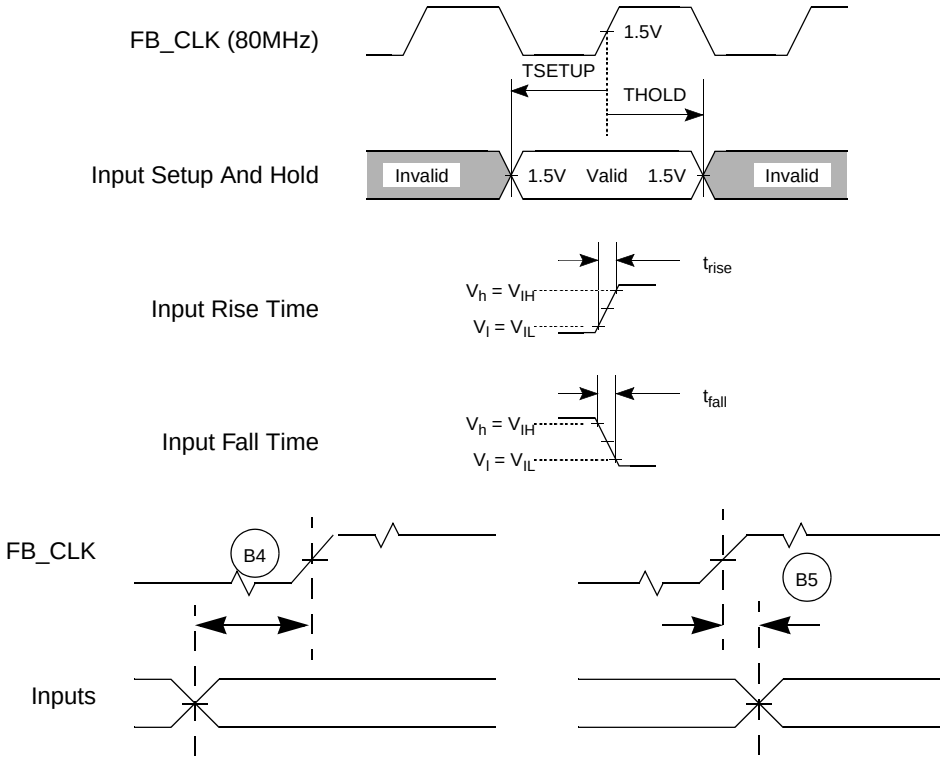

Figure 10. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces.

Chip-select, $\overline{\text{FB\_CS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is 1‘compatible with common ROM/flash memories.

5.6.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 12. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	80	Mhz	$f_{sys/3}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	12.5	—	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0] and $\overline{\text{OE}}$)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{\text{FB\_CS}}$[5:0], R/$\overline{\text{W}}$, $\overline{\text{TS}}$, $\overline{\text{BE/BWE}}$[3:0], and $\overline{\text{OE}}$)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge ($\overline{\text{TA}}$) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge ($\overline{\text{TA}}$) Input Hold	t_{CIFBCH}	0	—	ns	

1 Timing for chip selects only applies to the $\overline{\text{FB\_CS}}$[5:0] signals. Please see Section 5.7.2, “DDR SDRAM AC Timing Characteristics” for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *MCF5301x Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 13. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of operation		50	80	Mhz	1
SD1	Clock period	t_{SDCK}	12.5	20	ns	2
SD2	Pulse width high	t_{SDCKH}	0.45	0.55	SD_CLK	3
SD3	Pulse width low	t_{SDCKH}	0.45	0.55	SD_CLK	4
SD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output hold	$t_{SDCHACI}$	2.0	—	ns	
SD6	SD_SDR_DQS output valid	t_{DQSOV}	—	Self timed	ns	5
SD7	SD_DQS[3:0] input setup relative to SD_CLK	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns	6
SD8	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.			7
SD9	Data (D[31:0]) input setup relative to SD_CLK (reference only)	t_{DVSDCH}	0.25 × SD_CLK	—	ns	8
SD10	Data input hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns	
SD11	Data (D[31:0]) and data mask (SD_DQM[3:0]) output valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns	
SD12	Data (D[31:0]) and data mask (SD_DQM[3:0]) output hold	$t_{SDCHDMI}$	1.5	—	ns	

1 The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the *MCF5301x Reference Manual* for more information on setting the SDRAM clock rate.
2 SD_CLK is one SDRAM clock in (ns).
3 Pulse width high plus pulse width low cannot exceed min and max clock period.
4 Pulse width high plus pulse width low cannot exceed min and max clock period.
5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.
8 Since a read cycle in SDR mode still uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is just provided as guidance.

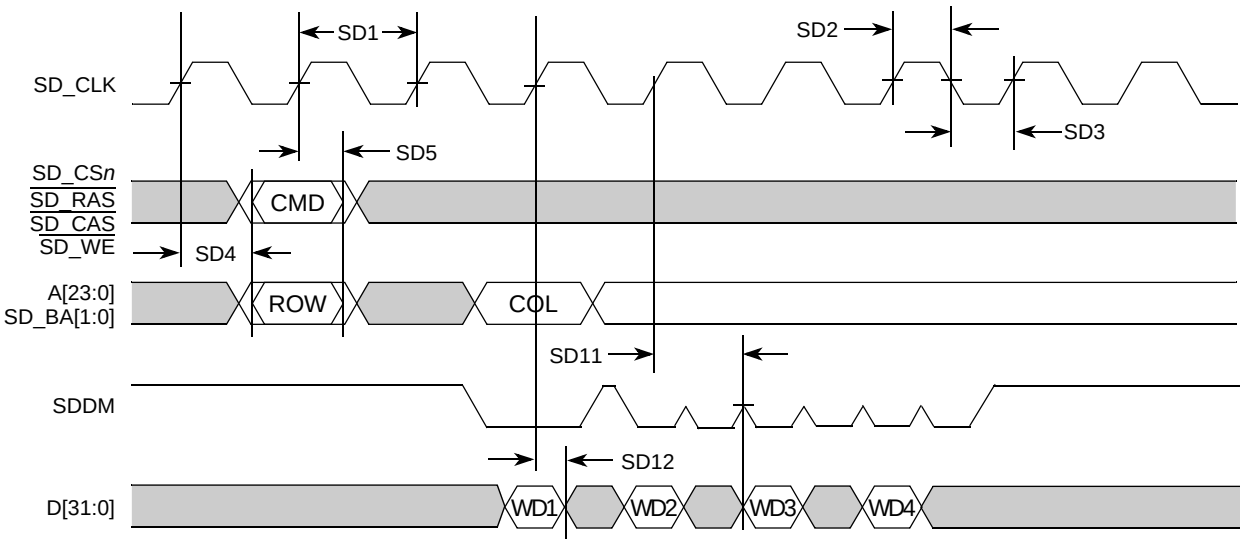

Figure 13. SDR Write Timing

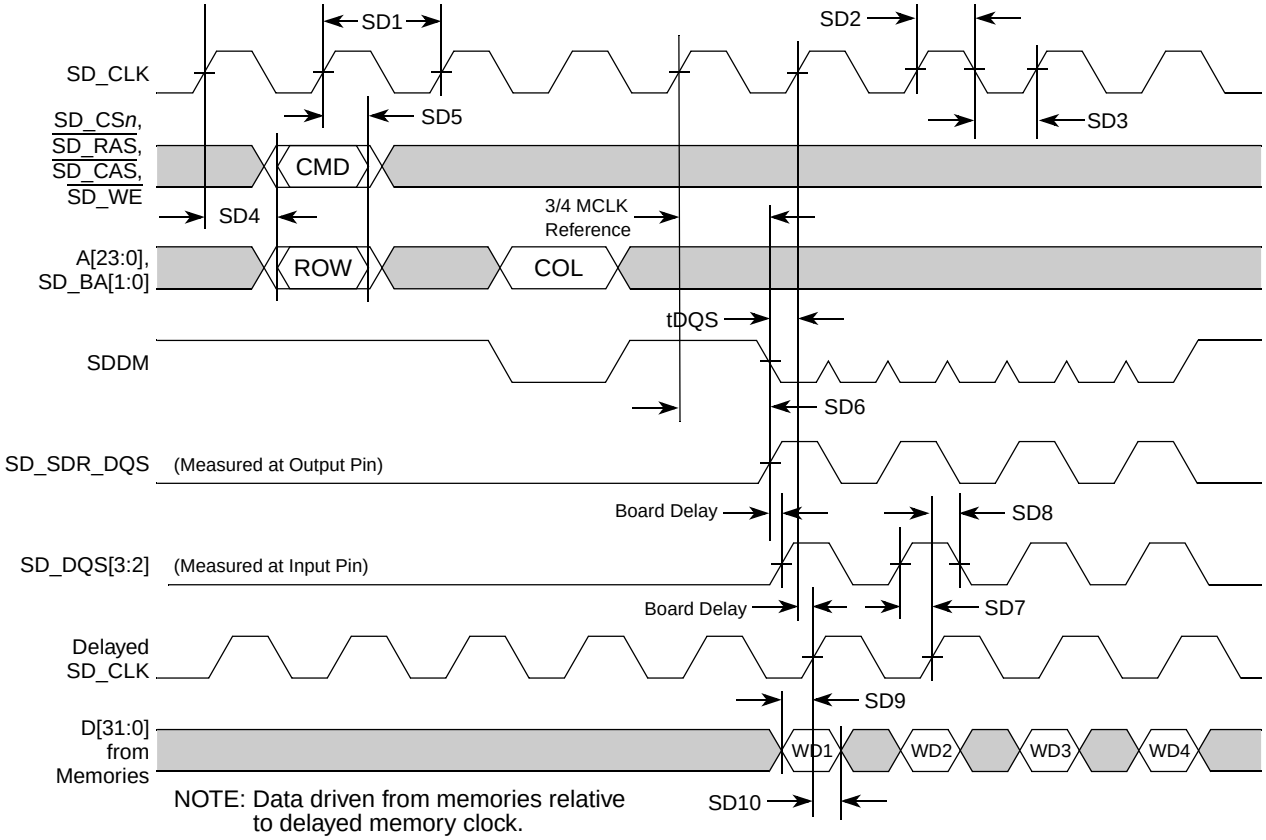

Figure 14. SDR Read Timing

Table 26. DSPI Module AC Timing Specifications[1] (continued)

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS10	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS11	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS12	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS13	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	20	ns	
DS14	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	18	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[DBR], DCTAR*n*[PBR], and DCTAR*n*[BR].

3 This specification assumes a 50/50 duty cycle setting. The duty cycle is programmable in DCTAR*n*[DBR], DCTAR*n*[CPHA], and DCTAR*n*[PBR].

4 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

5 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

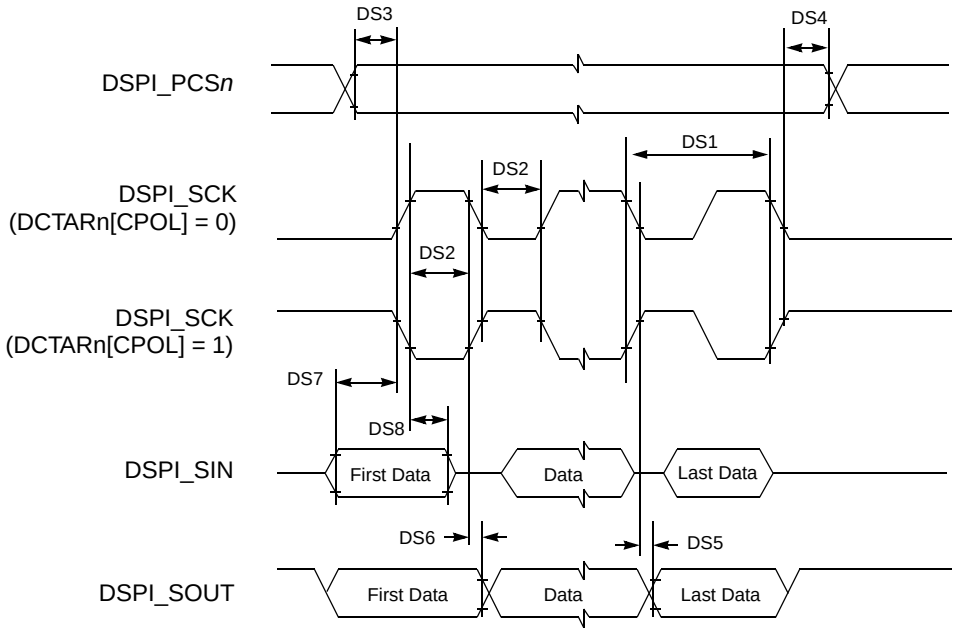

Figure 27. DSPI Classic SPI Timing — Master Mode

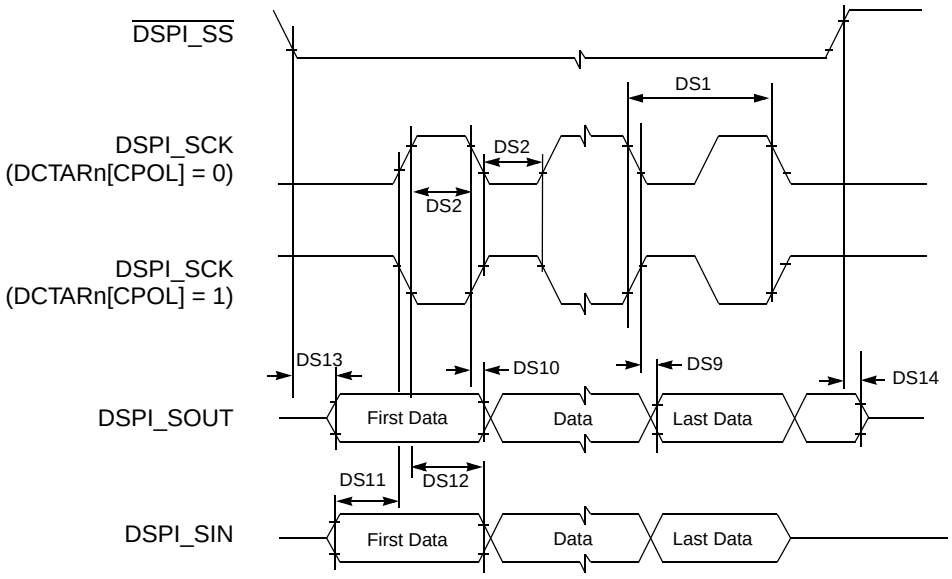

Figure 28. DSPI Classic SPI Timing — Slave Mode

5.16 eSDHC Electrical Specifications

This section describes the electrical information of the eSDHC.

5.16.1 eSDHC Timing

Figure 29 depicts the timing of eSDHC, and Table 29 lists the eSDHC timing characteristics.

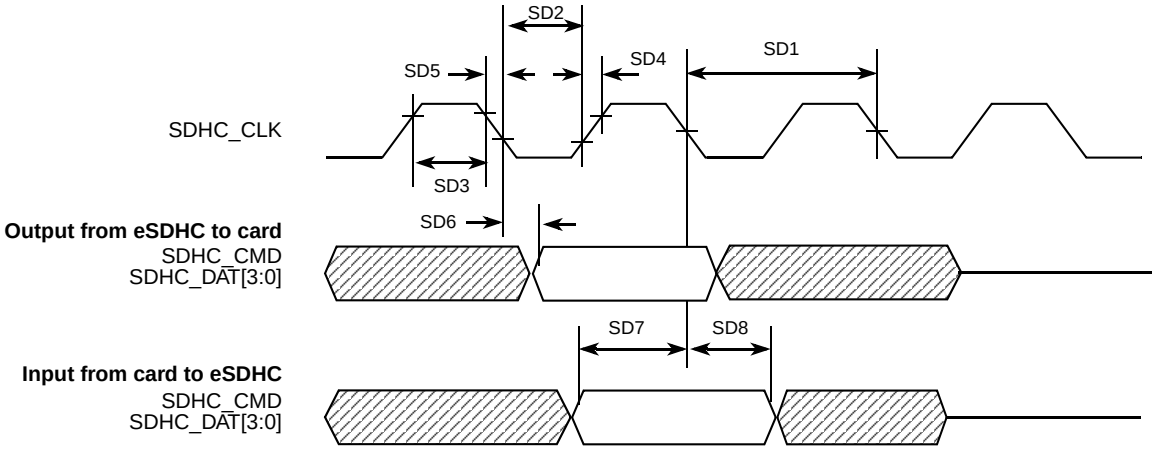

Figure 29. eSDHC Timing

Table 27. eSDHC Interfacde Timing Specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input / Card Outputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	4	—	ns
SD8	eSDHC Input Hold Time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.

4 In card identification mode, card clock must be 100 kHz – 400 kHz, voltage ranges from 2.7 to 3.6 V.

5.16.2 eSDHC Electrical DC Characterisics

Table 28 lists the eSDHC electrical DC characteristics.

Table 28. MMC/SD Interface Electrical Specifications

Num	Parameter	Design Value	Min	Max	Unit	Condition/Remark
General						
1	Peak Voltage on All Lines	—	–0.3	V_{DD} + 0.3	V	
All Inputs						
2	Input Leakage Current	—	–10	10	uA	
All Outputs						
3	Output Leakage Current	—	–10	10	uA	
Power Supply						
4	Supply Voltage (HV card)	3.1	2.7	3.6	V	for high voltage cards, must provide this voltage for card initialization
5	Supply Voltage (LV card)	1.8	1.65	1.95	V	for low voltage cards

Table 29. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK Rise Time [2]	S_{rise}	–	20	ns
3	SIM_CLK Fall Time [3]	S_{fall}	–	20	ns
4	SIM Input Transition Time (RX, SIM_PD)	S_{trans}	–	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

5.17.2 Reset Sequence

5.17.2.1 Cards with Internal Reset

The reset sequence for this kind of SIM card is as follows (see Figure 31):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

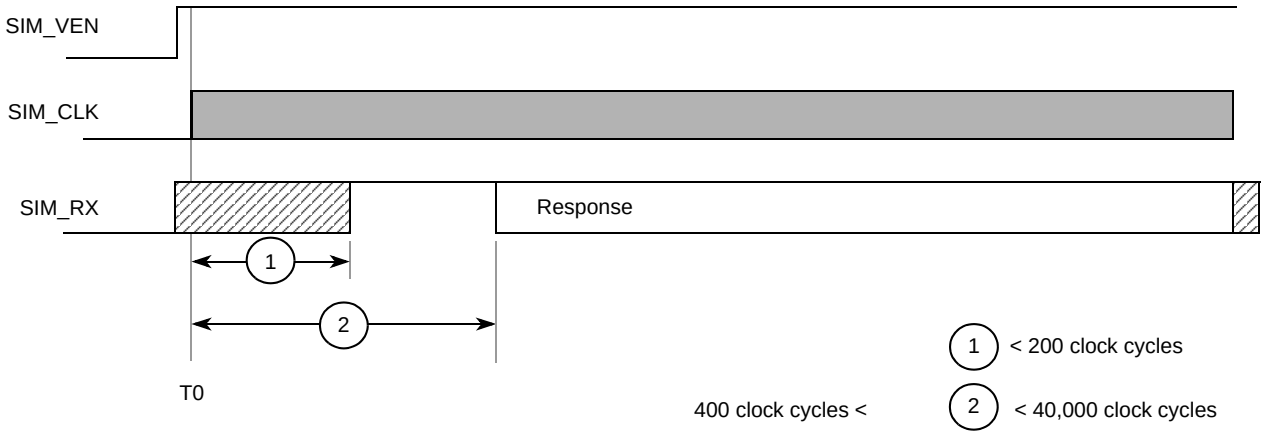

Figure 31. Internal-Reset Card Reset Sequence

5.17.2.2 Cards with Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 32):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Gain vs. Signal	Relative to –10dBm0 @1.02kHz +3 to –40dBm0 –40 to –50dBm0 –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB
Total Distortion (noise and harmonic) (300Hz – 20kHz Noise BW in 300Hz – 4kHz measured BW out)	1.02kHz tone (linear) +2dBm0[4] 0dBm0 –6dBm0 –10dBm0 –20dBm0 –30dBm0 –40dBm0 –45dBm0 –55dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[5]	Psophometric Weighting at the output	—	—	–72	dBm0p
Digital Offset[6]		—	—	5	%Full Scale
Frequency Response VCIHPF = logic high	Relative to 0dBm0@1.02kHz 50Hz 60Hz[7] 200Hz 300 to 3000Hz 3400Hz[8] 4000Hz 4600Hz	 –8 –0.5 –1.0 — — — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCIHPF=logic low	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300 to 3000Hz 3400Hz[9] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –1.0 — —	 — — — — — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Crosstalk D/A to A/D	D/A = 0 dBm0 @1.02kHz Measured while stimulated w/ 2667Hz @–50dBm0	—	—	–75	dB
Intermodulation Distortion	Two frequencies of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCIHPF=logic high CODEC_CLK=26MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	260 155 57 15 95 135 190	µS µS µS µS µS µS µS
Filter Group Delay VCIHPF=logic low CODEC_CLK=26MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 150 200	µS µS µS µS
Filter Absolute Group Delay VCIHPF=logic high	f=1.6kHz	—	—	300	µS
Filter Absolute Group Delay VCIHPF=logic low	f=1.6kHz	—	—	235	µS
Out of Band input fold-in spurious	with 0dBm0 input signal from 4.6 kHz to 8.4 kHz	—	—	–50	dB

1 All analog signals are referenced to VAG unless otherwise noted.

2 Power Supply Rejection Ratio is for Longjing IC only. Total PSRR from battery to output is obtained by summing the PSRR from Neptune to the one from the Regulator in Seaweed. It is assumed that the regulators in Seaweed will have a minimum PSRR of 45 dB.

3 For A/D differential input (ADC_P - ADC_M) 0dBm0 = 340mV$_{rms}$.
The codec output will not “foldback” or oscillate if overdriven, but clip.

4 The digital word corresponding to +3dBm0 is ‘0111111111111’b. Therefore if the audio level is set to +3dBm0, any variation in gain could cause large distortion if the digital number exceeds ‘0111111111111’b. For this reason the maximum recommended signal for low distortion is +3dBm0 – (Absolute Gain Error) = +2dBm0.

5 GSM Spec = –64 0dB.

6 This value is a preliminary target. The final number will be specified after obtaining the production statistical data.

7 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

8 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

9 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

Table 38. Microphone Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Total Harmonic Distortion (THD)	Gain = 0dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	%
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 0dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
Integrated Output Noise	BW = 20Hz – 20kHz	Gain = 0dB	—	12	—	µV
		Gain = 20dB	—	40	—	
Signal to Noise Ratio (SNR)	V_{OUT} = 0.5V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	92.4	—	dB
		Gain = 20dB	—	81.9	—	
THD plus Noise	V_{OUT} = 0.35V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	80	—	dB
		Gain = 20dB	—	80	—	
Power Supply Rejection Ratio	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 1kHz	—	60	—	dB
		f = 4kHz	—	60	—	
Commom Mode Rejection Ratio	Gain = 0dB, V_{ripple} = 100mV_{pp}	f = 1kHz	—	50	—	dB
		f = 4kHz	—	50	—	
Gain Error	Gain = 0, 6, 9.56, 15.56, 20, 24, 29.56, 39.9 dB		—	±0.5	—	dB
Input Impedance	Depends on the Gain Setting		1.5	—	24.0	kΩ

5.21 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns