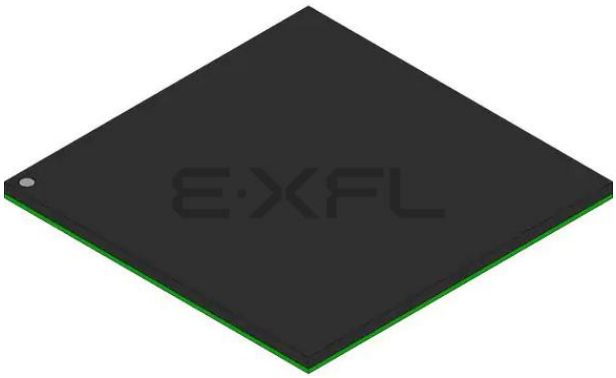

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53014cmj240j

Table 4. Current Measurementas at Different VCO vs. Core Frequencies

Stop Mode	480VCO, 240MHz core	240VCO, 120MHz core	480VCO, 120MHz core	480VCO, 48MHz core	Limp Mode, 20HMHz crystal
Executing	55.3mA	28.36mA	30.00mA	13.6mA	5.90mA
Run	39.5mA	20.3mA	22.02mA	10.29mA	4.42mA
Wait	16.28mA	8.53mA	10.23mA	5.53mA	2.43mA
Doze	16.19mA	8.53mA	10.18mA	5.55mA	2.41mA
Stop(0)	8.41mA	4.60mA	6.29mA	3.90mA	1.78mA
Stop(1)	8.13mA	4.48mA	6.15mA	3.88mA	1.77mA
Stop(2)	1.83mA	1.86mA	1.87mA	1.82mA	1.76mA
Stop(3)	0.65mA	0.66mA	0.67mA	0.67mA	0.65mA

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5301*x* pins grouped by function. The “Dir” column is the direction for the primary function of the pin only. Refer to Section 4.2, “Pinout—208 LQFP,” and Section 4.3, “Pinout–256 MAPBGA,” for package diagrams. For a more detailed discussion of the MCF3xx*x* signals, consult the *MCF5301x Reference Manual* (MCF53017RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5301*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	41	M3
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	42	N1
Clock								
EXTAL	—	—	—	—	I	EVDD	49	T2
XTAL	—	—	—	U[3]	O	EVDD	50	T3
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	55, 17	J5, G5
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[3:2]	—	—	O	SDVDD	115, 114	P16, N16
FB_A[21:16]	—	—	—	—	O	SDVDD	113–108	R16, N14, N15, P15-13
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	107, 106	R15, R14
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	105–103	N13, R12, R13
FB_A10	—	—	—	—	O	SDVDD	100	N12
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	99–97 95–89	P12, T14, T15, R11, P11, N11, T13, R10, T11, T12
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	208–198, 57–62, 64, 65	B3, A2, D6, C5, B4, A3, B5, C6, D12, C14, B14, C13, D11, B13, A14, A13
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	182–189, 177–170	B9, A9, A8, D7, B8, C8, D8, B7, C10, A10, B10, D10, C11, A11, B11, A12
FB_CLK	—	—	—	—	O	SDVDD	153	D13
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	197, 166, 179, 178	A4, B12, C9, D9
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	—	O	SDVDD	—	B6, C7
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	5	D2
$\overline{\text{FB\_CS0}}$	PCS0	$\overline{\text{FB\_CS4}}$	—	—	O	SDVDD	6	C2
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	1	D4
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	3	B2
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	2	C3
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	4	D3
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	206	C4

4.2 Pinout—208 LQFP

The pinout for the 208 LQFP devices is shown in Figure 5 and Figure 6.

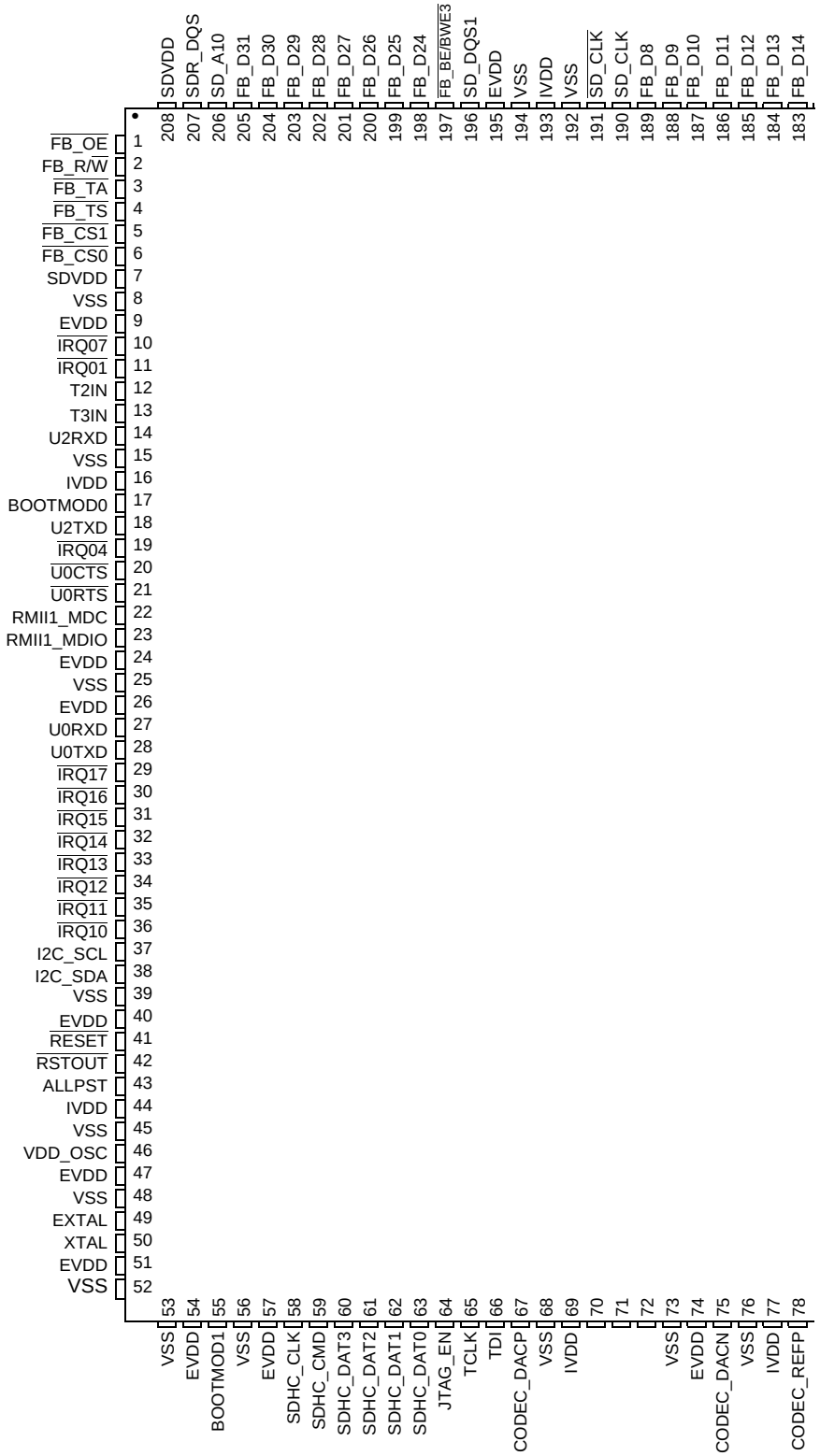

Figure 5. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Left (208 QFP)

4.3 Pinout–256 MAPBGA

The pinout for the MCF53014, MCF53015, MCF53016, and MCF53017 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_D 30	FB_D 26	FB_BE/ BWE3	SD_ DQS1	SD_ CLK	SD_ CLK	FB_D 13	FB_D 14	FB_D 6	FB_D 2	FB_D 0	FB_D 16	FB_D 17	SD_CS	VSS	A
B	USBH_ DM	FB_TA	FB_D 31	FB_D 27	FB_D 25	FB_CS5	FB_D 8	FB_D 11	FB_D 15	FB_D 5	FB_D 1	FB_BE/ BWE2	FB_D 18	FB_D 21	SD_ CKE	USBO_ DP	B
C	USBH_ DP	FB_CS0	FB_R/W	SD_A10	FB_D 28	FB_D 24	FB_CS4	FB_D 10	FB_BE/ BWE1	FB_D 7	FB_D 3	SD_ DQS2	FB_D 20	FB_D 22	SD_ RAS	USBO_ DM	C
D	IRQ04	FB_CS1	FB_TS	FB_OE	SD_SDR _DQS	FB_D 29	FB_D 12	FB_D 9	FB_BE/ BWE0	FB_D 4	FB_D 19	FB_D 23	FB_CLK	SD_ WE	SD_ CAS	SIM1_ VEN	D
E	RMII1_ MDC	U2RXD	T2IN	IRQ07	SDVDD	SDVDD	VDD_ USBO	VDD_ USBH	IVDD	SDVDD	SDVDD	SDVDD	SIM1_ RST	SIM1_ DATA	SIM1_ PD	DSPI_ SIN	E
F	RMII1_ MDIO	U2TXD	T3IN	IRQ01	EVDD	SDVDD	SDVDD	IVDD	IVDD	SDVDD	SDVDD	TEST	SIM1_ CLK	DSPI_ PCS1	DSPI_ SOUT	SIM0_ RST	F
G	U0TXD	U0RXD	U0RTS	U0CTS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	DSPI_ PCS0	RMII0_ MDC	RMII0_ MDIO	RMII0_ CRSDV	G
H	IRQ1 DEBUG7	IRQ1 DEBUG4	IRQ1 DEBUG5	IRQ1 DEBUG6	IVDD	IVDD	VSS	VSS	VSS	VSS	IVDD	IVDD	DSPI_ SCK	IRQ1 DEBUG2	RMII0_ RXD1	RMII0_ RXD0	H
J	IRQ1 FEC7	IRQ1 FEC6	IRQ1 FEC4	IRQ1 FEC3	BOOT MOD1	IVDD	VSS	VSS	VSS	VSS	IVDD	EVDD	IRQ1 DEBUG0	RMII0_ TXD0	RMII0_ TXD1	RMII0_ RXER	J
K	IRQ1 FEC2	IRQ1 FEC1	I2C_ SDA	IRQ1 FEC5	NC	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	T1IN	IRQ1 DEBUG3	IRQ1 DEBUG1	RMII0_ TXEN	K
L	IRQ1 FEC0	VSTBY_ SRAM	SIM0_ DATA	VSTBY_ RTC	EVDD	EVDD	EVDD	IVDD	IVDD	EVDD	EVDD	EVDD	IRQ06	SIM0_ PD	TRST	T0IN	L
M	I2C_ SCL	SIM0_ VEN	RESET	VDD_ OSC_A_ PLL	EVDD	EVDD	EVDD	JTAG_ EN	VDD_ EPM	NC	NC	EVDD	NC	TMS	TDO	SIM0_ CLK	M
N	RST OUT	DSPI_ PCS2	SSI_ RXD	SDHC_ DAT3	SDHC_ DAT0	SDHC_ DAT1	CODEC _VAG	AVDD_ CODEC	CODEC _BGR VREF	VSS_ CODEC	FB_A4	FB_A10	FB_A13	FB_A20	FB_A19	FB_A22	N
P	RTC_ EXTAL	DSPI_ PCS3	SSI_ TXD	SSI_ MCLK	SSI_ BCLK	CODEC _REG BYP	CODEC _REFP	CODEC _REFN	CODEC _ADCP	CODEC _ADCN	FB_A5	FB_A9	FB_A16	FB_A17	FB_A18	FB_A23	P
R	RTC_ XTAL	SSI_FS	SDHC_ CLK	SDHC_ CMD	SDHC_ DAT2	CODEC _DACP	CODEC _DACN	AMP_ HP OUT	AMP_ HP DUMMY	FB_A2	FB_A6	FB_A12	FB_A11	FB_A14	FB_A15	FB_A21	R
T	VSS	EXTAL	XTAL	TDI	TCLK	AVSS_ SPKR_ HDST	AMP_ SPKRP	AVDD_ SPKR	AMP_ SPKRN	AVSS_ SPKR_ HP	FB_A1	FB_A0	FB_A3	FB_A8	FB_A7	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7. MCF53014, MCF53015, MCF53016, and MCF53017 Pinout (256 MAPBGA)

5 Preliminary Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5301*x* microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	–0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	–0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	–0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	–0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	–0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L – T_H)	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JEDEC JESD22-A114 specification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.08	1.32	V
SRAM Standby Voltage	$SRAMV_{STBY}$	1.08	1.32	V
RTC Standby Voltage	$RTCV_{STBY}$	3.0	3.6	V
PLL Supply Voltage	$PLLV_{DD}$	3.0	3.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	$0.51 \times EV_{DD}$	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	EV_{IL}	$V_{SS} - 0.3$	$0.42 \times EV_{DD}$	V
CMOS Output High Voltage I_{OH} = –2.0 mA	EV_{OH}	$0.8 \times EV_{DD}$	—	V
CMOS Output Low Voltage I_{OL} = 2.0 mA	EV_{OL}	—	$0.2 \times EV_{DD}$	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 $SDV_{DD} \times 0.7$ Vref+0.15 2	 SDV_{DD}+0.3 SDV_{DD}+0.3 $SDV_{DD} + 0.3$	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 –0.3 –0.3 $V_{SS} - 0.3$	 $SDV_{DD} \times 0.3$ Vref+0.15 0.8	V

Table 10. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDVDD × 0.9 SDV_{DD} – 0.35 2.9	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 SDV_{DD} × 0.1 0.35 0.4	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Weak Internal Pull-Up/Pull-down Device Current[1]	I_{APU}	10	315	µA
Selectable Weak Internal Pull-Up/Pull-down Device Current[2]	I_{APU}	25	150	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 Refer to the signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 8 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

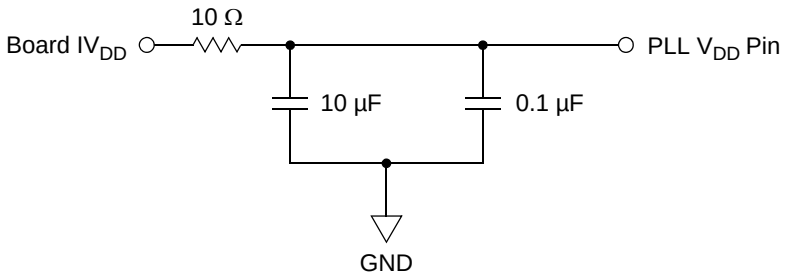

Figure 8. System PLL V_{DD} Power Filter

5.4.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

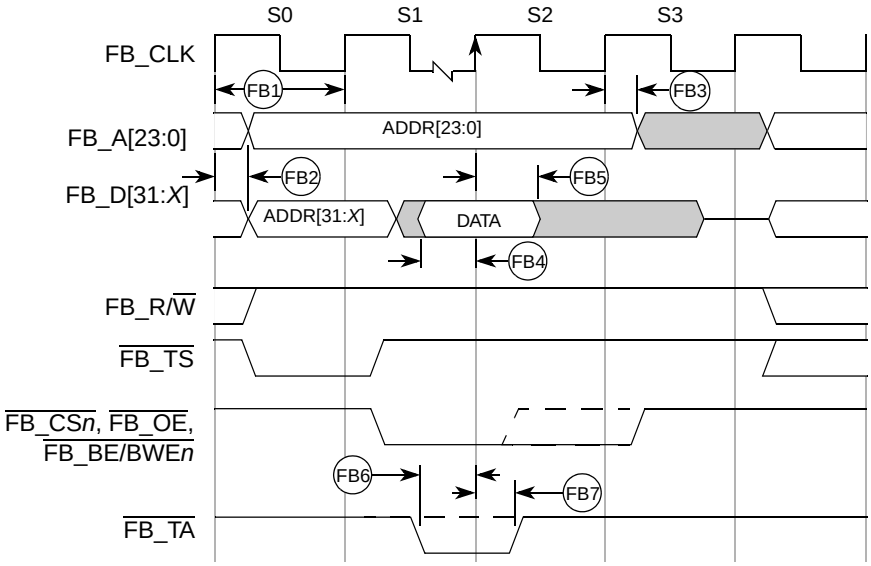

Figure 11. FlexBus Read Timing

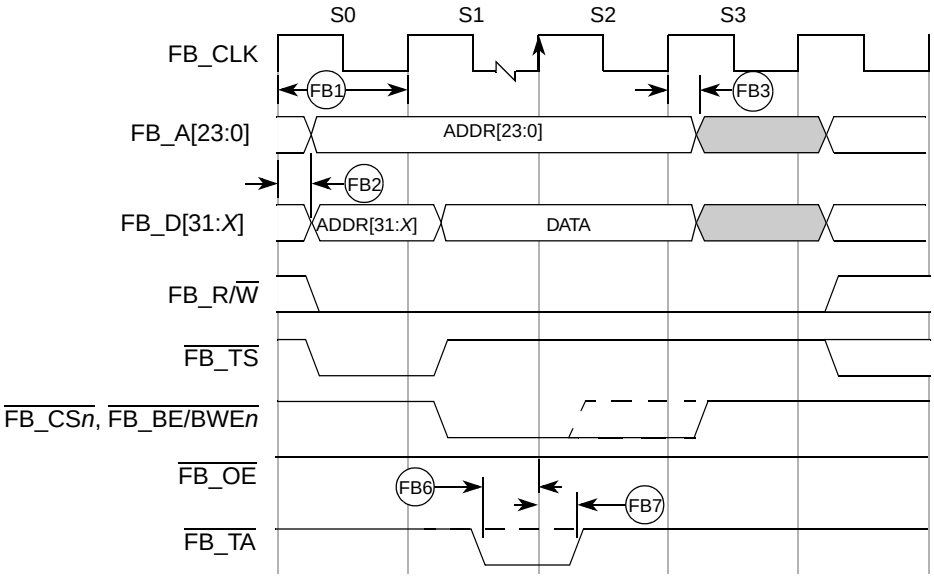

Figure 12. Flexbus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during

read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 13. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of operation		50	80	Mhz	1
SD1	Clock period	t_{SDCK}	12.5	20	ns	2
SD2	Pulse width high	t_{SDCKH}	0.45	0.55	SD_CLK	3
SD3	Pulse width low	t_{SDCKH}	0.45	0.55	SD_CLK	4
SD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] output hold	$t_{SDCHACI}$	2.0	—	ns	
SD6	SD_SDR_DQS output valid	t_{DQSOV}	—	Self timed	ns	5
SD7	SD_DQS[3:0] input setup relative to SD_CLK	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns	6
SD8	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.			7
SD9	Data (D[31:0]) input setup relative to SD_CLK (reference only)	t_{DVSDCH}	0.25 × SD_CLK	—	ns	8
SD10	Data input hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns	
SD11	Data (D[31:0]) and data mask (SD_DQM[3:0]) output valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns	
SD12	Data (D[31:0]) and data mask (SD_DQM[3:0]) output hold	$t_{SDCHDMI}$	1.5	—	ns	

1 The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the *MCF5301x Reference Manual* for more information on setting the SDRAM clock rate.
2 SD_CLK is one SDRAM clock in (ns).
3 Pulse width high plus pulse width low cannot exceed min and max clock period.
4 Pulse width high plus pulse width low cannot exceed min and max clock period.
5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.
8 Since a read cycle in SDR mode still uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is just provided as guidance.

8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

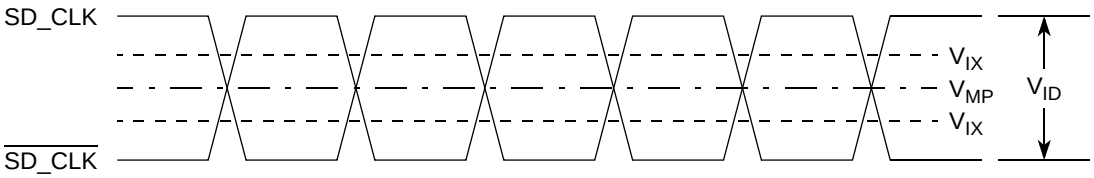

Figure 15. SD_CLK and SD_CLK Crossover Timing

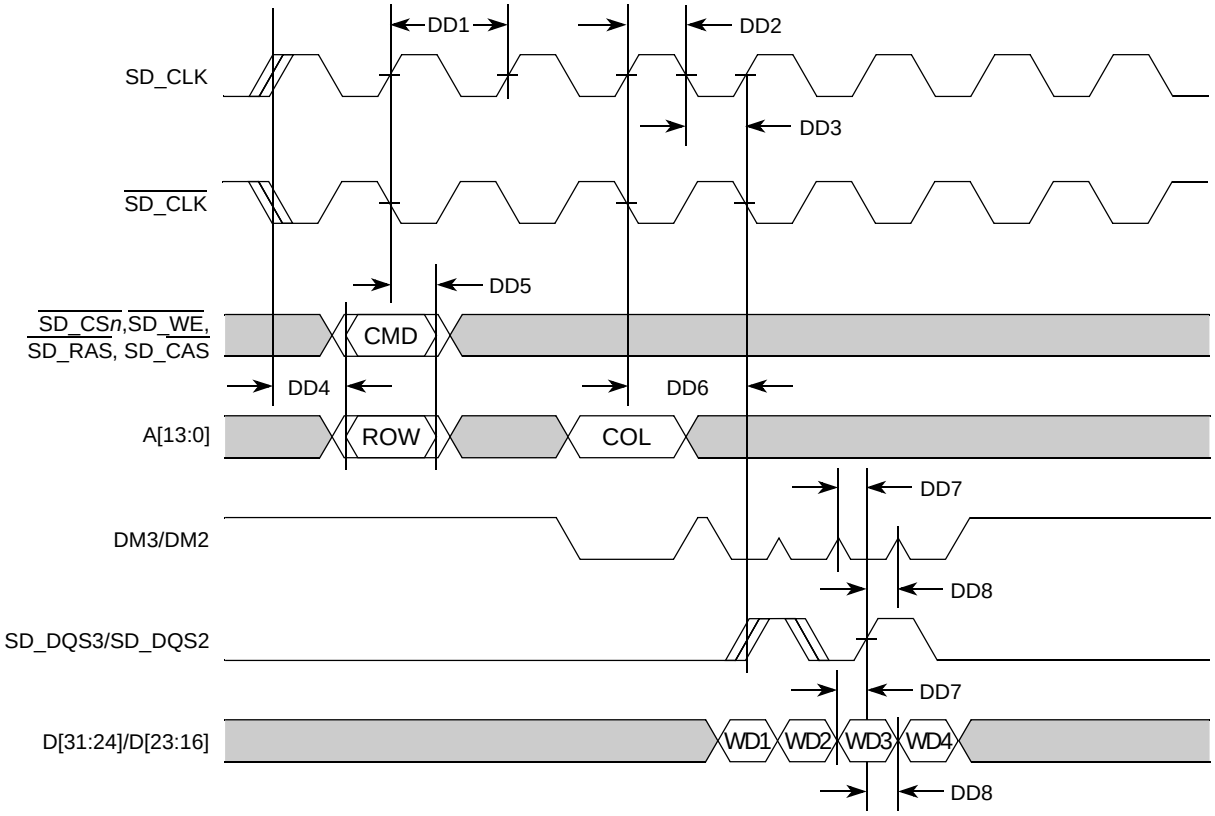

Figure 16. DDR Write Timing

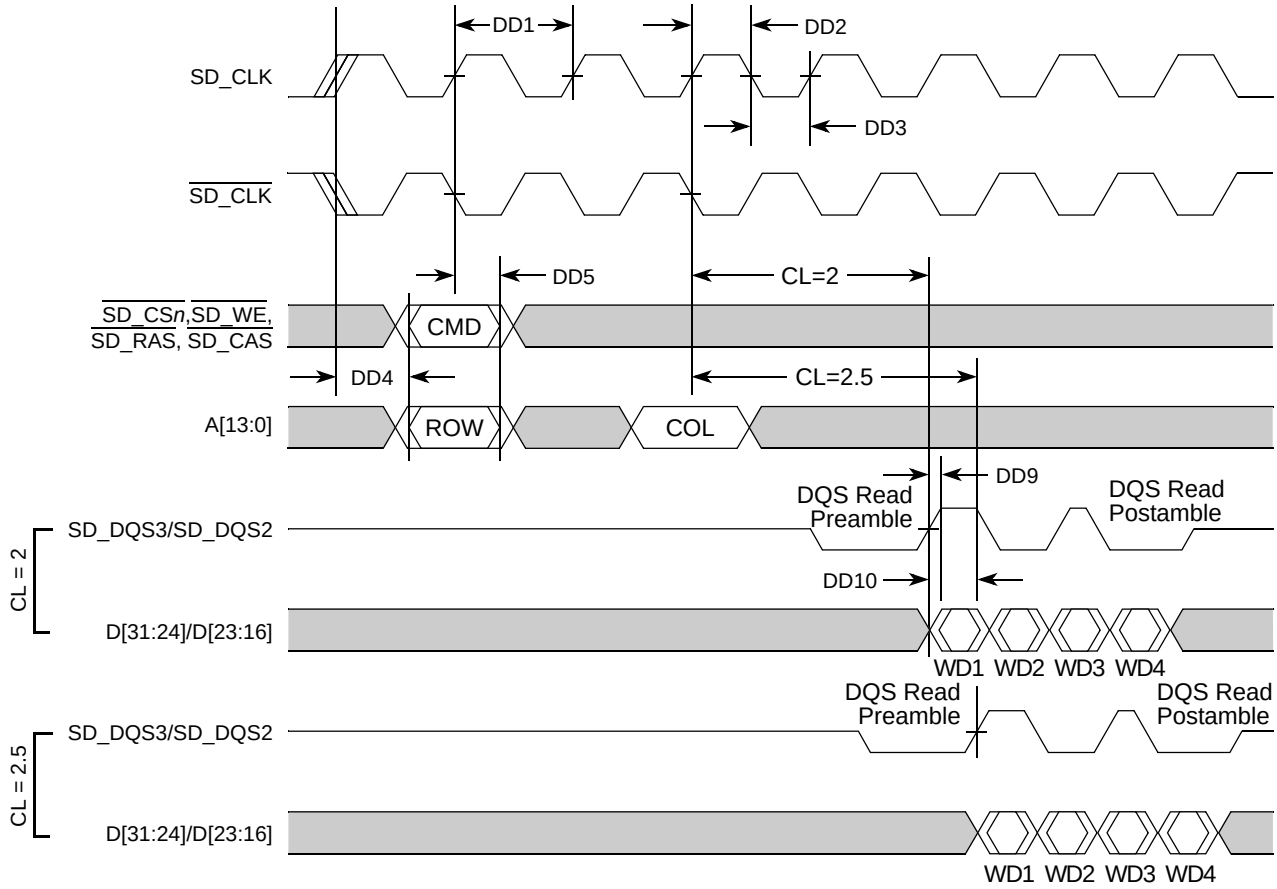

Figure 17. DDR Read Timing

5.8 General Purpose I/O Timing

Table 15. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, and Timer pins.

5.10 USB On-The-Go

The MCF53017 device is compliant with industry standard USB 2.0 specification.

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 17. SSI Timing - Master Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$8 \times t_{SYS}$	—	ns	[2]
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	[3]
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	
S5	SSI_BCLK to SSI_FS output valid		—	15	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	15	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		–2	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 18. SSI Timing — Slave Modes[1]

Num	Description	Symbol	Min	Max	Units	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	15	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25pF.

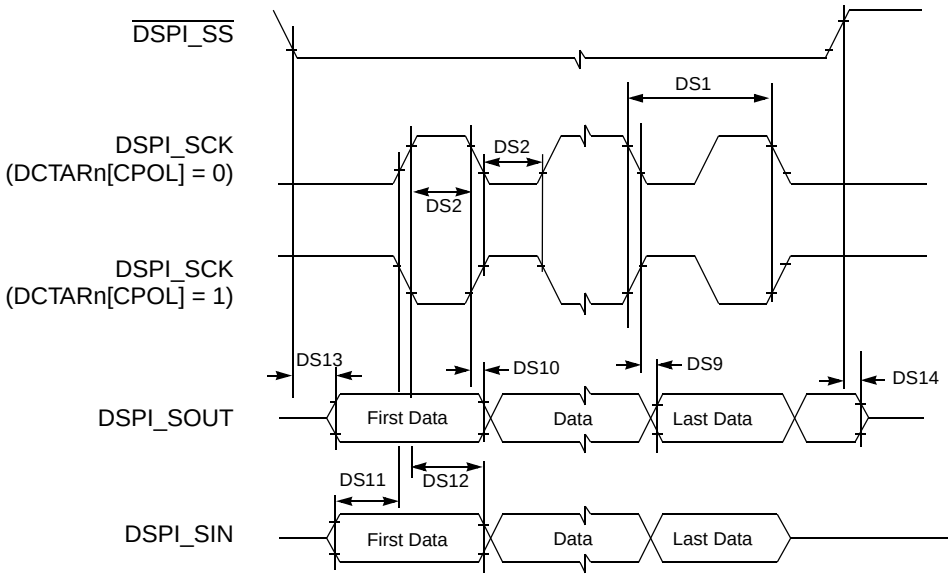

Figure 28. DSPI Classic SPI Timing — Slave Mode

5.16 eSDHC Electrical Specifications

This section describes the electrical information of the eSDHC.

5.16.1 eSDHC Timing

Figure 29 depicts the timing of eSDHC, and Table 29 lists the eSDHC timing characteristics.

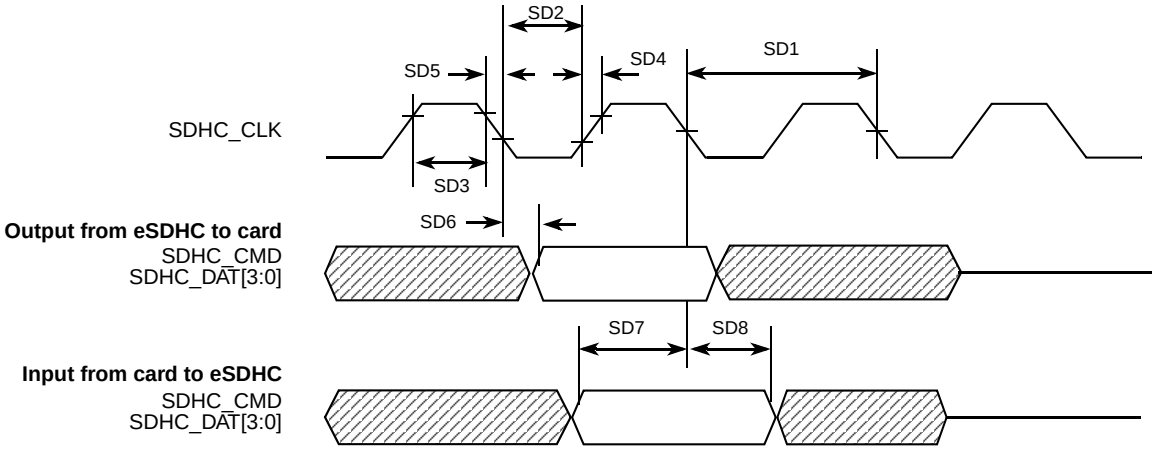

Figure 29. eSDHC Timing

Table 27. eSDHC Interfacde Timing Specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed)	f_{PP}[2]	0	25	MHz
	Clock Frequency (MMC Full Speed)	f_{PP}[3]	0	20	MHz
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–5	5	ns
eSDHC Input / Card Outputs SDHC_CMD, SDHC_DAT (Reference to SDHC_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	4	—	ns
SD8	eSDHC Input Hold Time	t_{IH}	0	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value from 0 to 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value from 0 to 20 MHz.

4 In card identification mode, card clock must be 100 kHz – 400 kHz, voltage ranges from 2.7 to 3.6 V.

5.16.2 eSDHC Electrical DC Characterisics

Table 28 lists the eSDHC electrical DC characteristics.

Table 28. MMC/SD Interface Electrical Specifications

Num	Parameter	Design Value	Min	Max	Unit	Condition/Remark
General						
1	Peak Voltage on All Lines	—	–0.3	V_{DD} + 0.3	V	
All Inputs						
2	Input Leakage Current	—	–10	10	uA	
All Outputs						
3	Output Leakage Current	—	–10	10	uA	
Power Supply						
4	Supply Voltage (HV card)	3.1	2.7	3.6	V	for high voltage cards, must provide this voltage for card initialization
5	Supply Voltage (LV card)	1.8	1.65	1.95	V	for low voltage cards

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Gain vs. Signal	Relative to –10dBm0 @1.02kHz +3 to –40dBm0 –40 to –50dBm0 –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB
Total Distortion (noise and harmonic) (300Hz – 20kHz Noise BW in 300Hz – 4kHz measured BW out)	1.02kHz tone (linear) +2dBm0[4] 0dBm0 –6dBm0 –10dBm0 –20dBm0 –30dBm0 –40dBm0 –45dBm0 –55dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[5]	Psophometric Weighting at the output	—	—	–72	dBm0p
Digital Offset[6]		—	—	5	%Full Scale
Frequency Response VCIHPF = logic high	Relative to 0dBm0@1.02kHz 50Hz 60Hz[7] 200Hz 300 to 3000Hz 3400Hz[8] 4000Hz 4600Hz	 –8 –0.5 –1.0 — — — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCIHPF=logic low	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300 to 3000Hz 3400Hz[9] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –1.0 — —	 — — — — — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Crosstalk D/A to A/D	D/A = 0 dBm0 @1.02kHz Measured while stimulated w/ 2667Hz @–50dBm0	—	—	–75	dB
Intermodulation Distortion	Two frequencies of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Figure 34 and Figure 35 show the filter frequency response for the audio signal for voice coding path. (All filter frequencies increase by 8.1/8.0 if VCLK is selected to generate f_{SYNC}=8.1kHz).

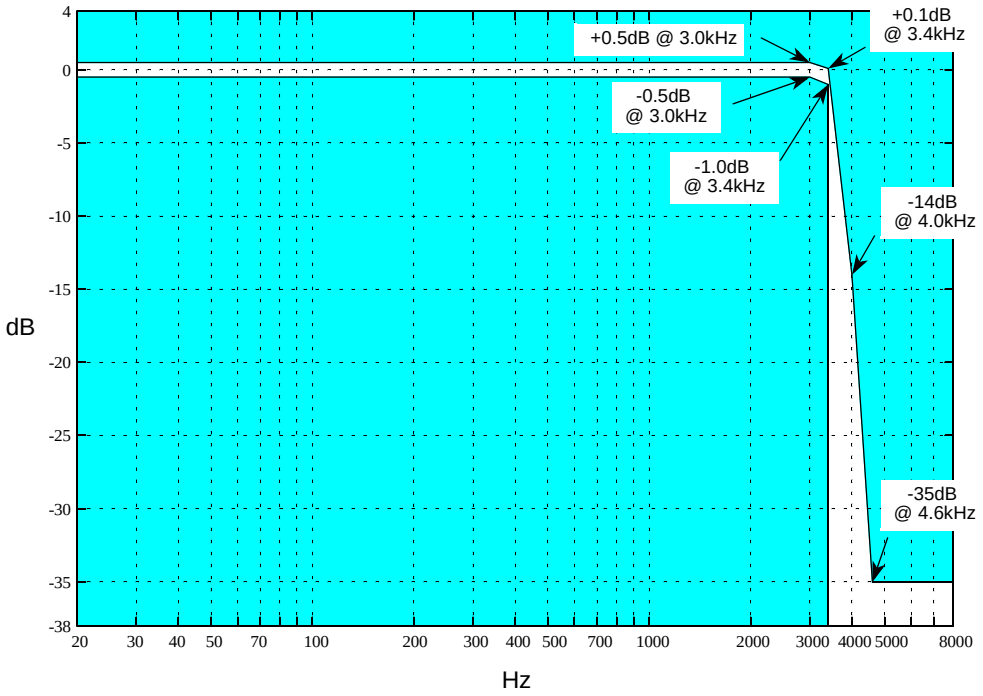

Figure 34. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=0, LPF Alone Without HPF)

Table 35. Speaker Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 1.4V_{RMS}, BW = 20Hz – 20kHz		—	99	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Max. Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	625	—	mA
Gain Error	Gain = –45,–21, –6, 0, 4, 6 dB		—	±0.5	—	dB

5.20.2 Handset Amplifier

The handset amplifier boosts the power from the DAC and drives the handset. It also provides analog volume control to optimize the noise performance of the entire channel. Table 36 shows the specifications for handset amplifier.

Table 36. Handset Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max. Output Power	F_{in} = 1kHz, THD + N = 1%, R_L = 8Ω		—	300	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 8Ω, F_{in} = 1kHz	Full Power, 250mW	—	0.050	—	%
		Half Power, 125mW	—	0.050	—	
	Gain = 0dB, R_L = 8Ω, F_{in} = 4kHz	Full Power, 250mW	—	0.1	—	
		Half Power, 125mW	—	0.050	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 1.4V_{RMS} , BW = 20Hz – 20kHz		—	99	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, Vripple = 200mVpp	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	325	—	mA
Gain Error	Gain = –45, –21, –6, 0, 4, 6 dB		—	±0.5	—	dB

5.20.3 Headphone Amplifier

The headphone amplifier boosts the power from the DAC and drives the headphone. It also provides analog volume control to optimize the noise performance of the entire channel. Table 37 shows the specifications for the microphone amplifier.

Table 37. Headphone Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	600	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 16Ω		—	40	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 16Ω, BW = 200Hz – 4kHz	Full Power, 31.25mW	—	0.05	—	%
		Half Power, 16.5mW	—	0.05	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 0.7V_{RMS} , BW = 20Hz – 20kHz		—	93	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	150	—	mA
Gain Error	Gain = –45, –21, –12, –6, –2, 0 dB		—	±0.5	—	dB

5.20.4 Microphone Amplifier

The microphone amplifier boosts the signal from the microphone and provides it to the ADC. The gain control present in the microphone amplifier helps in optimizing the noise performance of the entire channel. Table 38 shows the specifications for the microphone amplifier.

Table 38. Microphone Amplifier Specifications

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current		—	500	—	µA
Shutdown Current		—	TBD	—	
Input Reference Offset		—	2	5	mV

Table 39. JTAG and Boundary Scan Timing (continued)

Num	Characteristics[1]	Symbol	Min	Max	Unit
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

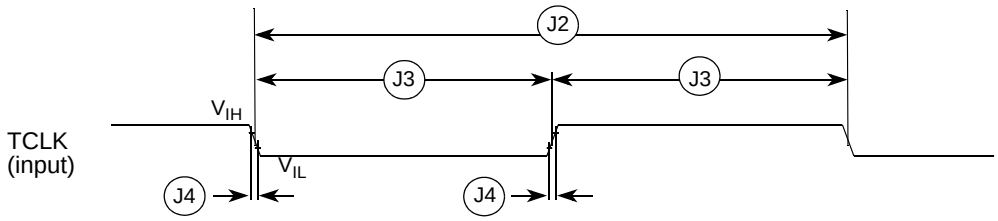

Figure 38. Test Clock Input Timing

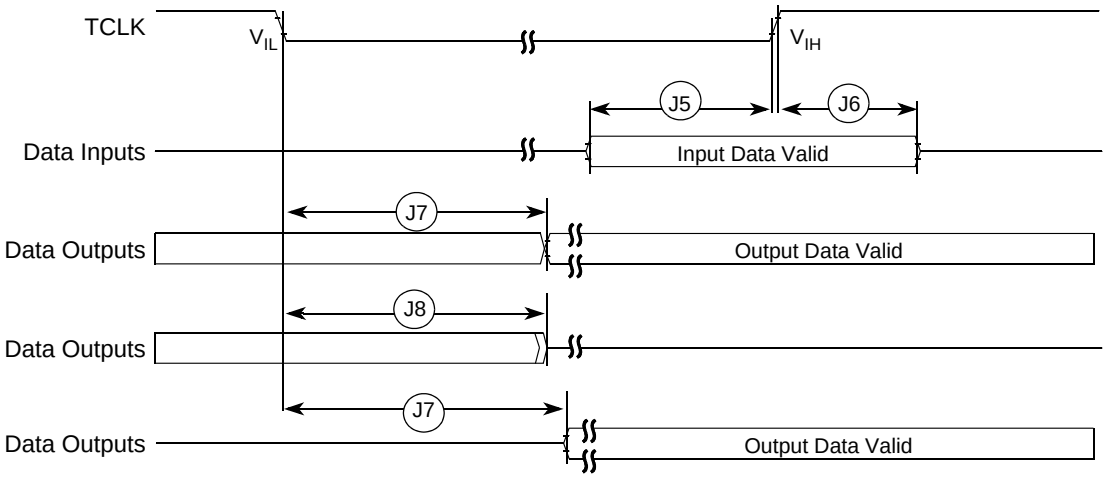

Figure 39. Boundary Scan (JTAG) Timing

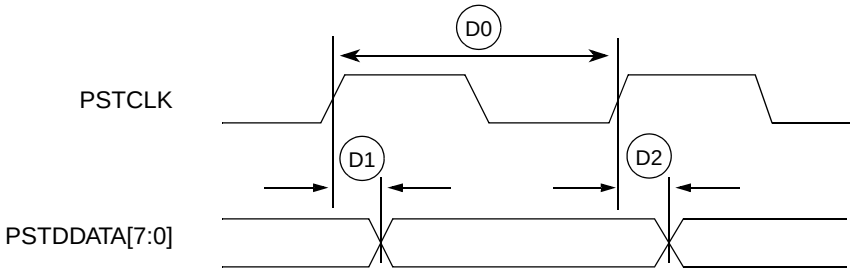

Figure 42. Real-Time Trace AC Timing

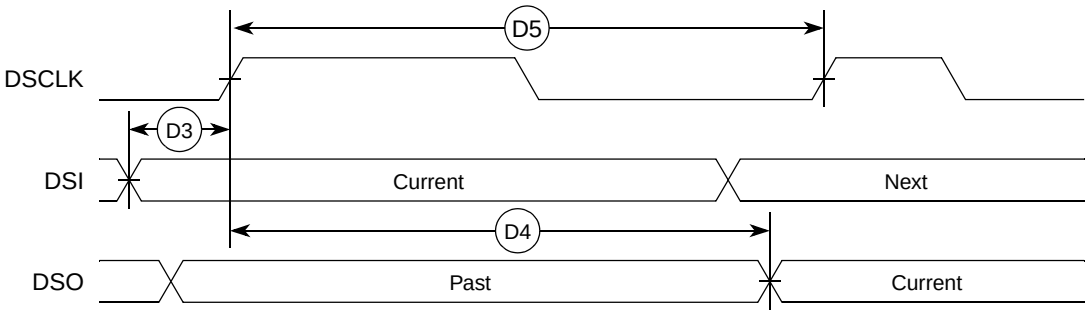

Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.