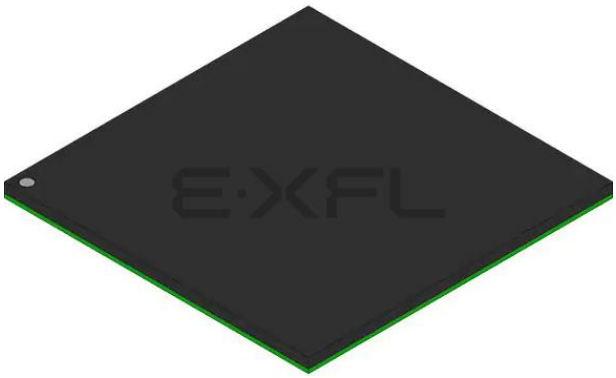

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Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53015cmj240j

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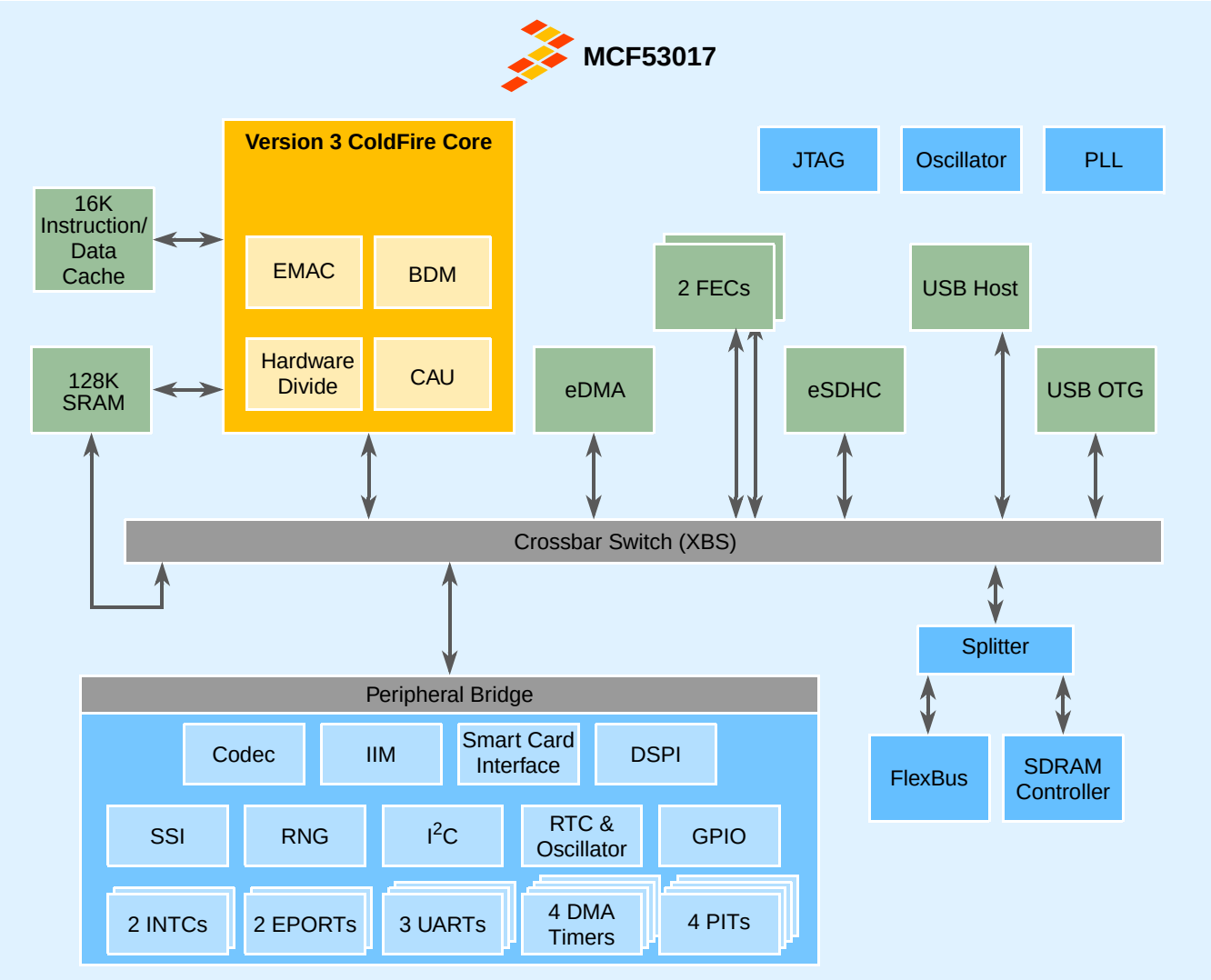
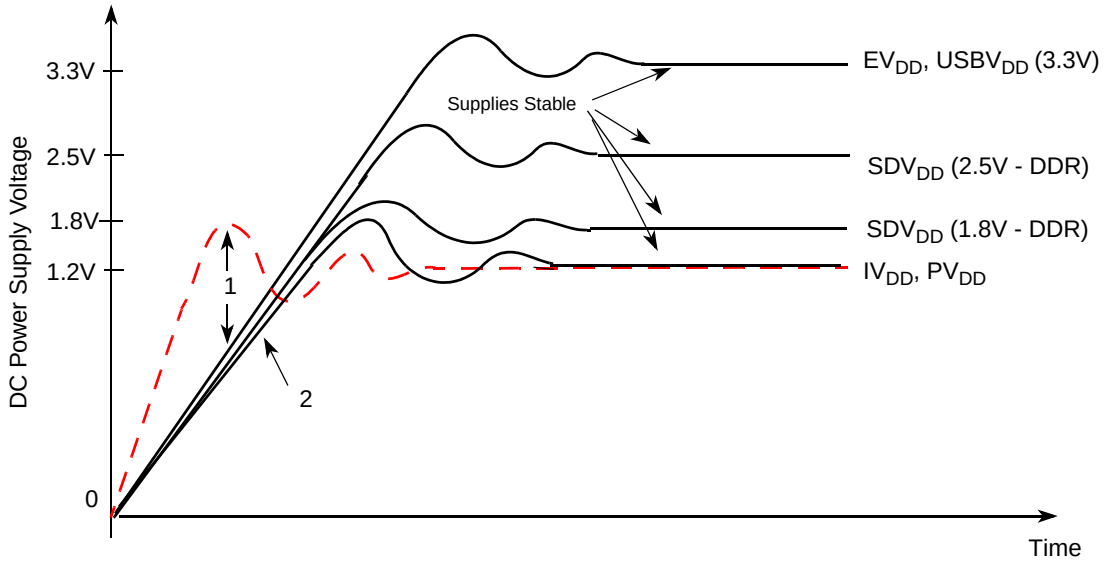


LEGEND

BDM	– Background debug module	**IIM**	– IC identification module
CAU	– Cryptography acceleration unit	**INTC**	– Interrupt controller
DSPI	– DMA serial peripheral interface	**JTAG**	– Joint Test Action Group interface
eDMA	– Enhanced direct memory access module	**PCI**	– Peripheral Component Interconnect
eSDHC	– Enhanced Secure Digital host controller	**PIT**	– Programmable interrupt timers
EMAC	– Enchanced multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random number generator
FEC	– Fast Ethernet Controller	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-Integrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller



Notes:
1. IV_{DD} should not exceed EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V at any time, including power-up.
2. Recommended that IV_{DD}/PV_{DD} should track EV_{DD}/SDV_{DD} up to 0.9V then separate for completion of ramps
3. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PV_{DD} and EV_{DD}/SDV_{DD} should track up to 0.9V and then separate for the completion of ramps with EV_{DD}/SDV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.3.2 Power Down Sequence

If IV_{DD}/PV_{DD} are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or PV_{DD} going low by more than 0.4V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0V.
2. Drop EVDD/SDVDD supplies.

Table 4. Current Measurementas at Different VCO vs. Core Frequencies

Stop Mode	480VCO, 240MHz core	240VCO, 120MHz core	480VCO, 120MHz core	480VCO, 48MHz core	Limp Mode, 20HMHz crystal
Executing	55.3mA	28.36mA	30.00mA	13.6mA	5.90mA
Run	39.5mA	20.3mA	22.02mA	10.29mA	4.42mA
Wait	16.28mA	8.53mA	10.23mA	5.53mA	2.43mA
Doze	16.19mA	8.53mA	10.18mA	5.55mA	2.41mA
Stop(0)	8.41mA	4.60mA	6.29mA	3.90mA	1.78mA
Stop(1)	8.13mA	4.48mA	6.15mA	3.88mA	1.77mA
Stop(2)	1.83mA	1.86mA	1.87mA	1.82mA	1.76mA
Stop(3)	0.65mA	0.66mA	0.67mA	0.67mA	0.65mA

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5301*x* pins grouped by function. The “Dir” column is the direction for the primary function of the pin only. Refer to Section 4.2, “Pinout—208 LQFP,” and Section 4.3, “Pinout–256 MAPBGA,” for package diagrams. For a more detailed discussion of the MCF3xx*x* signals, consult the *MCF5301x Reference Manual* (MCF53017RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
USB Host								
USBH_DM	—	—	—	—	O	USB VDD	—	B1
USBH_DP	—	—	—	—	O	USB VDD	—	C1
FEC 1								
RMII1_MDC	PFECI2C5	—	MII0_TXER	—		EVDD	22	E1
RMII1_MDIO	PFECI2C4	—	MII0_COL	—		EVDD	23	F1
FEC 0								
RMII0_CRS_DV	PFEC06	—	MII0_RXDV	—		EVDD	131	G16
RMII0_RXD[1:0]	PFEC0[5:4]	—	MII0_RXD[1:0]	—		EVDD	130, 129	H15, H16
RMII0_RXER	PFEC03	—	MII0_RXER	—		EVDD	127	J16
RMII0_TXD[1:0]	PFEC0[2:1]	—	MII0_TXD[1:0]	—		EVDD	125, 124	J15, J14
RMII0_TXEN	PFEC00	—	MII0_TXEN	D		EVDD	123	K16
RMII0_MDC	PFECI2C3	—	MII0_MDC	—		EVDD	133	G14
RMII0_MDIO	PFECI2C2	—	MII0_MDIO	—		EVDD	132	G15
Real Time Clock								
RTC_EXTAL	—	—	—	—	I	EVDD	—	P1
RTC_XTAL	—	—	—	—	O	EVDD	—	R1
Synchronous Serial Interface								
SSI_RXD	PSSI4	—	U1RXD	UD	I	EVDD	—	N3
SSI_TXD	PSSI3	—	U1TXD	UD	O	EVDD	—	P3
SSI_FS	PSSI2	—	$\overline{\text{U1RTS}}$	—	I/O	EVDD	—	R2
SSI_MCLK	PSSI1	—	SSI_CLKIN	—	O	EVDD	—	P4
SSI_BCLK	PSSI0	—	$\overline{\text{U1CTS}}$	—	I/O	EVDD	—	P5
I^2C								
I2C_SCL	PFECI2C1	U2RXD	RMII1_MDC	U	I/O	EVDD	37	M1
I2C_SDA	PFECI2C0	U2TXD	RMII1_MDIO	U	I/O	EVDD	38	K3
DSPI								
DSPI_PCS3	PDSPI6	USBH_VBUS_EN	—	—	I/O	EVDD	—	P2
DSPI_PCS2	PDSPI5	USBH_VBUS_OC	—	—	I/O	EVDD	—	N2

4.3 Pinout–256 MAPBGA

The pinout for the MCF53014, MCF53015, MCF53016, and MCF53017 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_D 30	FB_D 26	FB_BE/ BWE3	SD_ DQS1	SD_ CLK	SD_ CLK	FB_D 13	FB_D 14	FB_D 6	FB_D 2	FB_D 0	FB_D 16	FB_D 17	SD_CS	VSS	A
B	USBH_ DM	FB_TA	FB_D 31	FB_D 27	FB_D 25	FB_CS5	FB_D 8	FB_D 11	FB_D 15	FB_D 5	FB_D 1	FB_BE/ BWE2	FB_D 18	FB_D 21	SD_ CKE	USBO_ DP	B
C	USBH_ DP	FB_CS0	FB_R/W	SD_A10	FB_D 28	FB_D 24	FB_CS4	FB_D 10	FB_BE/ BWE1	FB_D 7	FB_D 3	SD_ DQS2	FB_D 20	FB_D 22	SD_ RAS	USBO_ DM	C
D	IRQ04	FB_CS1	FB_TS	FB_OE	SD_SDR _DQS	FB_D 29	FB_D 12	FB_D 9	FB_BE/ BWE0	FB_D 4	FB_D 19	FB_D 23	FB_CLK	SD_ WE	SD_ CAS	SIM1_ VEN	D
E	RMII1_ MDC	U2RXD	T2IN	IRQ07	SDVDD	SDVDD	VDD_ USBO	VDD_ USBH	IVDD	SDVDD	SDVDD	SDVDD	SIM1_ RST	SIM1_ DATA	SIM1_ PD	DSPI_ SIN	E
F	RMII1_ MDIO	U2TXD	T3IN	IRQ01	EVDD	SDVDD	SDVDD	IVDD	IVDD	SDVDD	SDVDD	TEST	SIM1_ CLK	DSPI_ PCS1	DSPI_ SOUT	SIM0_ RST	F
G	U0TXD	U0RXD	U0RTS	U0CTS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	DSPI_ PCS0	RMII0_ MDC	RMII0_ MDIO	RMII0_ CRSDV	G
H	IRQ1 DEBUG7	IRQ1 DEBUG4	IRQ1 DEBUG5	IRQ1 DEBUG6	IVDD	IVDD	VSS	VSS	VSS	VSS	IVDD	IVDD	DSPI_ SCK	IRQ1 DEBUG2	RMII0_ RXD1	RMII0_ RXD0	H
J	IRQ1 FEC7	IRQ1 FEC6	IRQ1 FEC4	IRQ1 FEC3	BOOT MOD1	IVDD	VSS	VSS	VSS	VSS	IVDD	EVDD	IRQ1 DEBUG0	RMII0_ TXD0	RMII0_ TXD1	RMII0_ RXER	J
K	IRQ1 FEC2	IRQ1 FEC1	I2C_ SDA	IRQ1 FEC5	NC	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	T1IN	IRQ1 DEBUG3	IRQ1 DEBUG1	RMII0_ TXEN	K
L	IRQ1 FEC0	VSTBY_ SRAM	SIM0_ DATA	VSTBY_ RTC	EVDD	EVDD	EVDD	IVDD	IVDD	EVDD	EVDD	EVDD	IRQ06	SIM0_ PD	TRST	T0IN	L
M	I2C_ SCL	SIM0_ VEN	RESET	VDD_ OSC_A_ PLL	EVDD	EVDD	EVDD	JTAG_ EN	VDD_ EPM	NC	NC	EVDD	NC	TMS	TDO	SIM0_ CLK	M
N	RST OUT	DSPI_ PCS2	SSI_ RXD	SDHC_ DAT3	SDHC_ DAT0	SDHC_ DAT1	CODEC _VAG	AVDD_ CODEC	CODEC _BGR VREF	VSS_ CODEC	FB_A4	FB_A10	FB_A13	FB_A20	FB_A19	FB_A22	N
P	RTC_ EXTAL	DSPI_ PCS3	SSI_ TXD	SSI_ MCLK	SSI_ BCLK	CODEC _REG BYP	CODEC _REFP	CODEC _REFN	CODEC _ADCP	CODEC _ADCN	FB_A5	FB_A9	FB_A16	FB_A17	FB_A18	FB_A23	P
R	RTC_ XTAL	SSI_FS	SDHC_ CLK	SDHC_ CMD	SDHC_ DAT2	CODEC _DACP	CODEC _DACN	AMP_ HP OUT	AMP_ HP DUMMY	FB_A2	FB_A6	FB_A12	FB_A11	FB_A14	FB_A15	FB_A21	R
T	VSS	EXTAL	XTAL	TDI	TCLK	AVSS_ SPKR_ HDST	AMP_ SPKRP	AVDD_ SPKR	AMP_ SPKRN	AVSS_ SPKR_ HP	FB_A1	FB_A0	FB_A3	FB_A8	FB_A7	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7. MCF53014, MCF53015, MCF53016, and MCF53017 Pinout (256 MAPBGA)

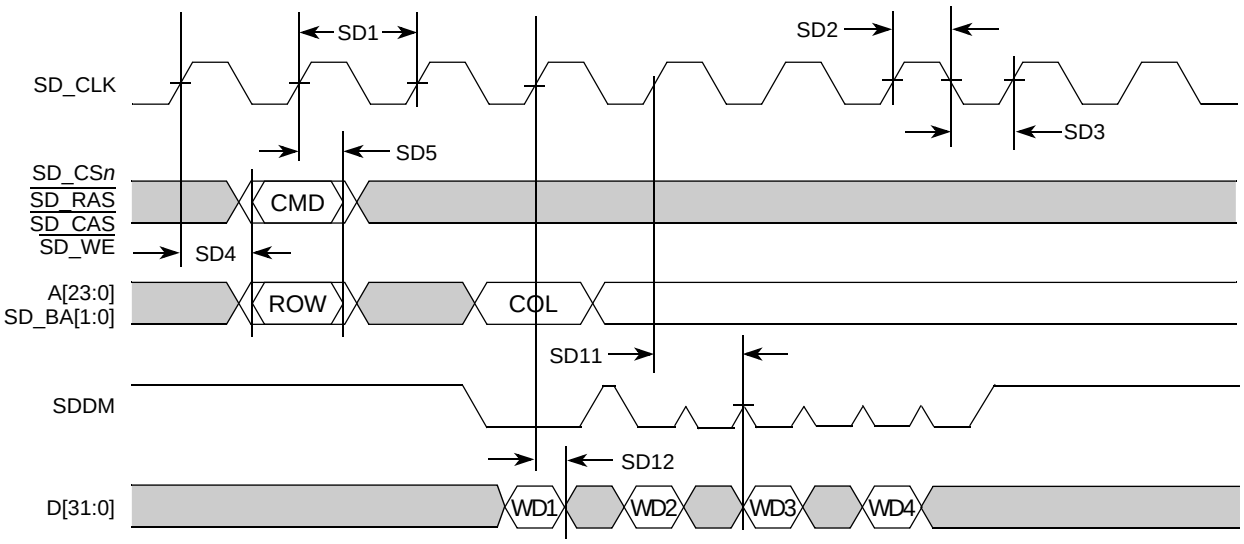


Figure 13. SDR Write Timing

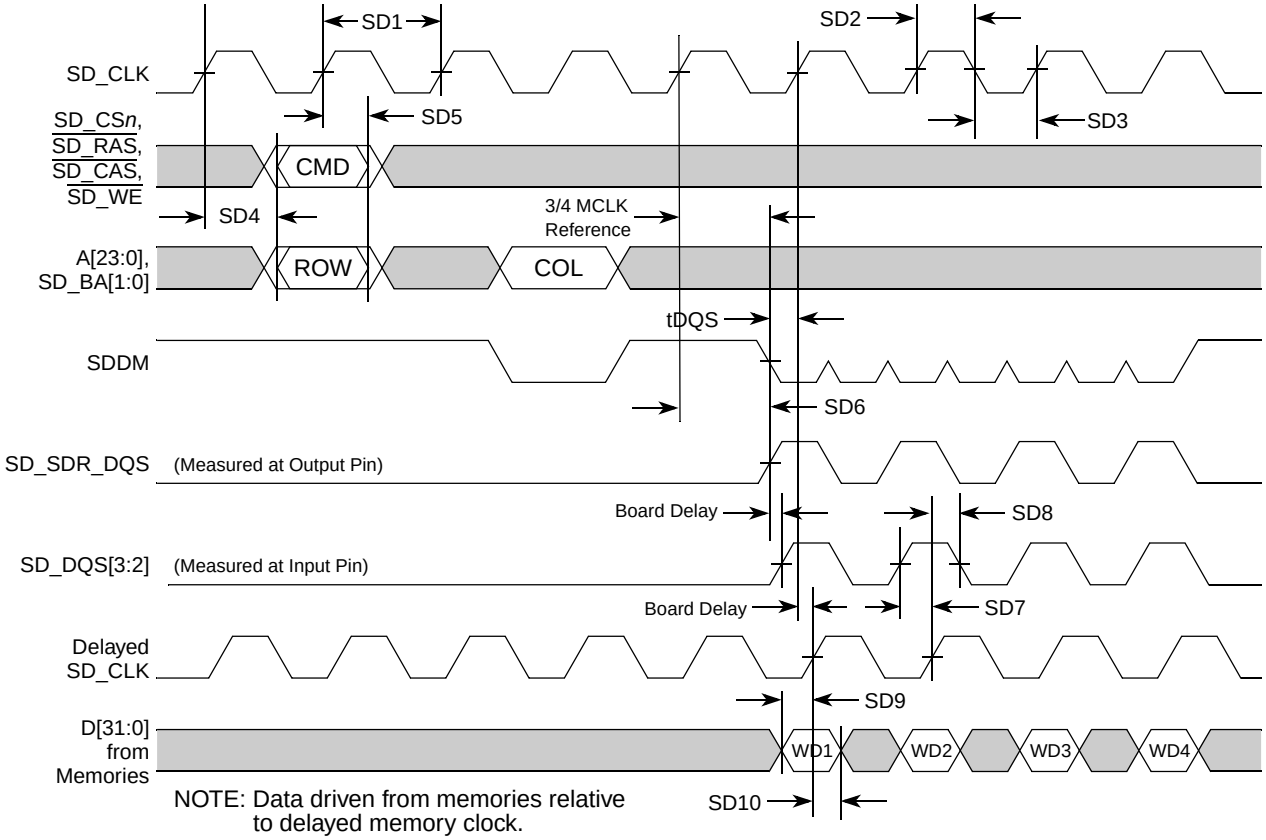


Figure 14. SDR Read Timing

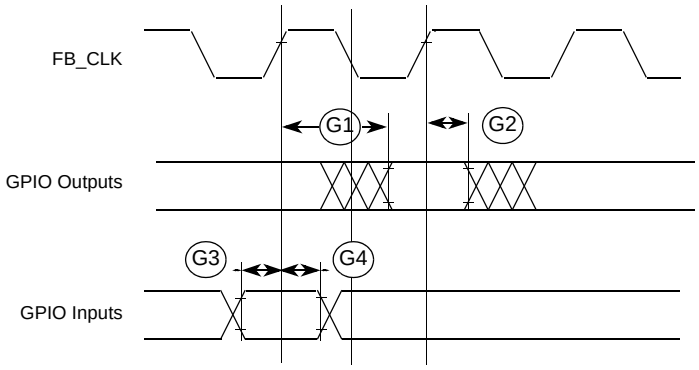


Figure 18. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 16. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

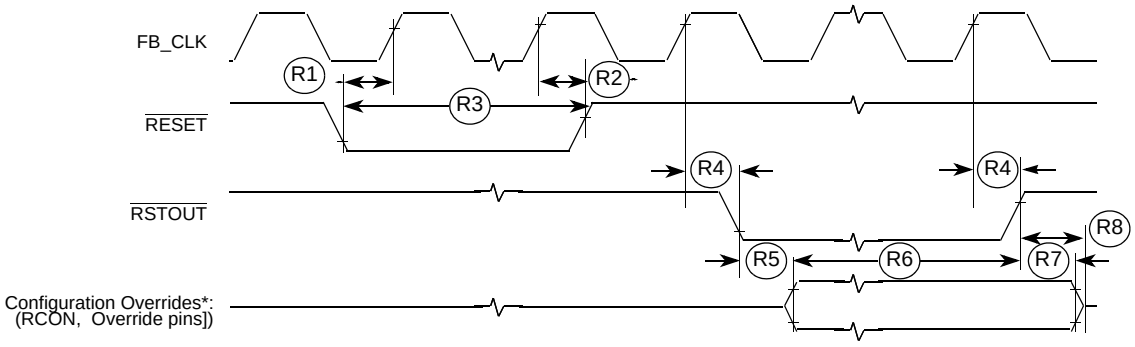


Figure 19. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5301x Reference Manual* for more information.

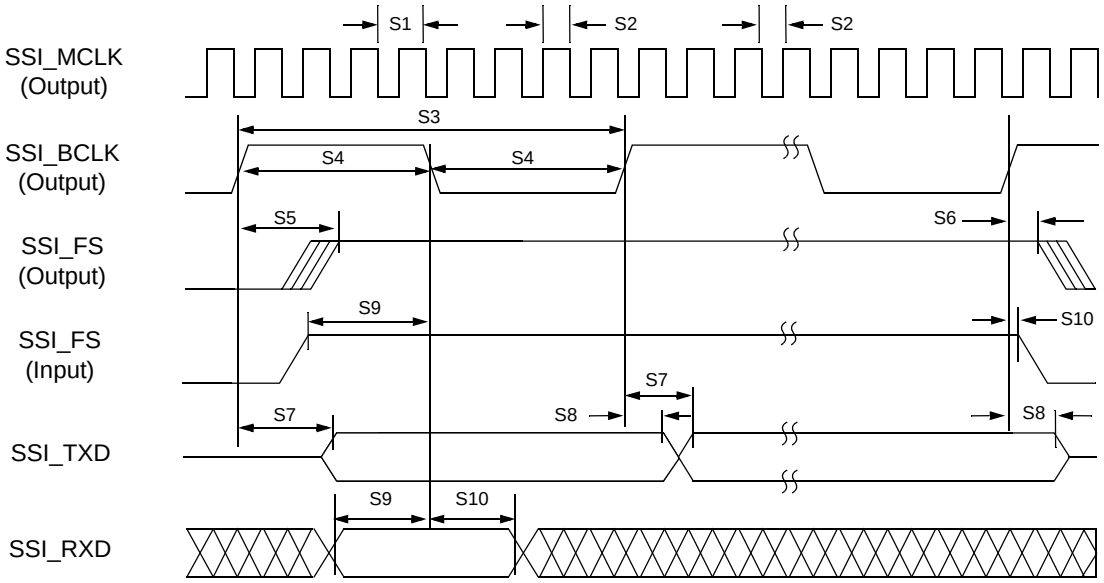


Figure 20. SSI Timing — Master Modes

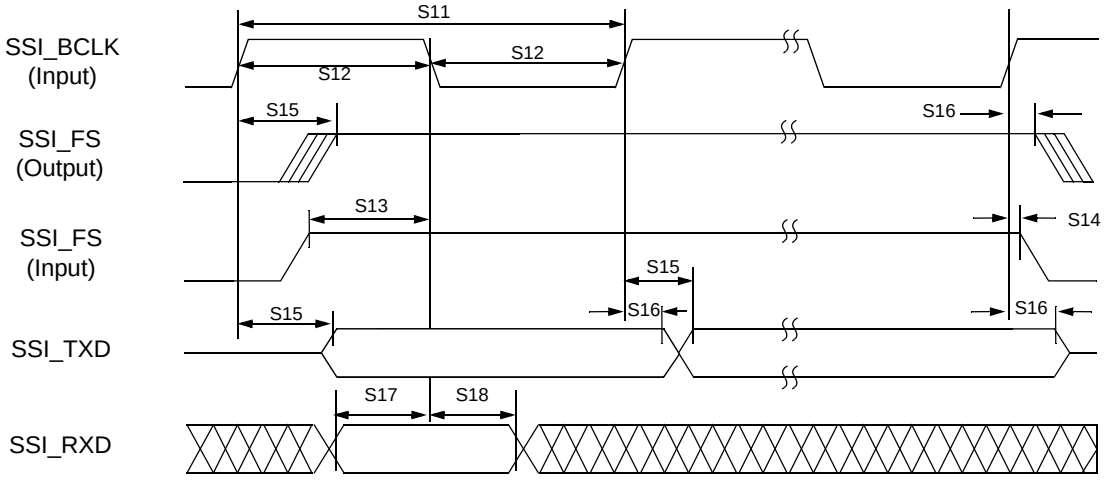


Figure 21. SSI Timing — Slave Modes

5.12 I²C Input/Output Timing Specifications

Table 19 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 19. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

5.13 Fast Ethernet AC Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for both MII and 7-Wire style interfaces for a range of transceiver devices.

Table 21. Receive Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	4	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	2	—	ns
E3	RXCLK pulse width high	35%	65%	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	35%	65%	RXCLK period

1 In MII mode, n = 3; In RMII mode, n = 1

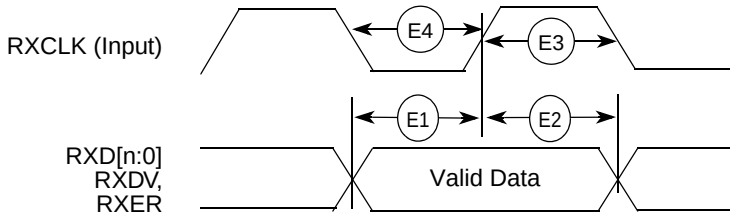


Figure 23. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 22. Transmit Signal Timing

Num	Characteristic	MII Mode		RMII Mode		Unit
		Min	Max	Min	Max	
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	—	10	ns
E7	TXCLK pulse width high	35%	65%	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	35%	65%	t_{TXCLK}

1 In MII mode, n = 3; In RMII mode, n = 1

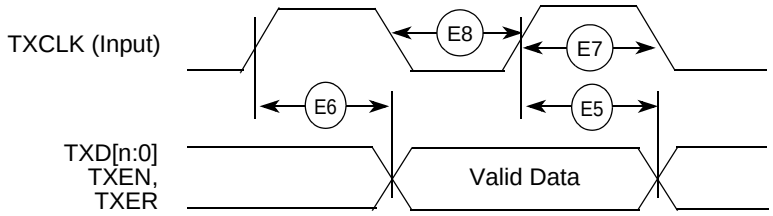


Figure 24. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 23. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

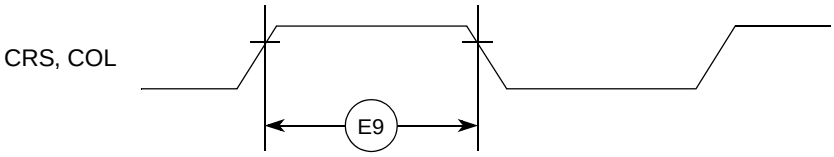


Figure 25. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 24. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

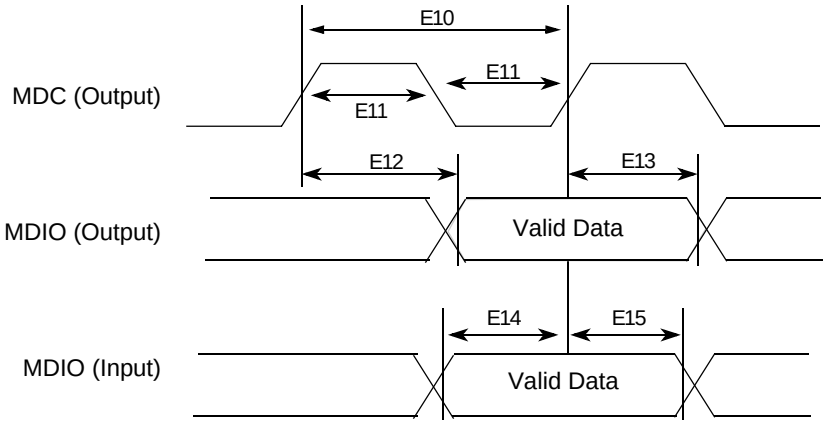


Figure 26. MII Serial Management Channel TIming Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 25 lists timer module AC timings.

Table 25. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with both master and slave operations. Many of the transfer attributes are programmable. Table 26 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF5301x Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. DSPI Module AC Timing Specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x t_{SYS}	—	ns	2
DS2	DSPI_SCK Duty Cycle	—	(tsck ÷ 2) – 2.0	(tsck ÷ 2) + 2.0	ns	3
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	(2 × t_{SYS}) – 1.5	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	(2 × t_{SYS}) – 3.0	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	4	ns	

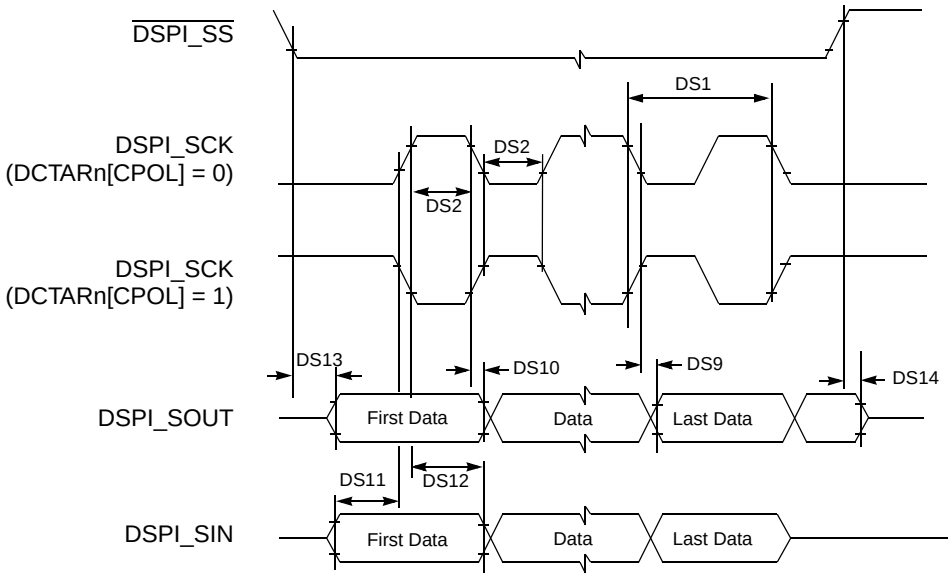


Figure 28. DSPI Classic SPI Timing — Slave Mode

5.16 eSDHC Electrical Specifications

This section describes the electrical information of the eSDHC.

5.16.1 eSDHC Timing

Figure 29 depicts the timing of eSDHC, and Table 29 lists the eSDHC timing characteristics.

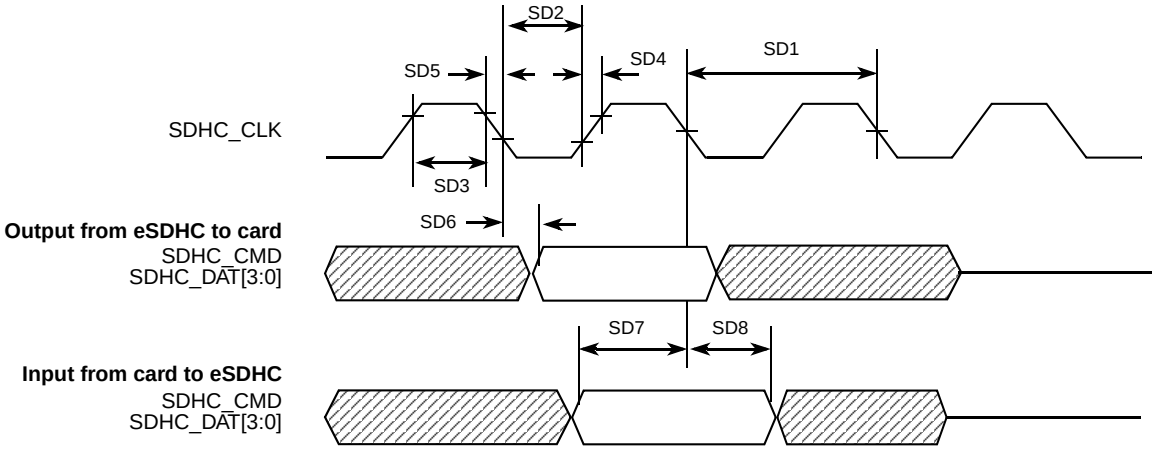


Figure 29. eSDHC Timing

Table 29. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK Rise Time [2]	S_{rise}	–	20	ns
3	SIM_CLK Fall Time [3]	S_{fall}	–	20	ns
4	SIM Input Transition Time (RX, SIM_PD)	S_{trans}	–	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

5.17.2 Reset Sequence

5.17.2.1 Cards with Internal Reset

The reset sequence for this kind of SIM card is as follows (see Figure 31):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

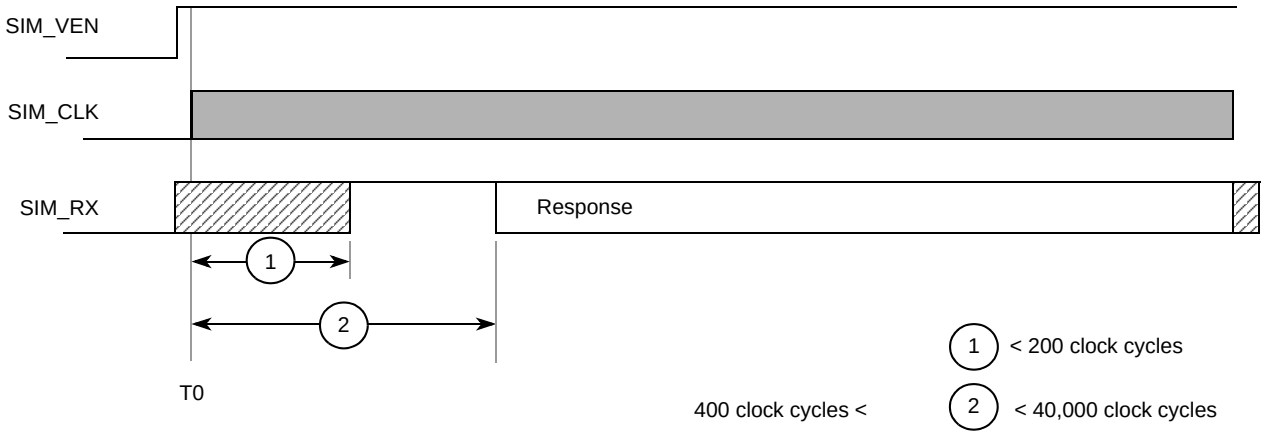


Figure 31. Internal-Reset Card Reset Sequence

5.17.2.2 Cards with Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 32):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

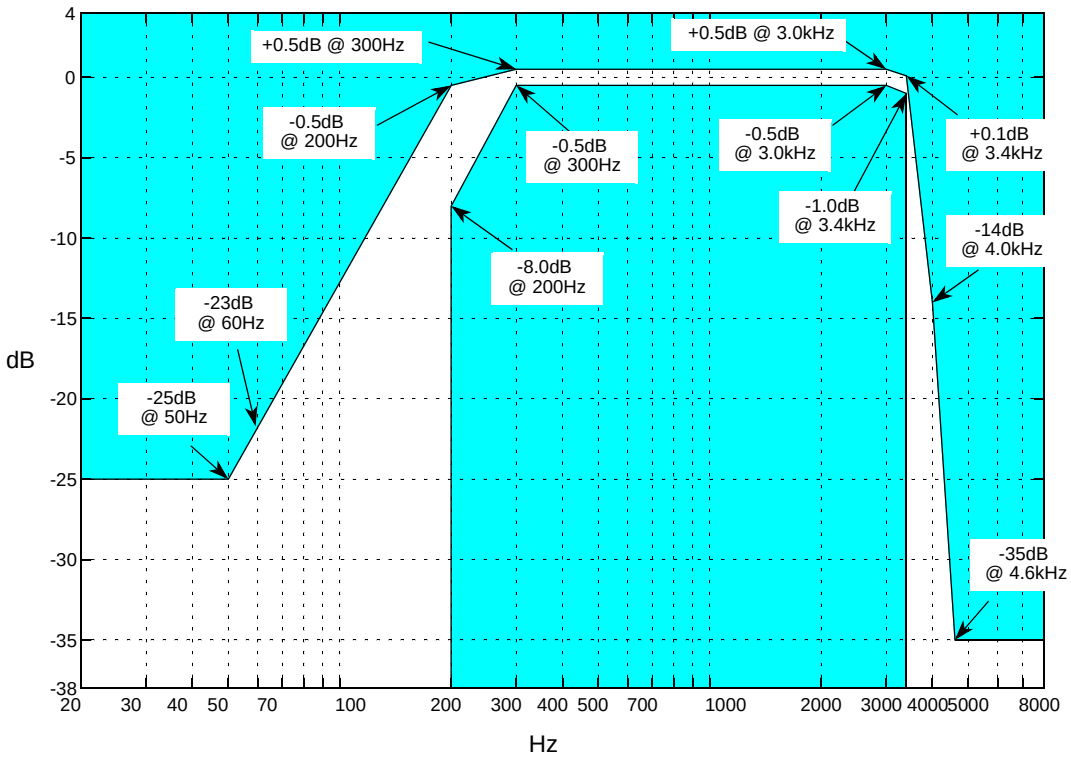


Figure 35. Voice Signal Frequency Response Requirements at the ADC Path (VCIHPF=1, HPF and LPF Together)

5.19.2 Voice Codec DAC Specifications

Voice-decoding function includes frequency ripple compensation, interpolation, digital-to-analog conversion, and anti-imaging filter. The input signal for the voice-decoding function is in linear 16-bit two's compliment PCM words at an 8 kHz or 8.1 kHz rate. Table 34 shows the voice decoding specifications.

Table 34. Voice Codec DAC Specifications[1]

Parameter	Condition	Min	Typ	Max	Units
Output Level	+3dbm0[2] (clipping level) on an individual differential output pin (CODEC_DACP or CODEC_DACN)	VAG–0.5	—	VAG+0.5	V
Output Source Impedance	10kΩ Load	—	100	—	Ω
Output Power Supply Rejection Ratio	20Hz to 100kHz with 100 mVrms, noise applied to AVDD (CODEC_REGBYP)	50	60	—	dBa
Absolute Gain	0dBm0@1.02kHz	–1.0	—	1.0	dB
Gain vs. Signal	–10dBm0@1.02kHz +3 to –40dBm0 –40 to –50dB –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Total Distortion (4 kHz noise BW in 300 Hz – 20 kHz measured BW out)	1.02 kHz tone (linear) +2 dBm0 0 dBm0 –6 dBm0 –10 dBm0 –20 dBm0 –30 dBm0 –40 dBm0 –45 dBm0 –55 dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[3] (At CODEC out)	A weighted to 20kHz	—	–78	–73	dBm0
	8kHz, 30Hz BW, D/A = zero code	No spurious			
Differential offset	T_A = 70 °C T_A = 25 °C	— —	— —	40 30	mV
Frequency Response VCOHPF = logic high (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 60Hz[4] 200Hz 300–3000Hz 3400Hz[5] 4000Hz 4600Hz	 — — –8 –0.5 –0.8 — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCOHPF = logic low (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300–3000Hz 3400Hz[6] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –0.8 — —	 — — — v — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Out-of-Band Spurious (Interpolation Image Suppression)	300 to 3400Hz @ 0dBm0 input 4600 to 7600Hz 7600 to 8400Hz 8400 to 20,000Hz	—	—	 –50 –50 –50	 dB dB dB
Crosstalk A/D to D/A	A/D = 0dBm0 @1.02kHz	—	—	–75	dB
Intermodulation Distortion	Two frequencies. of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Filter Group Delay VCOHPF = logic high CODEC_CLK=26 MHz (Relative to 1.6kHz)	500Hz < f < 600Hz 600Hz < f < 800Hz 800Hz < f < 1kHz 1kHz < f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	— — — — — — —	— — — — — — —	300 200 70 30 95 135 190	µs µs µs µs µs µs µs
Filter Group Delay VCOHPF = logic low CODEC_CLK=26 MHz (Relative to 1.6kHz)	f < 1.6kHz 1.6kHz < f < 2.6kHz 2.6kHz < f < 2.8kHz 2.8kHz < f < 3.0kHz	–40 0 — —	— — — —	0 100 160 200	µs µs µs µs
Filter Absolute Group Delay VCOHPF = logic high	f=1.6kHz	—	—	350	µs
Filter Absolute Group Delay VCOHPF = logic low	f=1.6kHz	—	—	320	µs

1 All analog signals are referenced to VAG unless otherwise noted. Output is 0dbm0 unless noted.

2 For D/A differential output (CODEC_DACP - CODEC_DACN) 0dBm0 = 500 mV_{rms}.

3 GSM Spec = –64.

4 Small frequency response deviation from straight line in the 60:200 Hz range is acceptable by spec requirements.

5 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

6 Small frequency response deviation from straight line in the 3400:4000 Hz range is acceptable by spec requirements.

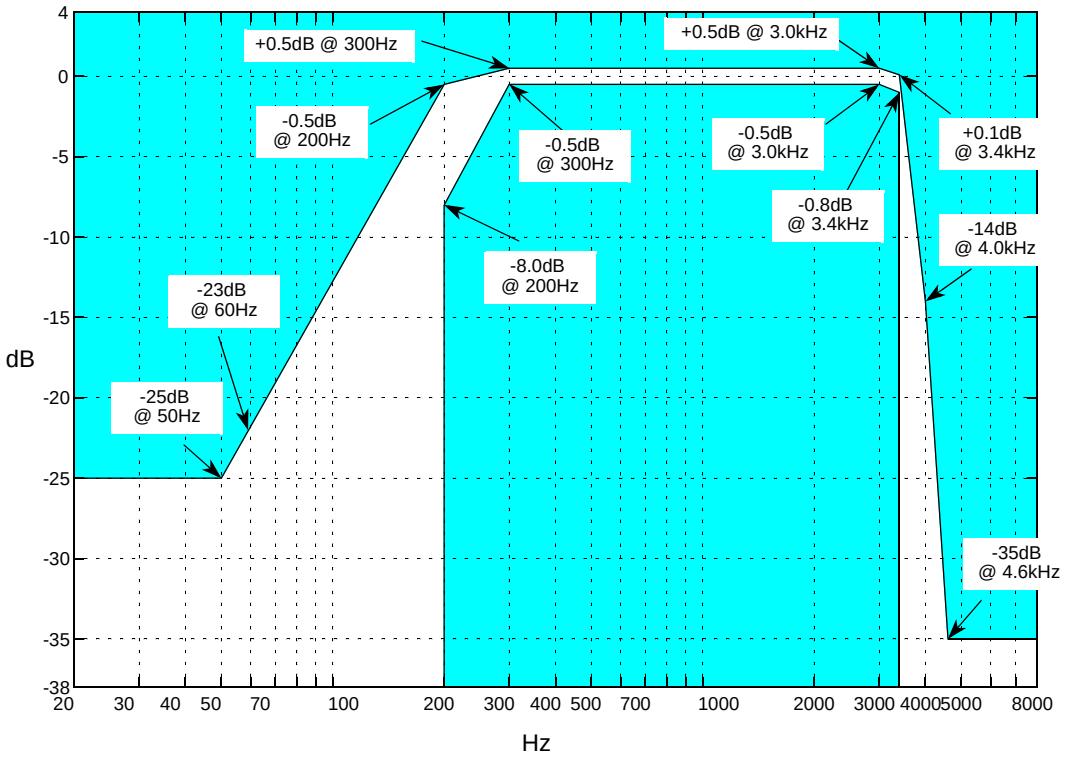


Figure 37. Voice Signal Frequency Response Requirements at the DAC Path (VCOHPF=1, HPF and LPF Together)

5.20 Integrated Amplifiers

5.20.1 Speaker Amplifier

The speaker amplifier boosts the power from the DAC and drives the speaker. It also provides analog volume control to optimize the noise performance of the entire channel. Table 35 shows the specifications for the speaker amplifier.

Table 35. Speaker Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	800	—	μA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Max Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 4Ω		—	600	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 4Ω, F_{in} = 1kHz	Full Power, 500mW	—	0.050	—	%
		Half Power, 250mW	—	0.050	—	
	Gain = 0dB, R_L = 4Ω, F_{in} = 4kHz	Full Power, 500mW	—	0.1	—	
		Half Power, 250mW	—	0.1	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	μV

Table 38. Microphone Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Total Harmonic Distortion (THD)	Gain = 0dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	%
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 0dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
Integrated Output Noise	BW = 20Hz – 20kHz	Gain = 0dB	—	12	—	µV
		Gain = 20dB	—	40	—	
Signal to Noise Ratio (SNR)	V_{OUT} = 0.5V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	92.4	—	dB
		Gain = 20dB	—	81.9	—	
THD plus Noise	V_{OUT} = 0.35V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	80	—	dB
		Gain = 20dB	—	80	—	
Power Supply Rejection Ratio	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 1kHz	—	60	—	dB
		f = 4kHz	—	60	—	
Commom Mode Rejection Ratio	Gain = 0dB, V_{ripple} = 100mV_{pp}	f = 1kHz	—	50	—	dB
		f = 4kHz	—	50	—	
Gain Error	Gain = 0, 6, 9.56, 15.56, 20, 24, 29.56, 39.9 dB		—	±0.5	—	dB
Input Impedance	Depends on the Gain Setting		1.5	—	24.0	kΩ

5.21 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns

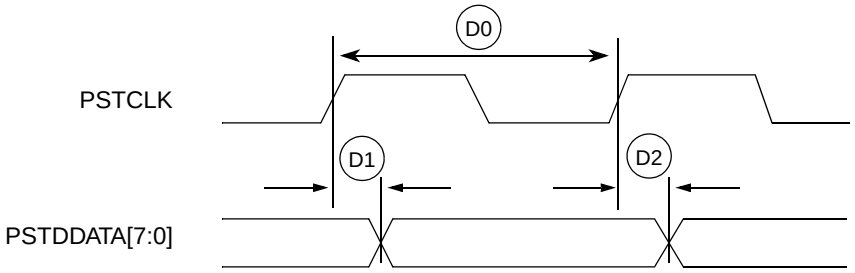


Figure 42. Real-Time Trace AC Timing

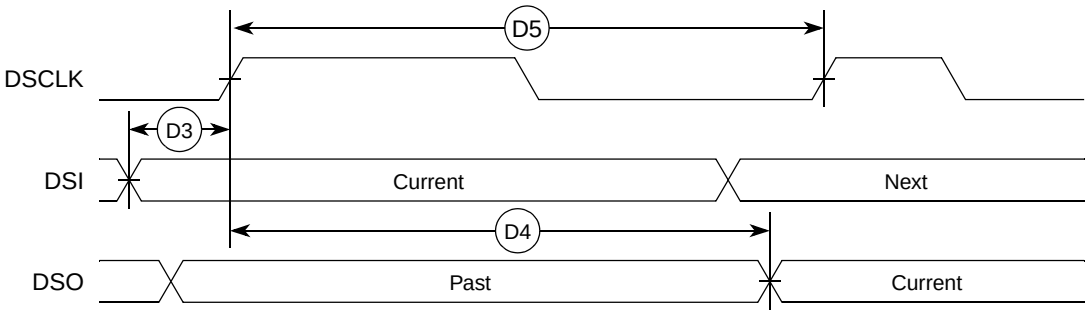


Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.