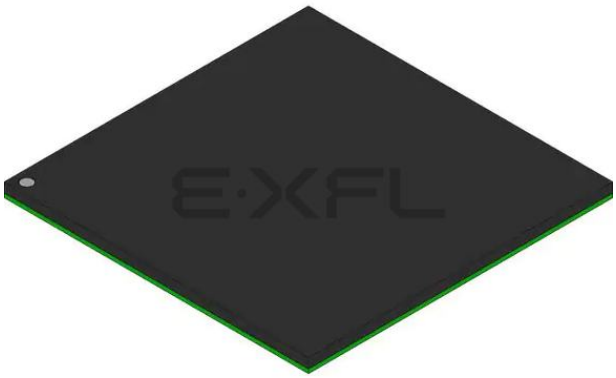

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53017cmj240j

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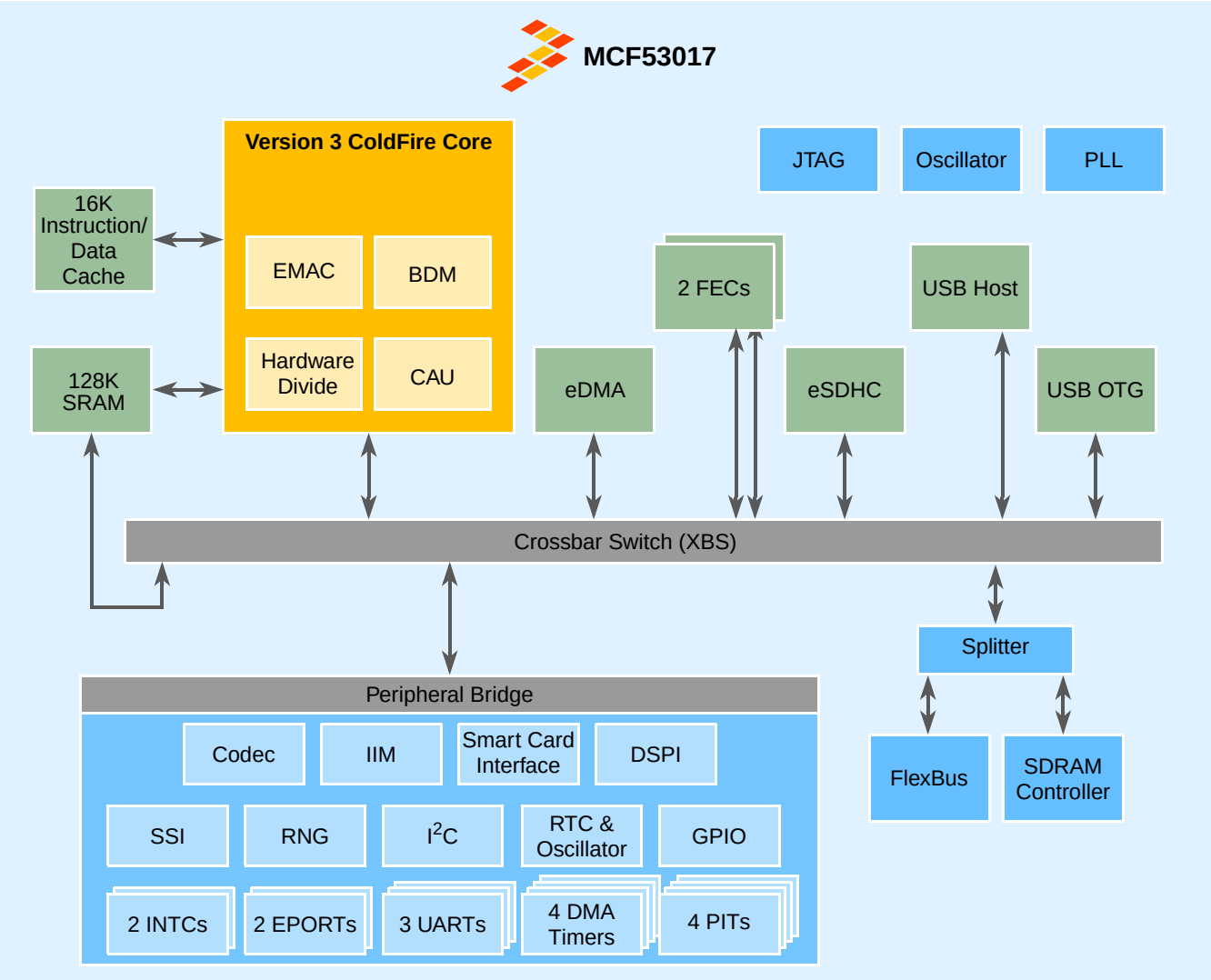

LEGEND

BDM	– Background debug module	**IIM**	– IC identification module
CAU	– Cryptography acceleration unit	**INTC**	– Interrupt controller
DSPI	– DMA serial peripheral interface	**JTAG**	– Joint Test Action Group interface
eDMA	– Enhanced direct memory access module	**PCI**	– Peripheral Component Interconnect
eSDHC	– Enhanced Secure Digital host controller	**PIT**	– Programmable interrupt timers
EMAC	– Enchanced multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random number generator
FEC	– Fast Ethernet Controller	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-Integrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

Table 1. MCF5301*x* Family Configurations (continued)

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
16-channel direct memory access (DMA)	•	•	•	•	•	•	•	•
General purpose I/O Module (GPIO)	•	•	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•	•	•
Package	208 LQFP				256 MAPBGA			

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF53010CQT240	MCF53010 Microprocessor	208 LQFP	240 MHz	–40° to +85° C
MCF53011CQT240	MCF53011 Microprocessor			
MCF53012CQT240	MCF53012 Microprocessor			
MCF53013CQT240	MCF53013 Microprocessor			
MCF53014CMJ240J	MCF53014 Microprocessor	256 MAPBGA		
MCF53015CMJ240J	MCF53015 Microprocessor			
MCF53016CMJ240J	MCF53016 Microprocessor			
MCF53017CMJ240J	MCF53017 Microprocessor			
The following are not available from Freescale for import or sale in the United States prior to September 2010				
MCF53014CMJ240	MCF53014 Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53015CMJ240	MCF53015 Microprocessor			
MCF53016CMJ240	MCF53016 Microprocessor			
MCF53017CMJ240	MCF53017 Microprocessor			

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 1 should be connected between the board IV_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated PV_{DD} pin as possible. The 10-ohm resistor in the given filter is required, do not implement the filter circuit using only capacitors. The PV_{DD} pins draw very little current, so concerns regarding voltage loss across the 10-ohm resistor are not valid.

Table 6. MCF5301*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	41	M3
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	42	N1
Clock								
EXTAL	—	—	—	—	I	EVDD	49	T2
XTAL	—	—	—	U[3]	O	EVDD	50	T3
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	55, 17	J5, G5
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[3:2]	—	—	O	SDVDD	115, 114	P16, N16
FB_A[21:16]	—	—	—	—	O	SDVDD	113–108	R16, N14, N15, P15-13
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	107, 106	R15, R14
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	105–103	N13, R12, R13
FB_A10	—	—	—	—	O	SDVDD	100	N12
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	99–97 95–89	P12, T14, T15, R11, P11, N11, T13, R10, T11, T12
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	208–198, 57–62, 64, 65	B3, A2, D6, C5, B4, A3, B5, C6, D12, C14, B14, C13, D11, B13, A14, A13
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	182–189, 177–170	B9, A9, A8, D7, B8, C8, D8, B7, C10, A10, B10, D10, C11, A11, B11, A12
FB_CLK	—	—	—	—	O	SDVDD	153	D13
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	197, 166, 179, 178	A4, B12, C9, D9
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	—	O	SDVDD	—	B6, C7
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	5	D2
$\overline{\text{FB\_CS0}}$	PCS0	$\overline{\text{FB\_CS4}}$	—	—	O	SDVDD	6	C2
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	1	D4
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	3	B2
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	2	C3
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	4	D3
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	206	C4

4.2 Pinout—208 LQFP

The pinout for the 208 LQFP devices is shown in Figure 5 and Figure 6.

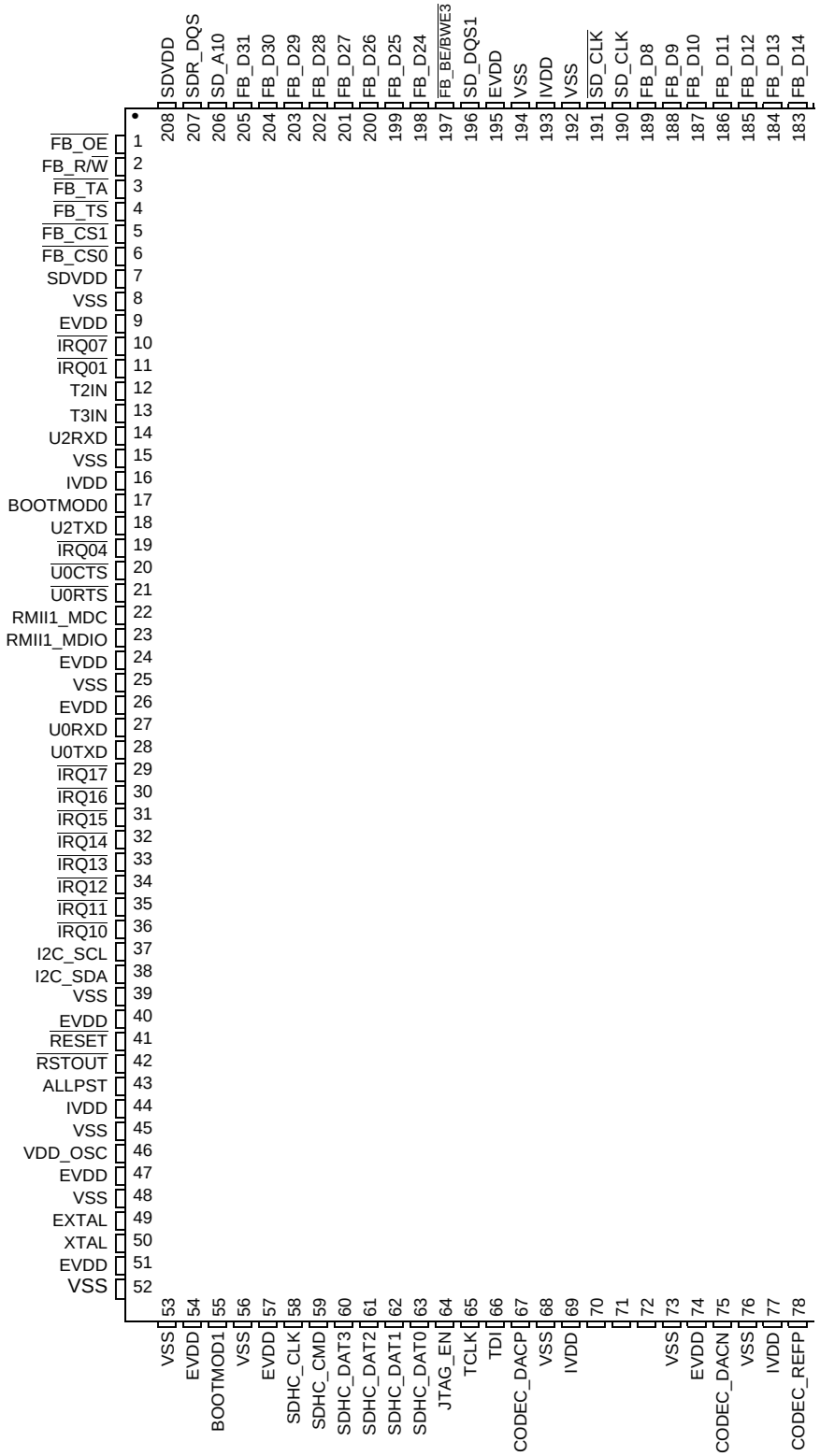

Figure 5. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Left (208 QFP)

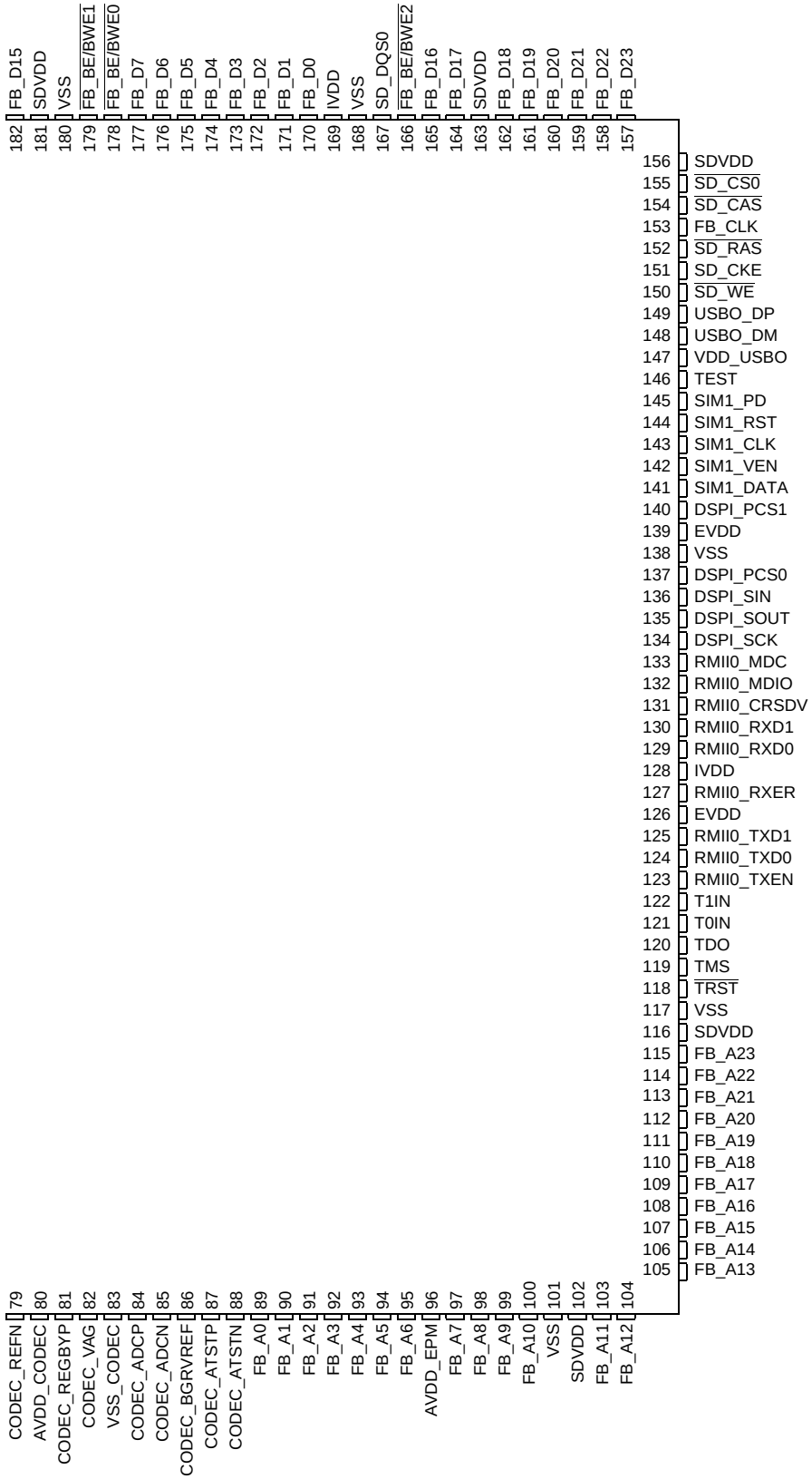

Figure 6. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Right (208 QFP)

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JEDEC JESD22-A114 specification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.08	1.32	V
SRAM Standby Voltage	$SRAMV_{STBY}$	1.08	1.32	V
RTC Standby Voltage	$RTCV_{STBY}$	3.0	3.6	V
PLL Supply Voltage	$PLLV_{DD}$	3.0	3.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	$0.51 \times EV_{DD}$	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	EV_{IL}	$V_{SS} - 0.3$	$0.42 \times EV_{DD}$	V
CMOS Output High Voltage I_{OH} = –2.0 mA	EV_{OH}	$0.8 \times EV_{DD}$	—	V
CMOS Output Low Voltage I_{OL} = 2.0 mA	EV_{OL}	—	$0.2 \times EV_{DD}$	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 $SDV_{DD} \times 0.7$ Vref+0.15 2	 SDV_{DD}+0.3 SDV_{DD}+0.3 $SDV_{DD} + 0.3$	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 –0.3 –0.3 $V_{SS} - 0.3$	 $SDV_{DD} \times 0.3$ Vref+0.15 0.8	V

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100kHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 12 are shown in Figure 11 and Figure 12.

* The timings are also valid for inputs sampled on the negative clock edge.

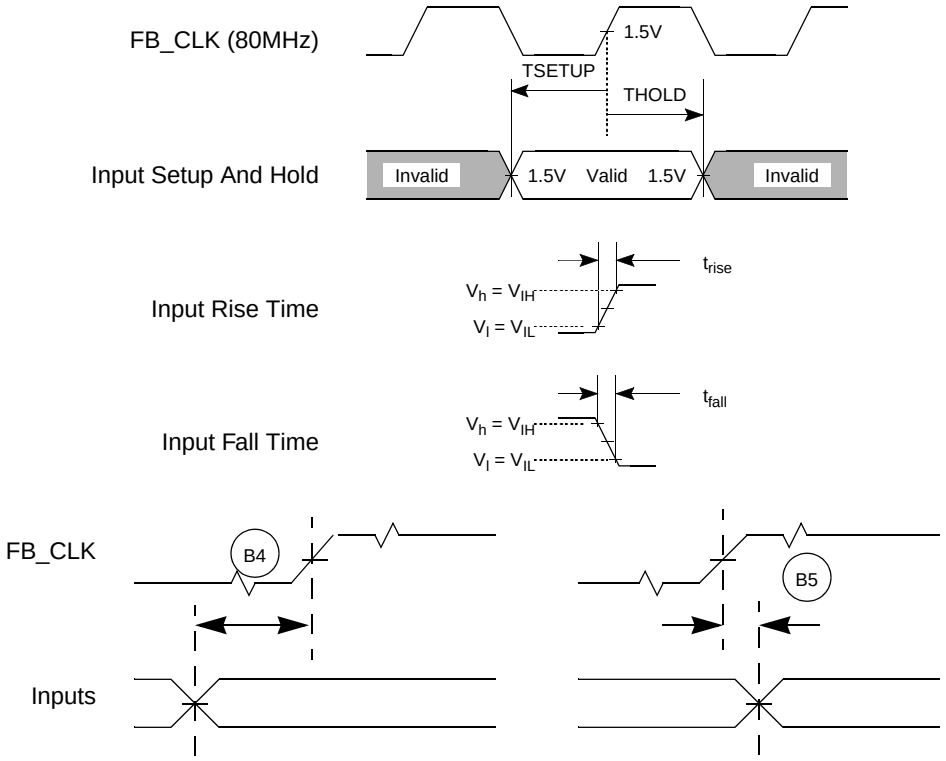

Figure 10. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces.

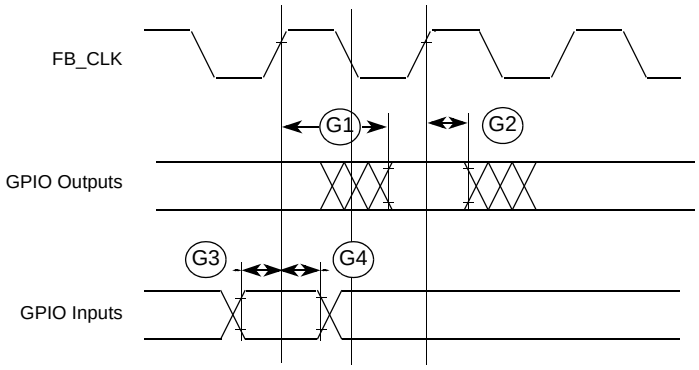

Figure 18. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 16. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

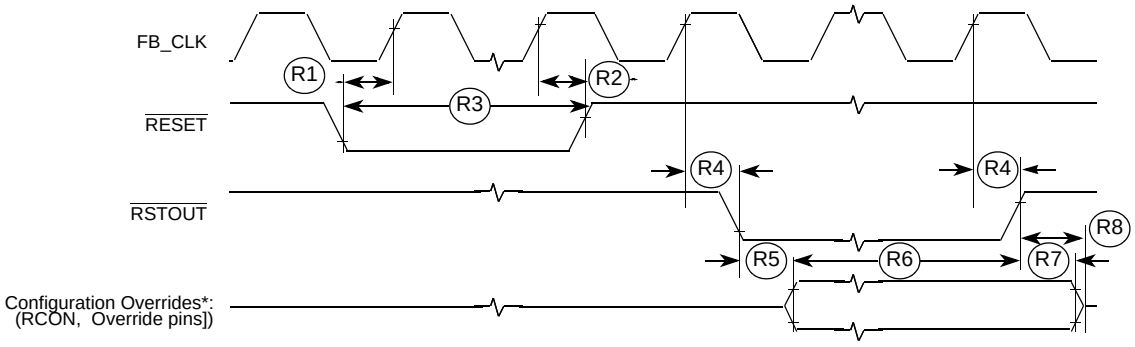

Figure 19. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5301x Reference Manual* for more information.

Table 29. SIM Timing Specification—High Drive Strength

Num	Description	Symbol	Min	Max	Unit
1	SIM Clock Frequency (SIM_CLK)[1]	S_{freq}	0.01	5 (Some new cards may reach 10)	MHz
2	SIM_CLK Rise Time [2]	S_{rise}	–	20	ns
3	SIM_CLK Fall Time [3]	S_{fall}	–	20	ns
4	SIM Input Transition Time (RX, SIM_PD)	S_{trans}	–	25	ns

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

5.17.2 Reset Sequence

5.17.2.1 Cards with Internal Reset

The reset sequence for this kind of SIM card is as follows (see Figure 31):

- After powerup, the clock signal is enabled on SIM_CLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40,000 clock cycles after T0.

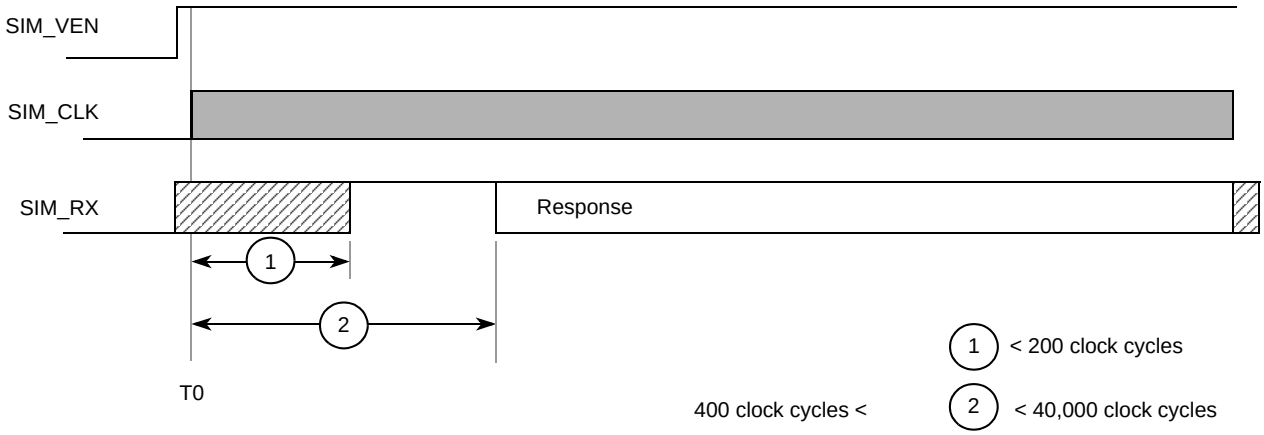

Figure 31. Internal-Reset Card Reset Sequence

5.17.2.2 Cards with Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 32):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

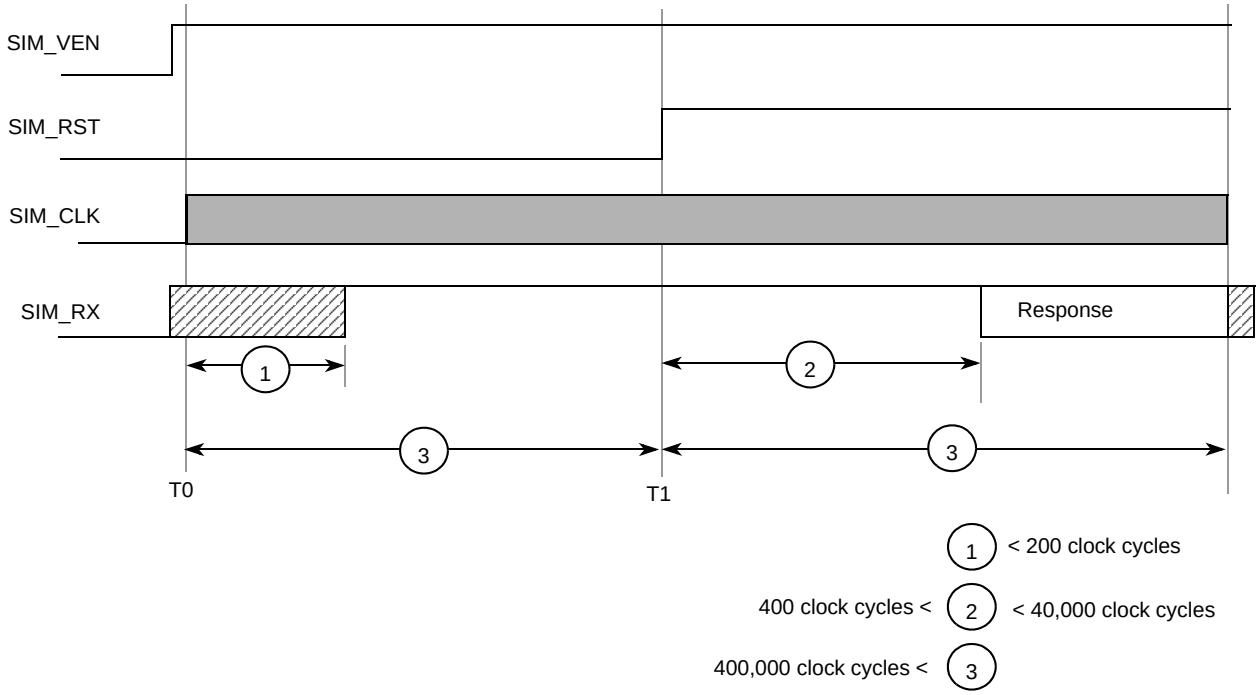

Figure 32. Active-Low-Reset Card Reset Sequence

5.17.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIM_PD port detects the removal of the SIM card
2. SIM_RST goes low
3. SIM_CLK goes low
4. SIM_TX goes low
5. SIM_VEN goes low

Each of these steps is completed in one CKIL period (usually 32 kHz). Power-down may be started in response to a card-removal detection or launched by the processor. Figure 33 and Table 30 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

Table 30. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 ÷ f_{CKIL}	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8 ÷ f_{CKIL}	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7 ÷ f_{CKIL}	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9 ÷ f_{CKIL}	25	ns

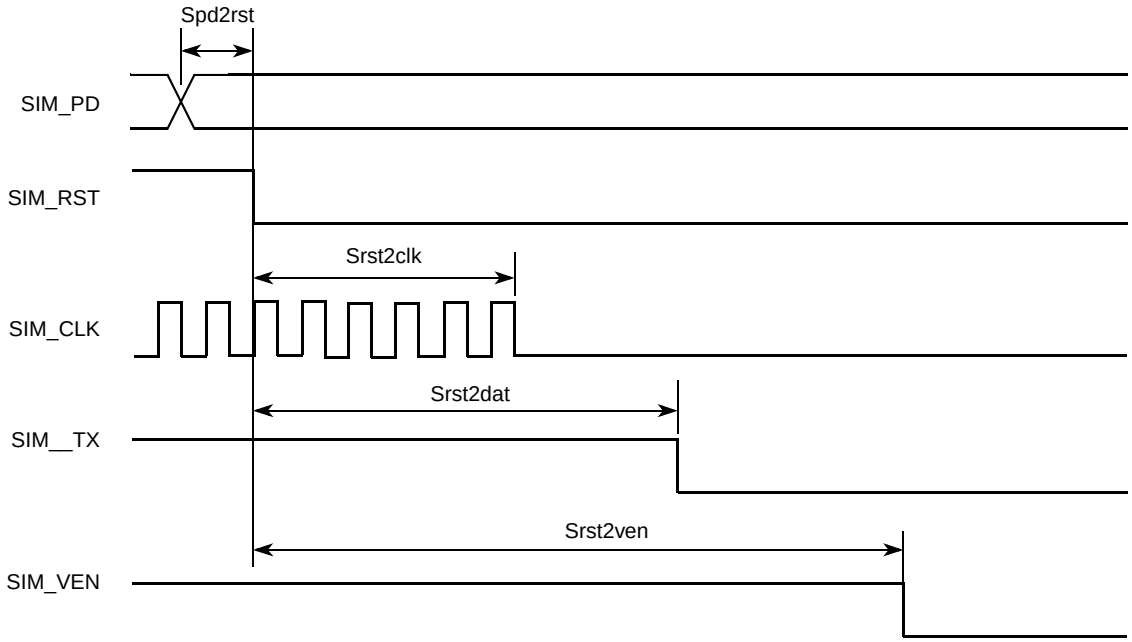

Figure 33. SmartCard Interface Power-Down AC Timing

5.18 IIM/Fusebox Electrical Specifications

Table 31. IIM/Fusebox Timing Characteristics

Num	Description	Symbol	Min	Max	Unit
1	Program time for eFuse[1]	$t_{program}$	125	—	µs

[1] The program length is defined by the value defined in IIM_FCR[PRG_LENGTH] of the IIM module. The value to program is based on a 32 kHz clock source (4 ÷ 32 kHz = 125 µs)

5.19 Voice Codec

The voice codec function is analog-to-digital and digital-to-analog conversion of the voice signal. The following section contains detailed electrical specifications for the analog and digital parts' performance. The voice codec is powered down when not enabled for power consumption.

Table 32 shows the voice codec general specifications.

Table 32. Voice Codec General Specifications

Parameter	Condition	Min	Typ	Max	Units
CODEC Input clock CODEC_CLK	VCLK[2:0]=0 VCLK[2:0]=1,2 VCLK[2:0]=3 VCLK[2:0]=4 VCLK[2:0]=5 VCLK[2:0]=6 VCLK[2:0]=7	— — — — — — —	16.8 19.44 20.0 24.0 26.0 28.0 30.0	— — — — — — —	MHz MHz MHz MHz MHz MHz MHz
VAG input Voltage	No Load, AVDD (CODEC_REGBYP) = 2.5V	1.225	1.325	1.425	V
Ref_Codec_p		TBD	1.665	TBD	V
Ref_Codec_n		TBD	0.985	TBD	V
VAG External Cap		—	0.1	—	µF
avoco_ref_codec_p External Cap		—	0.1	—	µF
avoco_ref_codec_n External Cap		—	0.1	—	µF
avoco_vagout_codec External Cap		—	0.1	—	µF
Codec Analog Supply Current (includes Rx and Tx paths)	AVDD (CODEC_REGBYP) = 2.5V, operational	—	5	6	mA
	Power-down mode	—	—	5	µA
Codec Digital Supply Current[1]	Operational mode	—	—	1	mA
Response to input ON/OFF (settling time at turn on)		—	—	1	ms

1 More accurate estimation will be given after some progress in design.

5.19.1 Voice Codec ADC Specifications

Voice coding function includes a 50 kHz second-order, low-pass anti-aliasing filter, an analog-to-digital converter, digital filters for decimation, band-passing, frequency ripple compensation, and DSP interface logic. The audio input A/D converter converts the incoming signal to 13-bit two's-compliment linear PCM words at an 8 or 8.1 kHz rate. Following the A/D converter, the signal is digitally filtered, low-pass, and selectable high-pass. Table 33 shows the voice coding specifications.

Table 33. Voice Codec ADC Specifications[1]

Parameter	Condition	Min	Typ	Max	Units
Power Supply Rejection Ratio with respect to AVDD (CODEC_REGBYP)[2]	20Hz to 100kHz, with 100 mV_{pp} noise applied to AVDD, with an external VAG cap	50	60	—	dB
Peak Input	(+3dBm0)[3] on an individual differential pin (ADC_P or ADC_M)	VAG–0.34	—	VAG+0.34	V
Tx AC Input Impedance	f=1.02kHz	100	—	—	kΩ
Absolute Gain	0dBm0@1.02kHz	–1.0	—	1.0	dB

Table 33. Voice Codec ADC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Gain vs. Signal	Relative to –10dBm0 @1.02kHz +3 to –40dBm0 –40 to –50dBm0 –50 to –55dBm0	 –0.25 –1.2 –1.3	 — — —	 0.25 1.2 1.3	 dB dB dB
Total Distortion (noise and harmonic) (300Hz – 20kHz Noise BW in 300Hz – 4kHz measured BW out)	1.02kHz tone (linear) +2dBm0[4] 0dBm0 –6dBm0 –10dBm0 –20dBm0 –30dBm0 –40dBm0 –45dBm0 –55dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[5]	Psophometric Weighting at the output	—	—	–72	dBm0p
Digital Offset[6]		—	—	5	%Full Scale
Frequency Response VCIHPF = logic high	Relative to 0dBm0@1.02kHz 50Hz 60Hz[7] 200Hz 300 to 3000Hz 3400Hz[8] 4000Hz 4600Hz	 –8 –0.5 –1.0 — — — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCIHPF=logic low	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300 to 3000Hz 3400Hz[9] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –1.0 — —	 — — — — — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Crosstalk D/A to A/D	D/A = 0 dBm0 @1.02kHz Measured while stimulated w/ 2667Hz @–50dBm0	—	—	–75	dB
Intermodulation Distortion	Two frequencies of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

Table 34. Voice Codec DAC Specifications[1] (continued)

Parameter	Condition	Min	Typ	Max	Units
Total Distortion (4 kHz noise BW in 300 Hz – 20 kHz measured BW out)	1.02 kHz tone (linear) +2 dBm0 0 dBm0 –6 dBm0 –10 dBm0 –20 dBm0 –30 dBm0 –40 dBm0 –45 dBm0 –55 dBm0	 57 60 60 55 45 35 25 20 15	 60 64 70 65 55 45 35 30 20	 — — — — — — — — —	 dB dB dB dB dB dB dB dB dB
Idle Channel Noise[3] (At CODEC out)	A weighted to 20kHz	—	–78	–73	dBm0
	8kHz, 30Hz BW, D/A = zero code	No spurious			
Differential offset	T_A = 70 °C T_A = 25 °C	— —	— —	40 30	mV
Frequency Response VCOHPF = logic high (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 60Hz[4] 200Hz 300–3000Hz 3400Hz[5] 4000Hz 4600Hz	 — — –8 –0.5 –0.8 — —	 — — — — — — —	 –25 –23 –0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB dB
Frequency Response VCOHPF = logic low (Min. limit valid for CODEC_CLK=26MHz)	Relative to 0dBm0@1.02kHz 50Hz 200Hz 300–3000Hz 3400Hz[6] 4000Hz 4600Hz	 –0.5 –0.5 –0.5 –0.8 — —	 — — — v — —	 +0.5 +0.5 +0.5 +0.1 –14 –35	 dB dB dB dB dB dB
Inband Spurious	1.02kHz @ 0dBm0, 300 to 3kHz	—	—	–48	dB
Out-of-Band Spurious (Interpolation Image Suppression)	300 to 3400Hz @ 0dBm0 input 4600 to 7600Hz 7600 to 8400Hz 8400 to 20,000Hz	—	—	 –50 –50 –50	 dB dB dB
Crosstalk A/D to D/A	A/D = 0dBm0 @1.02kHz	—	—	–75	dB
Intermodulation Distortion	Two frequencies. of amplitudes –4 to –21 dBm0 from the range 300 to 3400Hz	—	—	–41	dB

5.20.3 Headphone Amplifier

The headphone amplifier boosts the power from the DAC and drives the headphone. It also provides analog volume control to optimize the noise performance of the entire channel. Table 37 shows the specifications for the microphone amplifier.

Table 37. Headphone Amplifier Specifications

Parameter	Conditions		Min	Typ	Max	Units
Quiescent Current			—	600	—	µA
Shutdown Current			—	TBD	—	
Input Reference Offset			—	2	5	mV
Output Power	F_{in} = 1kHz, THD+N = 1%, R_L = 16Ω		—	40	—	mW
Total Harmonic Distortion (THD)	Gain = 0dB, R_L = 16Ω, BW = 200Hz – 4kHz	Full Power, 31.25mW	—	0.05	—	%
		Half Power, 16.5mW	—	0.05	—	
Integrated Output Noise	Gain = 0dB, BW = 20Hz – 20kHz		—	15	—	µV
Signal to Noise Ratio (SNR)	Gain = 0dB, V_{OUT} = 0.7V_{RMS} , BW = 20Hz – 20kHz		—	93	—	dB
Power Supply Rejection Ratio (PSRR)	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 217Hz	—	60	—	dB
		f = 1kHz	—	60	—	
		f = 4kHz	—	60	—	
Maximum Cap Load Drive	No Sustained Oscillations		—	300	—	pF
Output SC Current			—	150	—	mA
Gain Error	Gain = –45, –21, –12, –6, –2, 0 dB		—	±0.5	—	dB

5.20.4 Microphone Amplifier

The microphone amplifier boosts the signal from the microphone and provides it to the ADC. The gain control present in the microphone amplifier helps in optimizing the noise performance of the entire channel. Table 38 shows the specifications for the microphone amplifier.

Table 38. Microphone Amplifier Specifications

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current		—	500	—	µA
Shutdown Current		—	TBD	—	
Input Reference Offset		—	2	5	mV

Table 38. Microphone Amplifier Specifications (continued)

Parameter	Conditions		Min	Typ	Max	Units
Total Harmonic Distortion (THD)	Gain = 0dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	%
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 1k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 0dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
	Gain = 20dB, Fin = 4k	V_{OUT} = 0.5V_{RMS}	—	0.01	—	
		V_{OUT} = 0.35V_{RMS}	—	0.01	—	
Integrated Output Noise	BW = 20Hz – 20kHz	Gain = 0dB	—	12	—	µV
		Gain = 20dB	—	40	—	
Signal to Noise Ratio (SNR)	V_{OUT} = 0.5V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	92.4	—	dB
		Gain = 20dB	—	81.9	—	
THD plus Noise	V_{OUT} = 0.35V_{RMS}, BW = 20Hz – 20kHz	Gain = 0dB	—	80	—	dB
		Gain = 20dB	—	80	—	
Power Supply Rejection Ratio	Gain = 0dB, V_{ripple} = 200mV_{pp}	f = 1kHz	—	60	—	dB
		f = 4kHz	—	60	—	
Commom Mode Rejection Ratio	Gain = 0dB, V_{ripple} = 100mV_{pp}	f = 1kHz	—	50	—	dB
		f = 4kHz	—	50	—	
Gain Error	Gain = 0, 6, 9.56, 15.56, 20, 24, 29.56, 39.9 dB		—	±0.5	—	dB
Input Impedance	Depends on the Gain Setting		1.5	—	24.0	kΩ

5.21 JTAG and Boundary Scan Timing

Table 39. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns

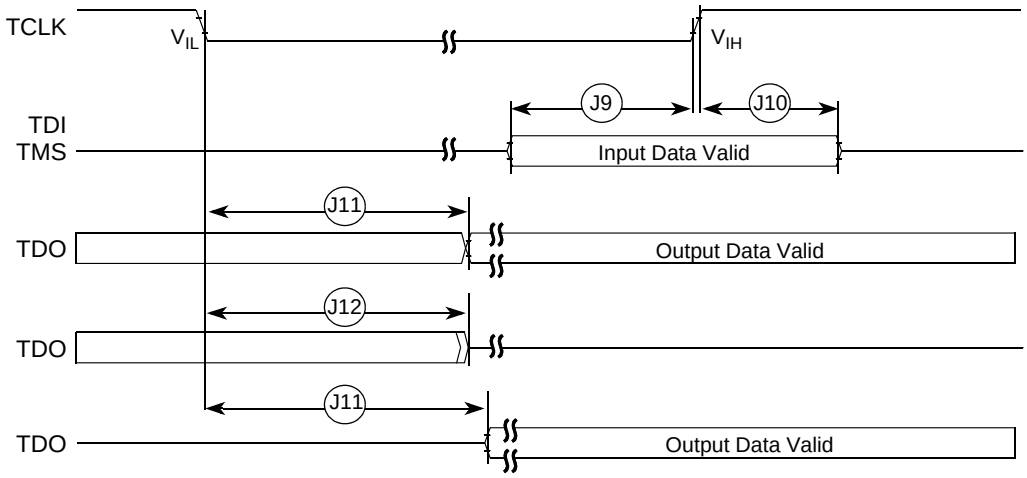

Figure 40. Test Access Port Timing

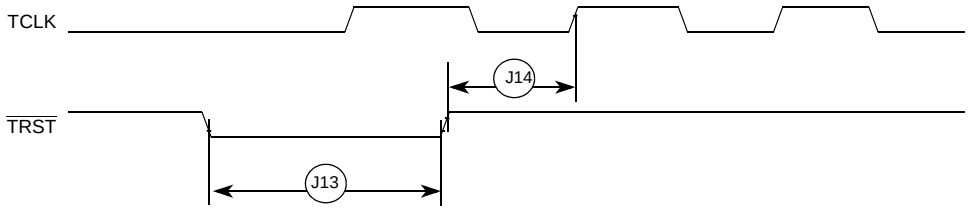

Figure 41. TRST Timing

5.22 Debug AC Timing Specifications

Table 40 lists specifications for the debug AC timing parameters shown in Figure 42.

Table 40. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1.5	1.5	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

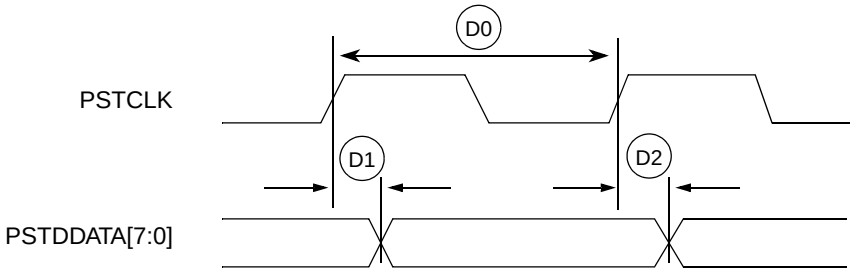

Figure 42. Real-Time Trace AC Timing

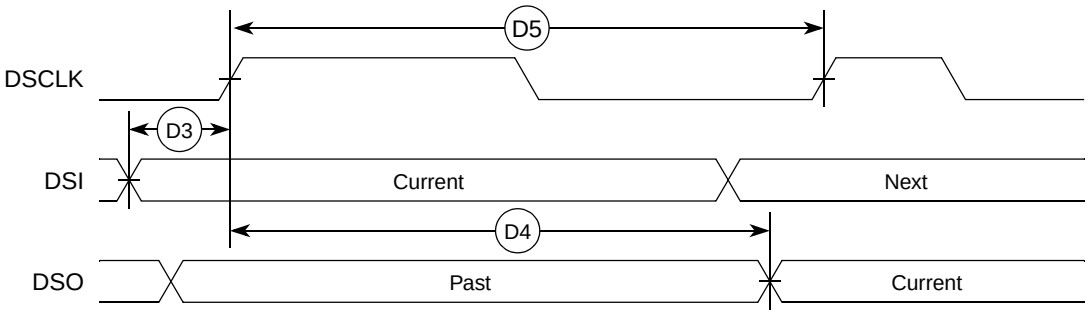

Figure 43. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the package case number per device. Use these numbers in the web page keyword search engine to find the latest package outline drawings.

Table 41. Package Information

Device	Package Type	Case Outline Number
MCF53010	208 LQFP	98ASS23458W
MCF53011		
MCF53012		
MCF53013		
MCF53014	256 MAPBGA	98ARH98219A
MCF53015		
MCF53016		
MCF53017		

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

8 Revision History

Table 42 summarizes revisions to this document.

Table 42. Revision History

Revision	Date	Location	Changes
3	12 Aug 2009	—	Initial public revision
4	10 Feb 2010	Table 8 Table 41	Added thermal characteristics for 208LQFP package Added 208LQFP case outline number
5	3 Mar 2010	Table 2	Added non-J suffixed part numbers for the 256MAPBGA package

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