Infineon Technologies - C167CSL40MCABXUMA2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167csl40mcabxuma2

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
P1L.0-7	118-125		
P1H.0-7	128-135		
P1L.0	118	I	AN16 Analog Input Channel 16
P1L.1	119	I	AN17 Analog Input Channel 17
P1L.2	120	I	AN18 Analog Input Channel 18
P1L.3	121	I	AN19 Analog Input Channel 19
P1L.4	122	I	AN20 Analog Input Channel 20
P1L.5	123	I	AN21 Analog Input Channel 21
P1L.6	124	I	AN22 Analog Input Channel 22
P1L.7	125	I	AN23 Analog Input Channel 23
P1H.4	132	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	133	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	134	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	135	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Note: When one or both of the on-chip CAN Modules are used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 ... A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CS's instructions can be executed in just one machine cycle which requires 50 ns at 40 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

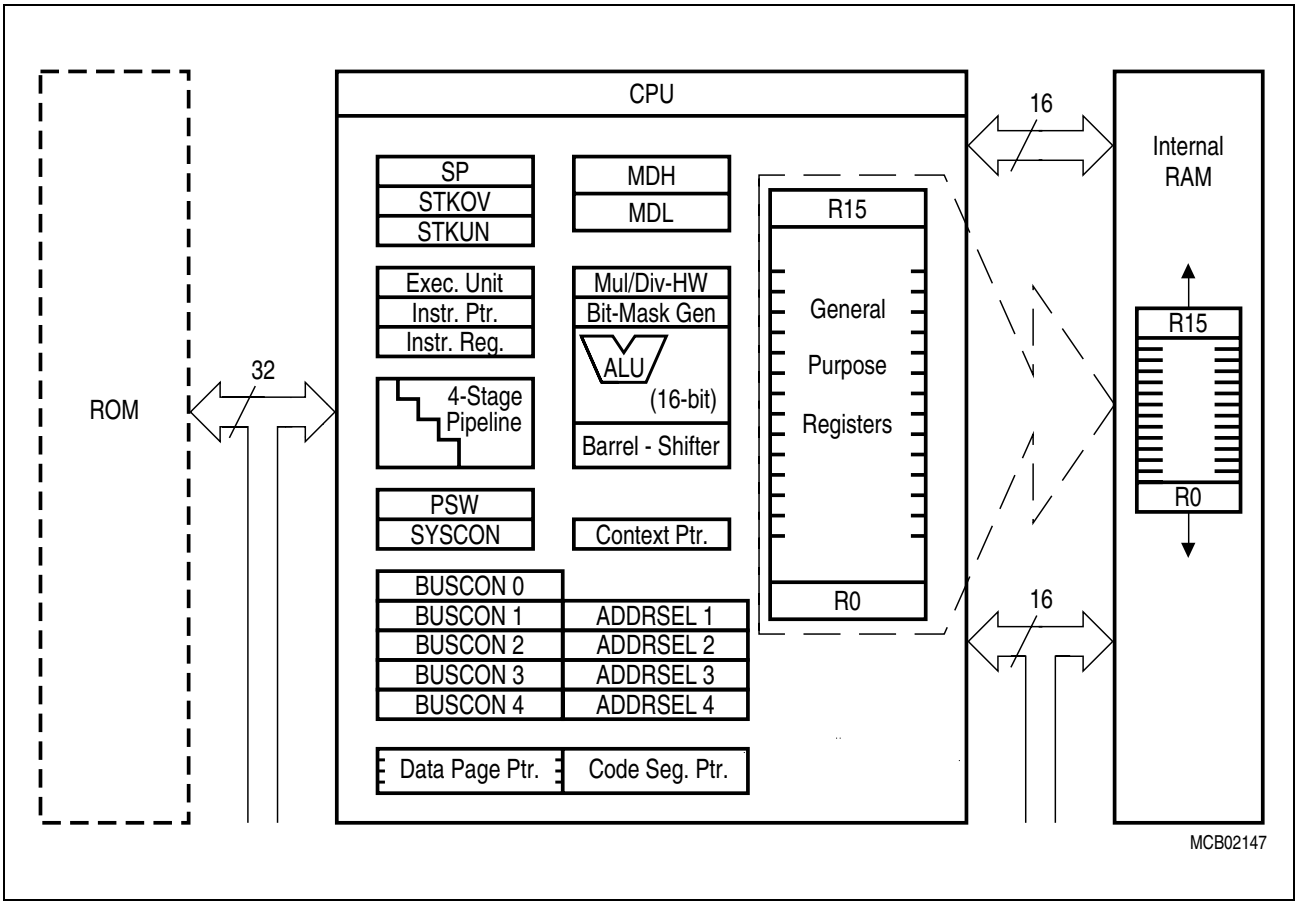

Figure 4 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C167CS instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C167CS is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CS supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CS has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C167CS interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

The C167CS also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	 RESET RESET RESET	 $00'0000_H$ $00'0000_H$ $00'0000_H$	 00_H 00_H 00_H	 III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 $00'0008_H$ $00'0010_H$ $00'0018_H$	 02_H 04_H 06_H	 II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	 UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP	 $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$	 $0A_H$ $0A_H$ $0A_H$ $0A_H$ $0A_H$	 I I I I I
Reserved	–	–	$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	–
Software Traps – TRAP Instruction	–	–	Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

Real Time Clock

The Real Time Clock (RTC) module of the C167CS consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver ($f_{RTC} = f_{OSC}/32$) and is therefore independent from the selected clock generation mode of the C167CS. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

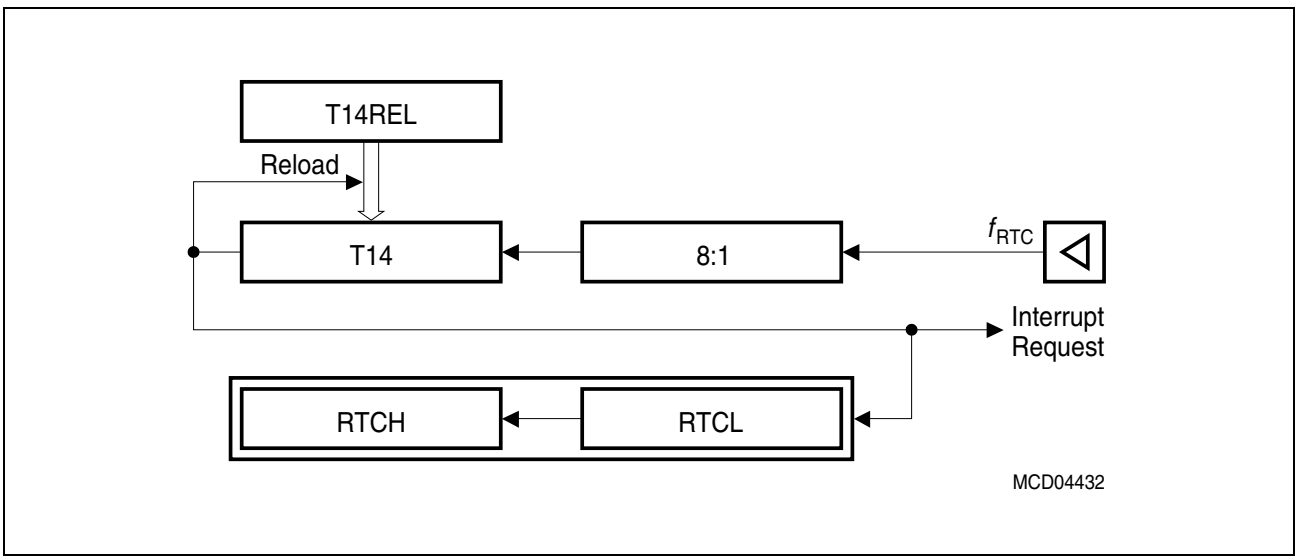

Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 Kbit/s/ 1.03 Mbit/s/1.25 Mbit/s and half-duplex synchronous communication at up to 3.1/ 4.1 Mbit/s/5.0 Mbit/s (@ 25/33/40 MHz CPU clock).
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25/8.25/10 Mbit/s (@ 25/33/40 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 3 separate interrupt vectors are provided.
The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
C1UAR	$EFn2_H$ **X**	---	CAN1 Upper Arbitration Reg. (msg. **n**)	$UUUU_H$
C1UGML	$EF08_H$ **X**	---	CAN1 Upper Global Mask Long	$UUUU_H$
C1UMLM	$EF0C_H$ **X**	---	CAN1 Upper Mask of Last Message	$UUUU_H$
C2BTR	$EE04_H$ **X**	---	CAN2 Bit Timing Register	$UUUU_H$
C2CSR	$EE00_H$ **X**	---	CAN2 Control/Status Register	$XX01_H$
C2GMS	$EE06_H$ **X**	---	CAN2 Global Mask Short	$UFUU_H$
C2PCIR	$EE02_H$ **X**	---	CAN2 Port Control/Interrupt Register	$XXXX_H$
C2LGML	$EE0A_H$ **X**	---	CAN2 Lower Global Mask Long	$UUUU_H$
C2LMLM	$EE0E_H$ **X**	---	CAN2 Lower Mask of Last Message	$UUUU_H$
C2UAR	$EEn2_H$ **X**	---	CAN2 Upper Arbitration Reg. (msg. **n**)	$UUUU_H$
C2UGML	$EE08_H$ **X**	---	CAN2 Upper Global Mask Long	$UUUU_H$
C2UMLM	$EE0C_H$ **X**	---	CAN2 Upper Mask of Last Message	$UUUU_H$
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC0	$FE80_H$	40_H	CAPCOM Register 0	0000_H
CC0IC **b**	$FF78_H$	BC_H	CAPCOM Reg. 0 Interrupt Ctrl. Reg.	0000_H
CC1	$FE82_H$	41_H	CAPCOM Register 1	0000_H
CC10	$FE94_H$	$4A_H$	CAPCOM Register 10	0000_H
CC10IC **b**	$FF8C_H$	$C6_H$	CAPCOM Reg. 10 Interrupt Ctrl. Reg.	0000_H
CC11	$FE96_H$	$4B_H$	CAPCOM Register 11	0000_H
CC11IC **b**	$FF8E_H$	$C7_H$	CAPCOM Reg. 11 Interrupt Ctrl. Reg.	0000_H
CC12	$FE98_H$	$4C_H$	CAPCOM Register 12	0000_H
CC12IC **b**	$FF90_H$	$C8_H$	CAPCOM Reg. 12 Interrupt Ctrl. Reg.	0000_H
CC13	$FE9A_H$	$4D_H$	CAPCOM Register 13	0000_H
CC13IC **b**	$FF92_H$	$C9_H$	CAPCOM Reg. 13 Interrupt Ctrl. Reg.	0000_H
CC14	$FE9C_H$	$4E_H$	CAPCOM Register 14	0000_H
CC14IC **b**	$FF94_H$	CA_H	CAPCOM Reg. 14 Interrupt Ctrl. Reg.	0000_H
CC15	$FE9E_H$	$4F_H$	CAPCOM Register 15	0000_H
CC15IC **b**	$FF96_H$	CB_H	CAPCOM Reg. 15 Interrupt Ctrl. Reg.	0000_H
CC16	$FE60_H$	30_H	CAPCOM Register 16	0000_H
CC16IC **b**	$F160_H$ **E**	$B0_H$	CAPCOM Reg. 16 Interrupt Ctrl. Reg.	0000_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
DP1L b	$F104_H$ E	82_H	P1L Direction Control Register	00_H
DP1H b	$F106_H$ E	83_H	P1H Direction Control Register	00_H
DP2 b	$FFC2_H$	$E1_H$	Port 2 Direction Control Register	0000_H
DP3 b	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 b	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP6 b	$FFCE_H$	$E7_H$	Port 6 Direction Control Register	00_H
DP7 b	$FFD2_H$	$E9_H$	Port 7 Direction Control Register	00_H
DP8 b	$FFD6_H$	EB_H	Port 8 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON b	$F1C0_H$ E	$E0_H$	External Interrupt Control Register	0000_H
EXISEL b	$F1DA_H$ E	ED_H	External Interrupt Source Select Reg.	0000_H
FOCON b	$FFAA_H$	$D5_H$	Frequency Output Control Register	0000_H
IDCHIP	$F07C_H$ E	$3E_H$	Identifier	$0CXX_H$
IDMANUF	$F07E_H$ E	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ E	$3D_H$	Identifier	$X040_H$
IDMEM2	$F076_H$ E	$3B_H$	Identifier	$XXXX_H$
IDPROG	$F078_H$ E	$3C_H$	Identifier	$XXXX_H$
ISNC b	$F1DE_H$ E	EF_H	Interrupt Subnode Control Register	0000_H
MDC b	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 b	$F1C2_H$ E	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 b	$F1C6_H$ E	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4 b	$F1CA_H$ E	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP6 b	$F1CE_H$ E	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7 b	$F1D2_H$ E	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8 b	$F1D6_H$ E	EB_H	Port 8 Open Drain Control Register	00_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
ONES	**b**	$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P1DIDIS		$FEA4_H$		52_H	Port 1 Digital Input Disable Register	0000_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
P7	**b**	$FFD0_H$		$E8_H$	Port 7 Register (8 bits)	00_H
P8	**b**	$FFD4_H$		EA_H	Port 8 Register (8 bits)	00_H
PECC0		$FEC0_H$		60_H	PEC Channel 0 Control Register	0000_H
PECC1		$FEC2_H$		61_H	PEC Channel 1 Control Register	0000_H
PECC2		$FEC4_H$		62_H	PEC Channel 2 Control Register	0000_H
PECC3		$FEC6_H$		63_H	PEC Channel 3 Control Register	0000_H
PECC4		$FEC8_H$		64_H	PEC Channel 4 Control Register	0000_H
PECC5		$FECA_H$		65_H	PEC Channel 5 Control Register	0000_H
PECC6		$FECC_H$		66_H	PEC Channel 6 Control Register	0000_H
PECC7		$FECE_H$		67_H	PEC Channel 7 Control Register	0000_H
PICON	**b**	$F1C4_H$	**E**	$E2_H$	Port Input Threshold Control Register	0000_H
POCON0H		$F082_H$	**E**	41_H	Port P0H Output Control Register	0000_H
POCON0L		$F080_H$	**E**	40_H	Port P0L Output Control Register	0000_H
POCON1H		$F086_H$	**E**	43_H	Port P1H Output Control Register	0000_H
POCON1L		$F084_H$	**E**	42_H	Port P1L Output Control Register	0000_H
POCON2		$F088_H$	**E**	44_H	Port P2 Output Control Register	0000_H
POCON20		$F0AA_H$	**E**	55_H	Dedicated Pin Output Control Register	0000_H
POCON3		$F08A_H$	**E**	45_H	Port P3 Output Control Register	0000_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address		8-Bit Addr.	Description	Reset Value
POCON4	$F08C_H$	**E**	46_H	Port P4 Output Control Register	0000_H
POCON6	$F08E_H$	**E**	47_H	Port P6 Output Control Register	0000_H
POCON7	$F090_H$	**E**	48_H	Port P7 Output Control Register	0000_H
POCON8	$F092_H$	**E**	49_H	Port P8 Output Control Register	0000_H
PP0	$F038_H$	**E**	$1C_H$	PWM Module Period Register 0	0000_H
PP1	$F03A_H$	**E**	$1D_H$	PWM Module Period Register 1	0000_H
PP2	$F03C_H$	**E**	$1E_H$	PWM Module Period Register 2	0000_H
PP3	$F03E_H$	**E**	$1F_H$	PWM Module Period Register 3	0000_H
PSW b	$FF10_H$		88_H	CPU Program Status Word	0000_H
PT0	$F030_H$	**E**	18_H	PWM Module Up/Down Counter 0	0000_H
PT1	$F032_H$	**E**	19_H	PWM Module Up/Down Counter 1	0000_H
PT2	$F034_H$	**E**	$1A_H$	PWM Module Up/Down Counter 2	0000_H
PT3	$F036_H$	**E**	$1B_H$	PWM Module Up/Down Counter 3	0000_H
PTCR	$F0AE_H$	**E**	57_H	Port Temperature Compensation Reg.	0000_H
PW0	$FE30_H$		18_H	PWM Module Pulse Width Register 0	0000_H
PW1	$FE32_H$		19_H	PWM Module Pulse Width Register 1	0000_H
PW2	$FE34_H$		$1A_H$	PWM Module Pulse Width Register 2	0000_H
PW3	$FE36_H$		$1B_H$	PWM Module Pulse Width Register 3	0000_H
PWMCON0 b	$FF30_H$		98_H	PWM Module Control Register 0	0000_H
PWMCON1 b	$FF32_H$		99_H	PWM Module Control Register 1	0000_H
PWMIC b	$F17E_H$	**E**	BF_H	PWM Module Interrupt Control Register	0000_H
RP0H b	$F108_H$	**E**	84_H	System Start-up Config. Reg. (Rd. only)	XX_H
RSTCON b	$F1E0_H$	**m**	---	Reset Control Register	$00XX_H$
RTCH	$F0D6_H$	**E**	$6B_H$	RTC High Register	$XXXX_H$
RTCL	$F0D4_H$	**E**	$6A_H$	RTC Low Register	$XXXX_H$
S0BG	$FEB4_H$		$5A_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000_H
S0CON b	$FFB0_H$		$D8_H$	Serial Channel 0 Control Register	0000_H
S0EIC b	$FF70_H$		$B8_H$	Serial Channel 0 Error Interrupt Ctrl. Reg	0000_H

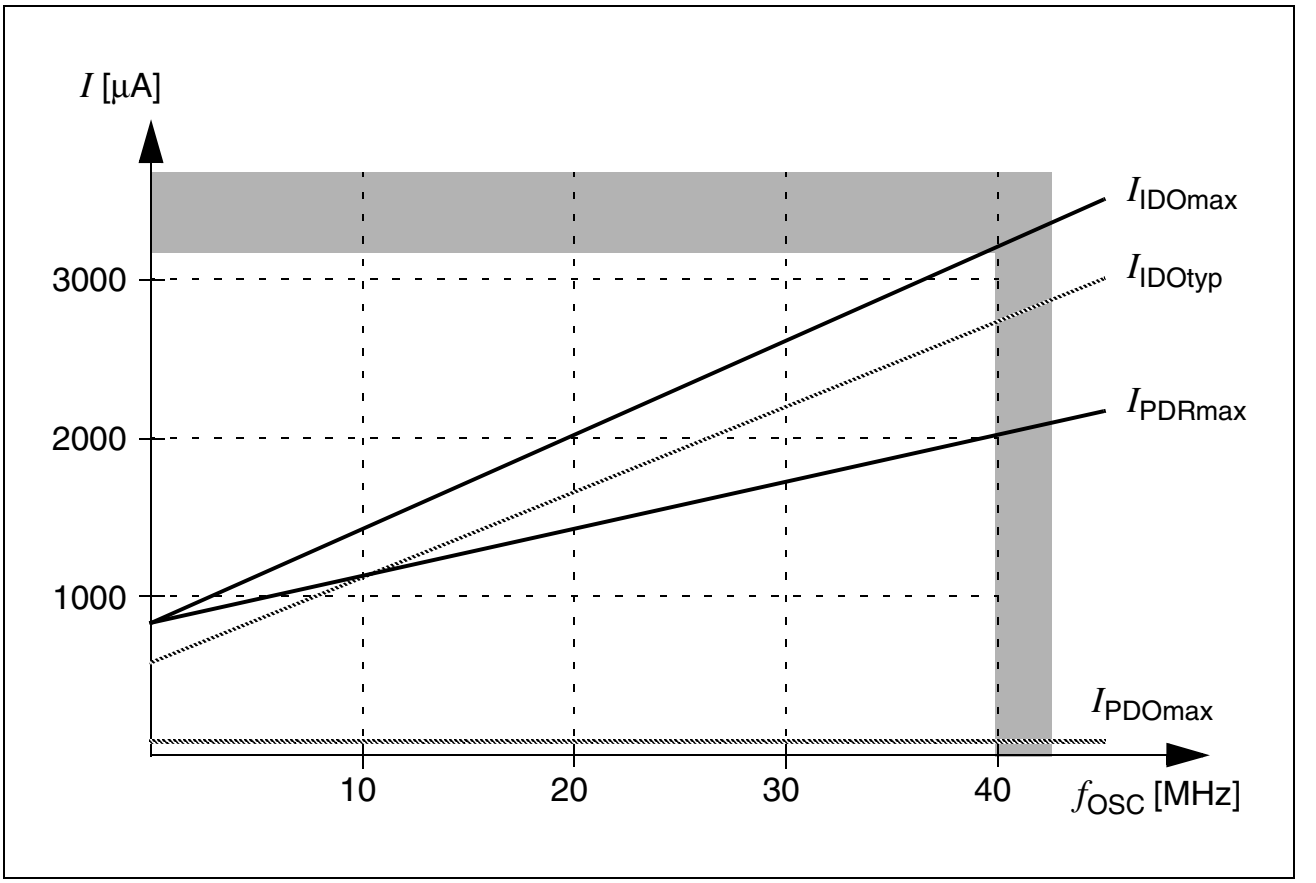

Figure 9 **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

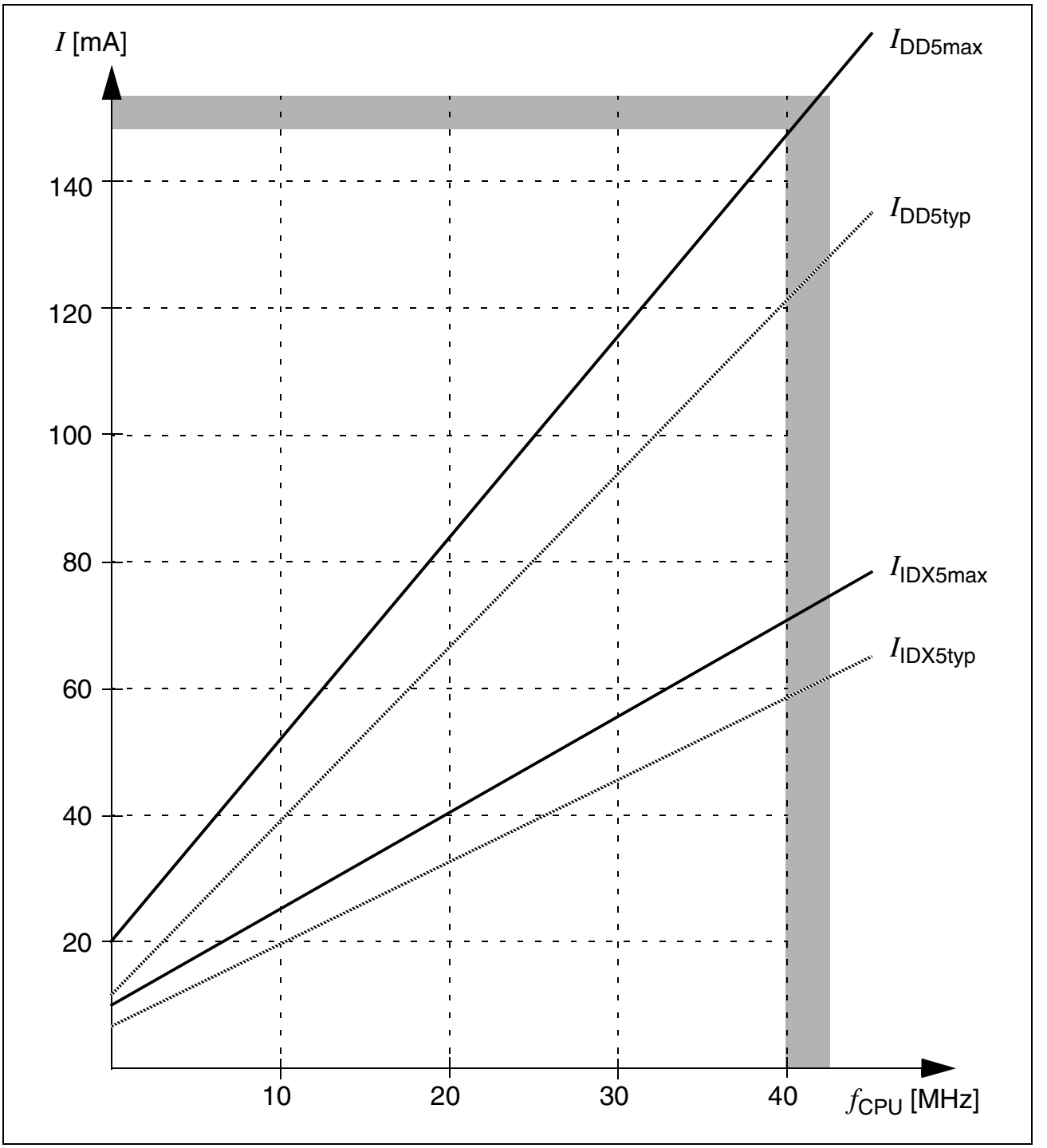

Figure 10 Supply/Idle Current as a Function of Operating Frequency

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 12**).
For a period of $N \times$ TCL the minimum value is computed using the corresponding deviation D_N:

$$(N \times \text{TCL})_{min} = N \times \text{TCL}_{NOM} - D_N;\ D_N\ [\text{ns}] = \pm(13.3 + N \times 6.3) / f_{CPU}\ [\text{MHz}],$$

where N = number of consecutive TCLs and $1 \le N \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 25 = 1.288$ ns, and $(3\text{TCL})_{min} = 3\text{TCL}_{NOM} - 1.288$ ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

*Note: For all periods longer than 40 TCL the N = 40 value can be used (see **Figure 12**).*

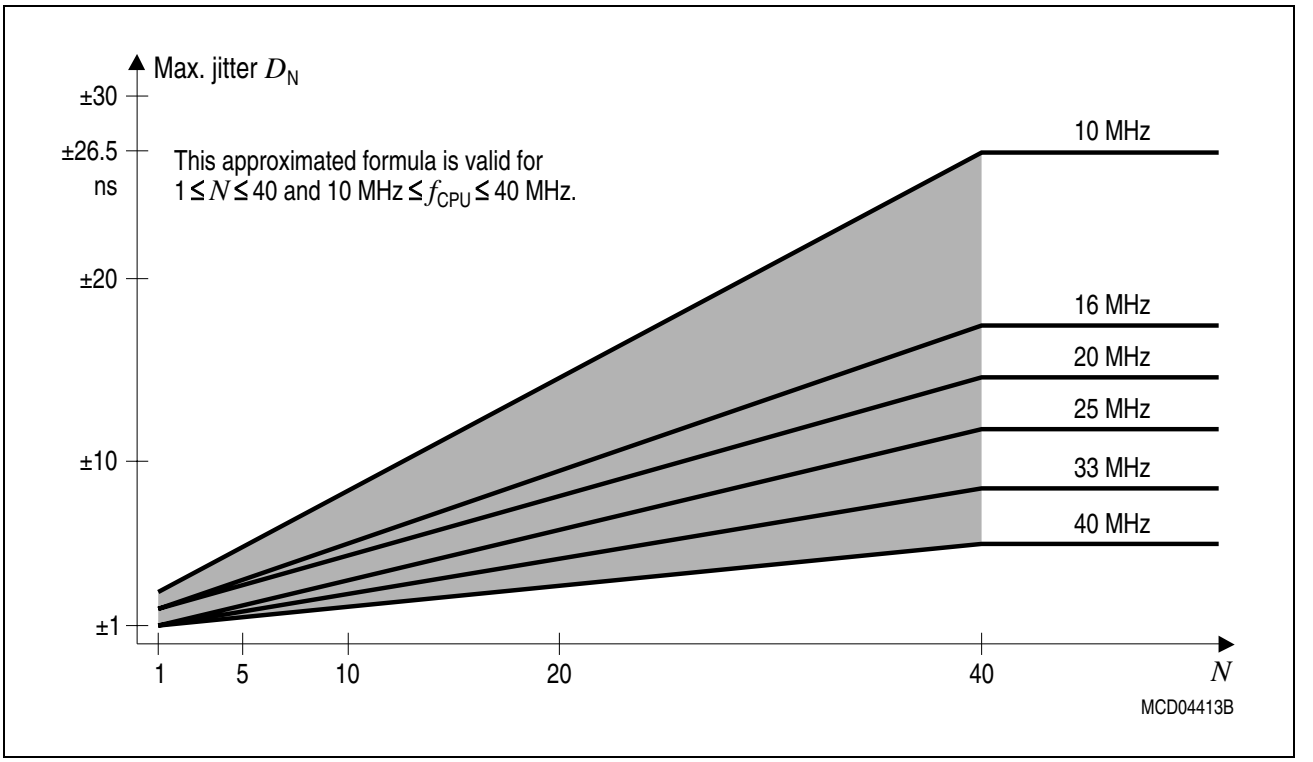

Figure 12 Approximated Maximum Accumulated PLL Jitter

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

AC Characteristics
External Clock Drive XTAL1
(Operating Conditions apply)

Table 12 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	25	–	20	–	37[1]	500[1]	ns
High time[2]	t_1	SR	12[3]	–	5	–	10	–	ns
Low time[2]	t_2	SR	12[3]	–	5	–	10	–	ns
Rise time[2]	t_3	SR	–	8	–	5	–	10	ns
Fall time[2]	t_4	SR	–	8	–	5	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

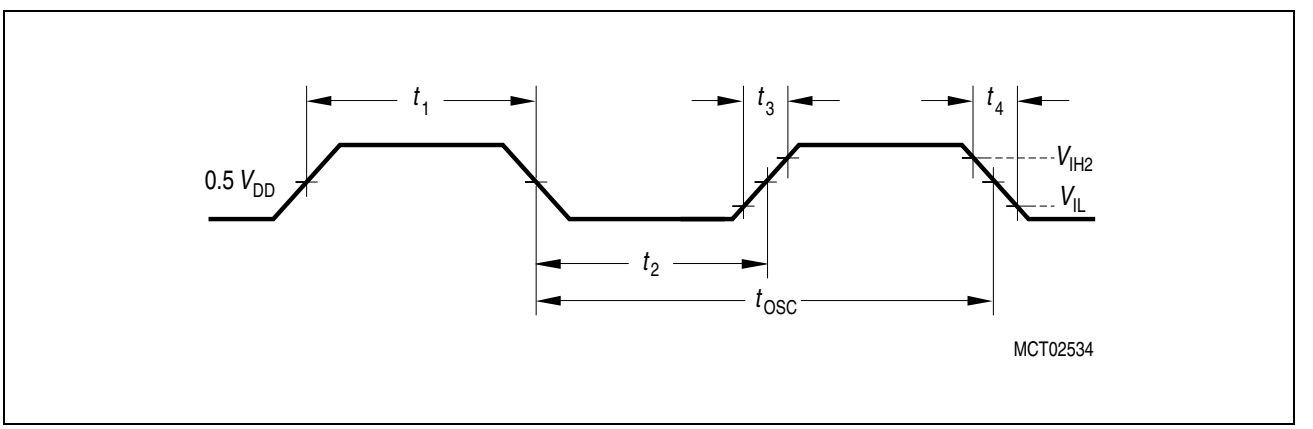

Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

A/D Converter Characteristics

(Operating Conditions apply)

Table 13 A/D Converter Characteristics

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC1)	–	±2	LSB	Channels 0 … 15
			–	±10	LSB	Channels 16 … 23
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC}/60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S/450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DD}$ = +0.2 V) the maximum TUE is increased to ±3/11 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins and P1H pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB (±12 LSB for channels 16 … 23).

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

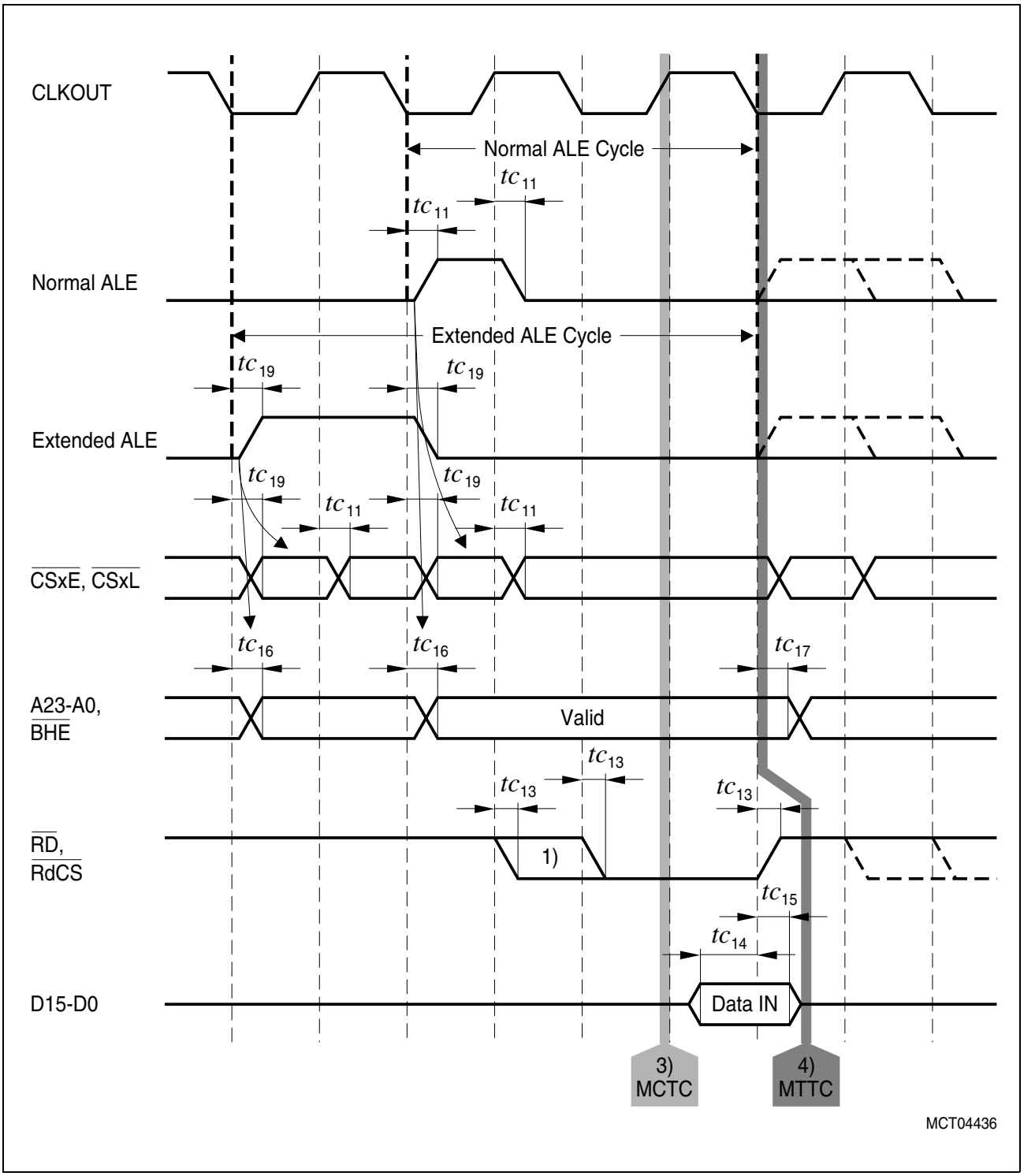

Figure 18 Demultiplexed Bus, Read Access

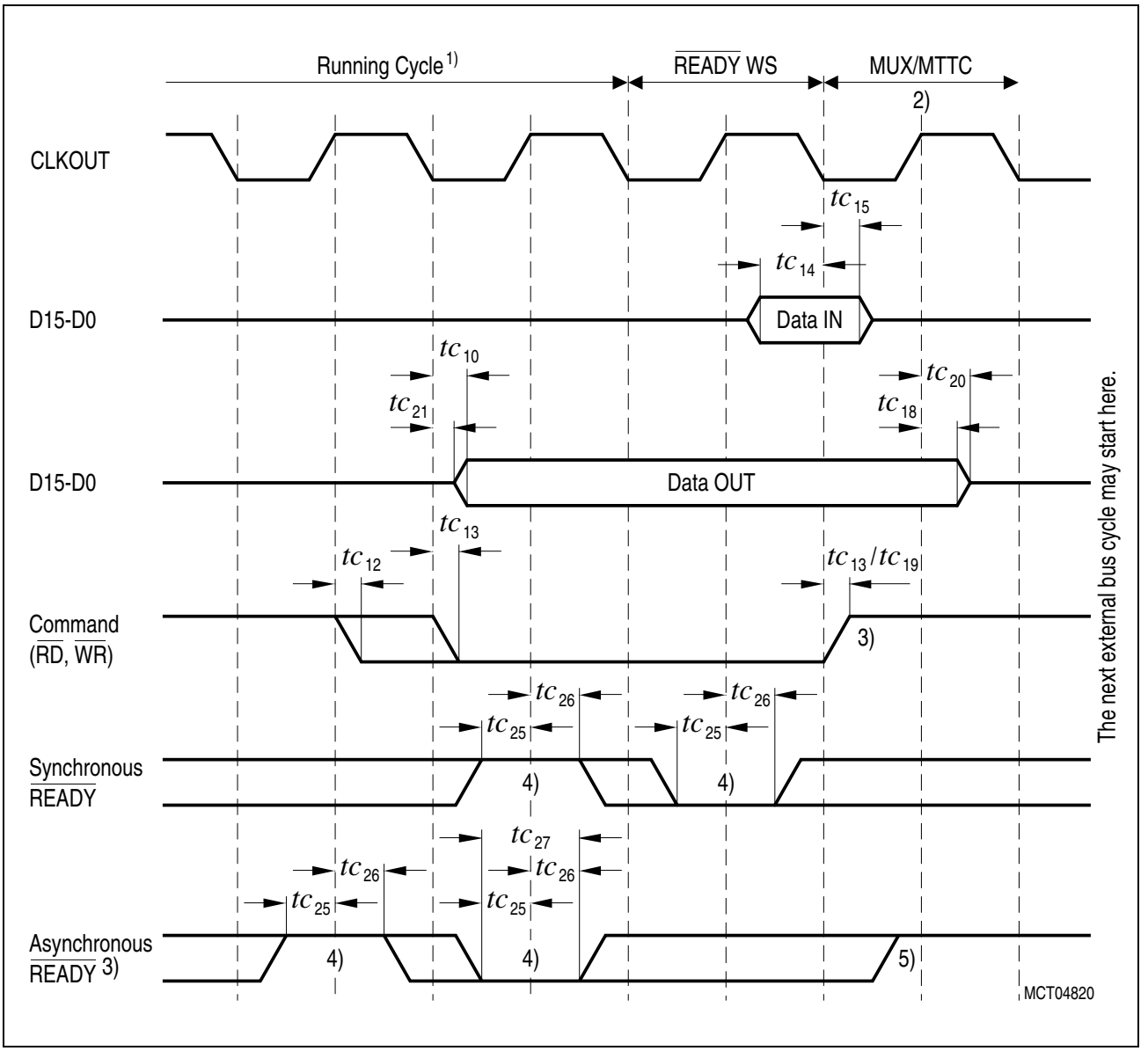

Figure 21 READY Timing