Infineon Technologies - C167CSL40MCAKXQLA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167csl40mcakxqla1

Table 2 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	7	I/O	$\overline{HLDA}$ Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	$\overline{BREQ}$ Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). Port 8 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P8.0	9	I/O I I	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., CAN1_RxD CAN 1 Receive Data Input, CAN2_RxD CAN 2 Receive Data Input
P8.1	10	I/O O O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., CAN1_TxD CAN 1 Transmit Data Output, CAN2_TxD CAN 2 Transmit Data Output
P8.2	11	I/O I I	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., CAN1_RxD CAN 1 Receive Data Input, CAN2_RxD CAN 2 Receive Data Input
P8.3	12	I/O I I	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., CAN1_TxD CAN 1 Transmit Data Output, CAN2_TxD CAN 2 Transmit Data Output
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	140	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CS. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C167CS to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
V_{AREF}	37	–	Reference voltage for the A/D converter.
V_{AGND}	38	–	Reference ground for the A/D converter.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

1) The CAN interface lines are assigned to ports P4 and P8 under software control. Within the CAN module several assignments can be selected.

Note: The following behaviour differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C167CS combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

Figure 3 gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CS.

Note: All time specifications refer to a CPU clock of 40 MHz (see definition in the AC Characteristics section).

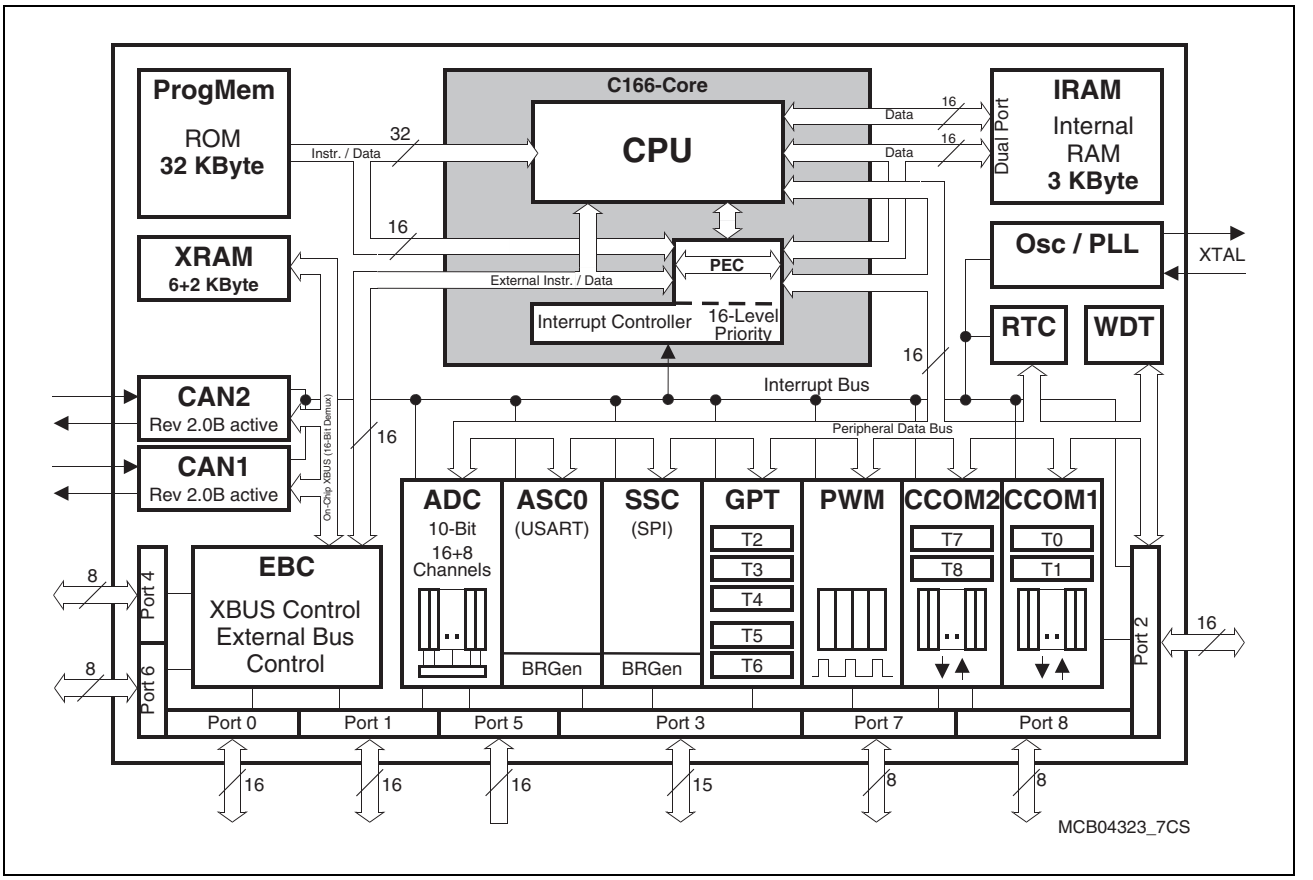


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN) of the C167CS can be individually enabled or disabled during initialization. Register XPERCON selects the required modules which are then enabled by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.

Note: The default value of register XPERCON after reset selects 2 KByte XRAM and module CAN1, so the default XBUS resources are compatible with the C167CR.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C167CS offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C167CS is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CS supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CS has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C167CS interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 3 C167CS Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H

Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘capture’d) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 5 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible.
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible.
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated.
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated.
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

Real Time Clock

The Real Time Clock (RTC) module of the C167CS consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver ($f_{RTC} = f_{OSC}/32$) and is therefore independent from the selected clock generation mode of the C167CS. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

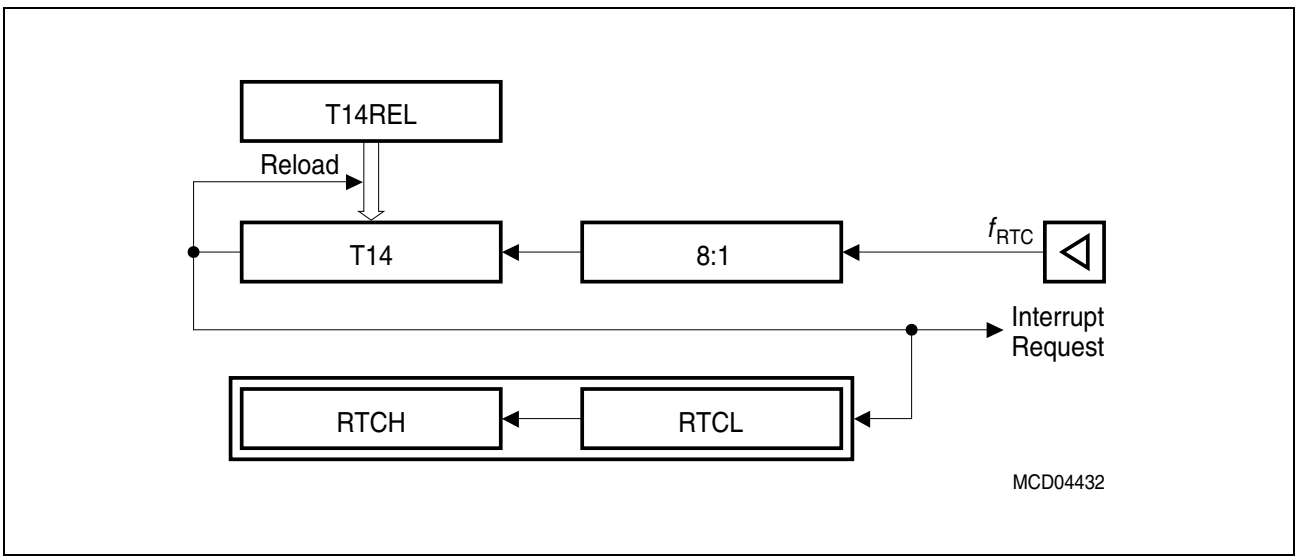


Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

Parallel Ports

The C167CS provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output CLKOUT (or the programmable frequency output FOUT).
Port 5 (and parts of PORT1) is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) and driver characteristics (output current) of the C167CS's port drivers can be selected via the Port Output Control registers (POCONx).

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
XP3IC	**b**	$F19E_H$	**E**	CF_H	RTC/PLL Interrupt Control Register	0000_H
XPERCON		$F024_H$	**E**	12_H	X-Peripheral Control Register	0401_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CS and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C167CS will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the C167CS.

DC Characteristics

(Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	0.2 V_{DD} - 0.1	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	0.3 V_{DD}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	2.0	V	–
Input high voltage (TTL, all except $\overline{\text{RSTIN}}$ and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{\text{RSTIN}}$ (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	–	mV	Series resistance = 0 Ω
Output low voltage[2)]	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[3)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[3)4)]
Output high voltage[5)]	V_{OH}	CC	V_{DD} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[3)]
			V_{DD} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[3)4)]
Input leakage current (Port 5)	I_{OZ1}	CC	–	±200	nA	0 V < V_{IN} < V_{DD}

AC Characteristics
Definition of Internal Timing

The internal operation of the C167CS is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see **Figure 11**).

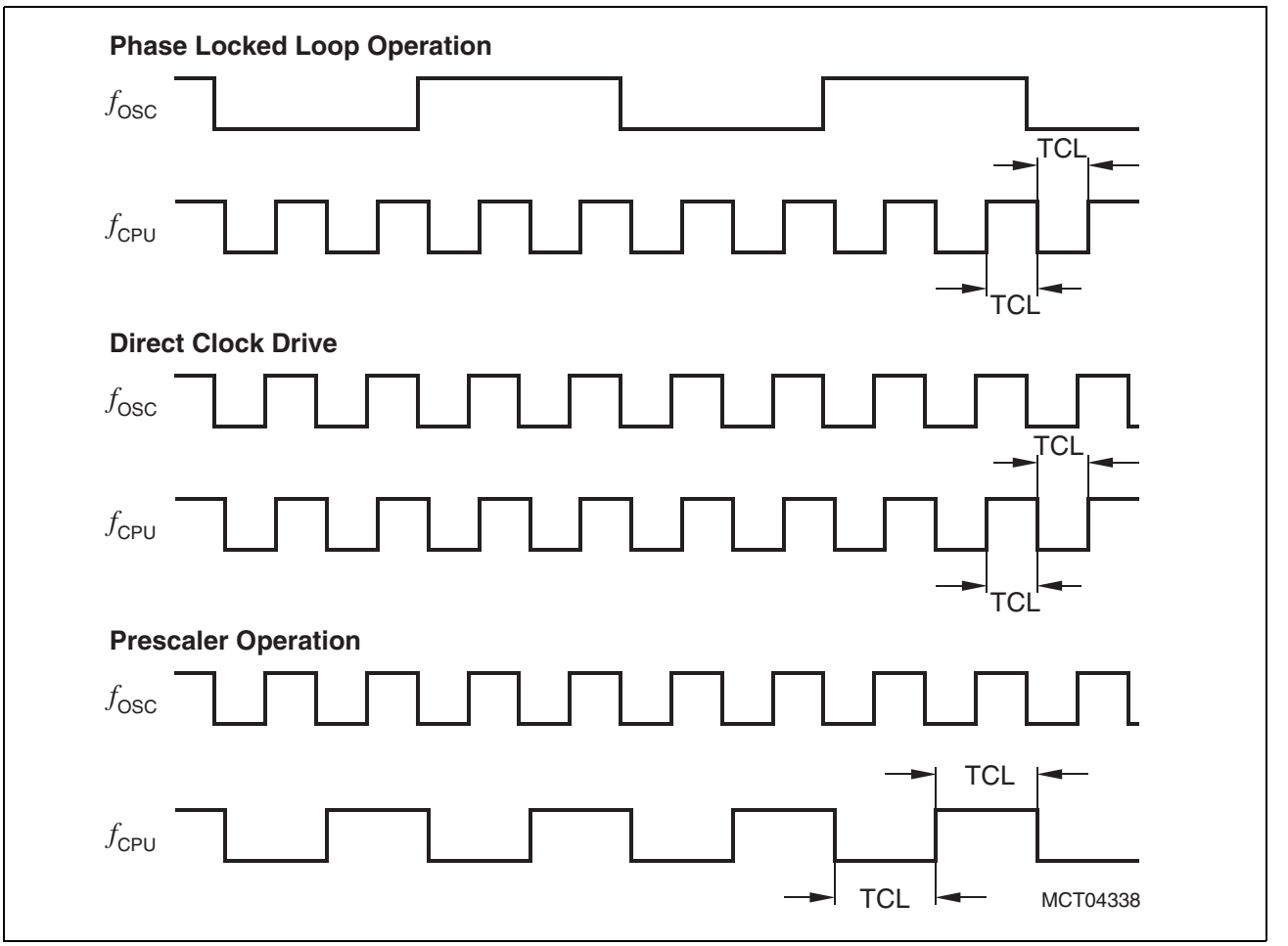


Figure 11 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C167CS.

*Note: The example for PLL operation shown in **Figure 11** refers to a PLL factor of 4.*

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5.
Upon a long hardware reset register RP0H is loaded with the logic levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins

AC Characteristics
External Clock Drive XTAL1
(Operating Conditions apply)

Table 12 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	25	–	20	–	37[1]	500[1]	ns
High time[2]	t_1	SR	12[3]	–	5	–	10	–	ns
Low time[2]	t_2	SR	12[3]	–	5	–	10	–	ns
Rise time[2]	t_3	SR	–	8	–	5	–	10	ns
Fall time[2]	t_4	SR	–	8	–	5	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

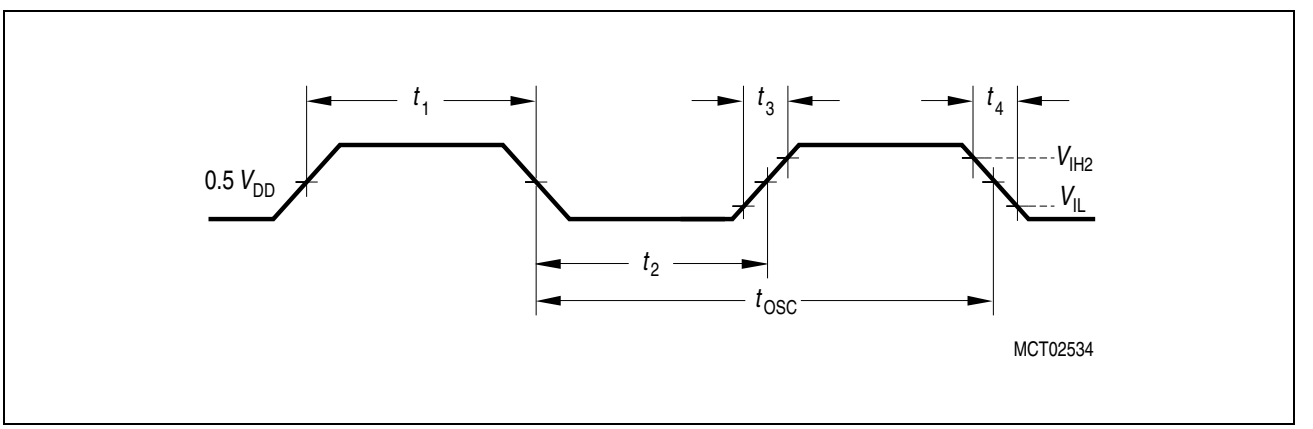


Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

A/D Converter Characteristics

(Operating Conditions apply)

Table 13 A/D Converter Characteristics

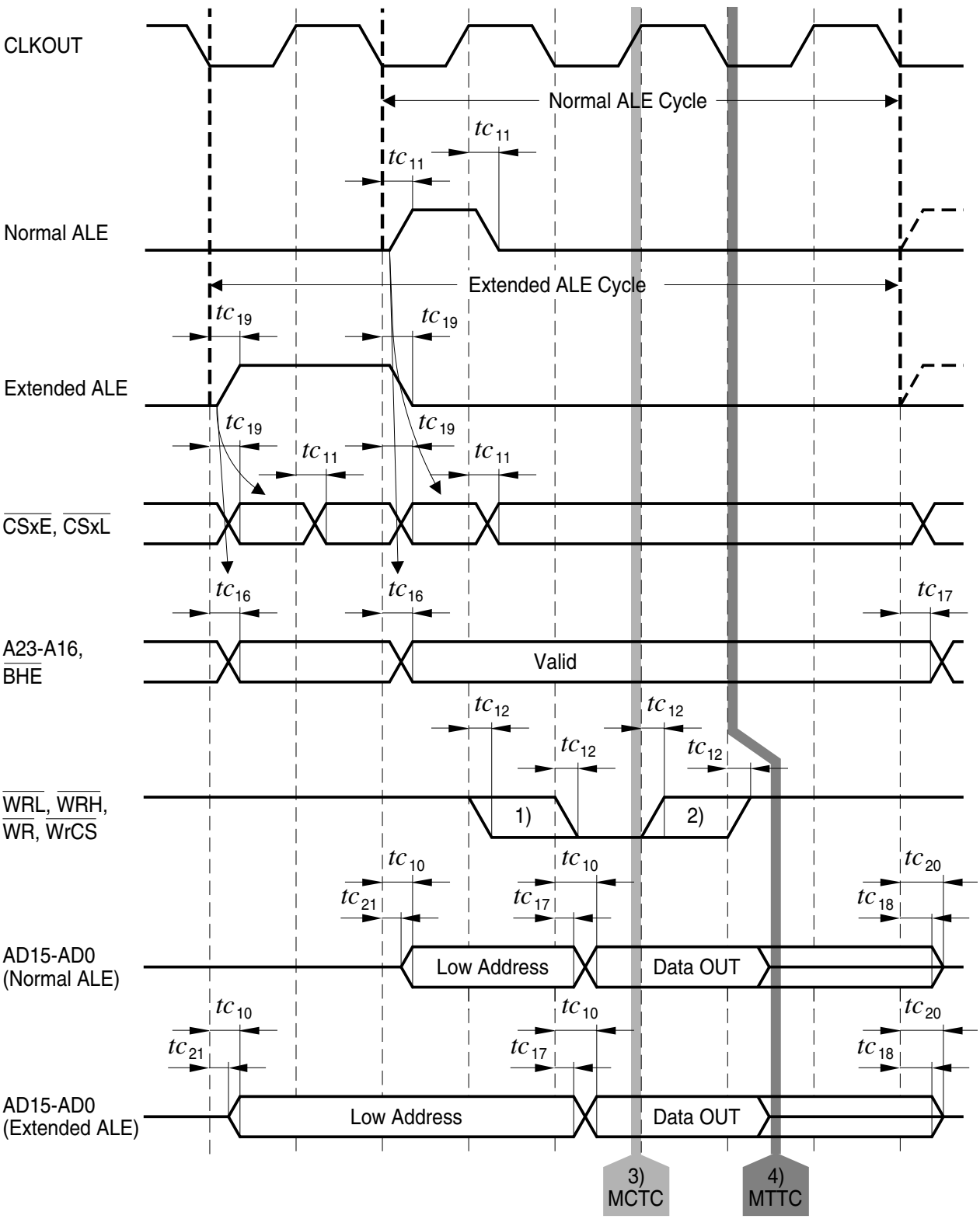
Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2t_{CPU}	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC1)	–	±2	LSB	Channels 0 … 15
			–	±10	LSB	Channels 16 … 23
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC}/60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S/450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DD}$ = +0.2 V) the maximum TUE is increased to ±3/11 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins and P1H pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB (±12 LSB for channels 16 … 23).

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.



Note: Write data is deactivated 2 TCL earlier if early write is enabled (same timing).

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Figure 19 Multiplexed Bus, Write Access

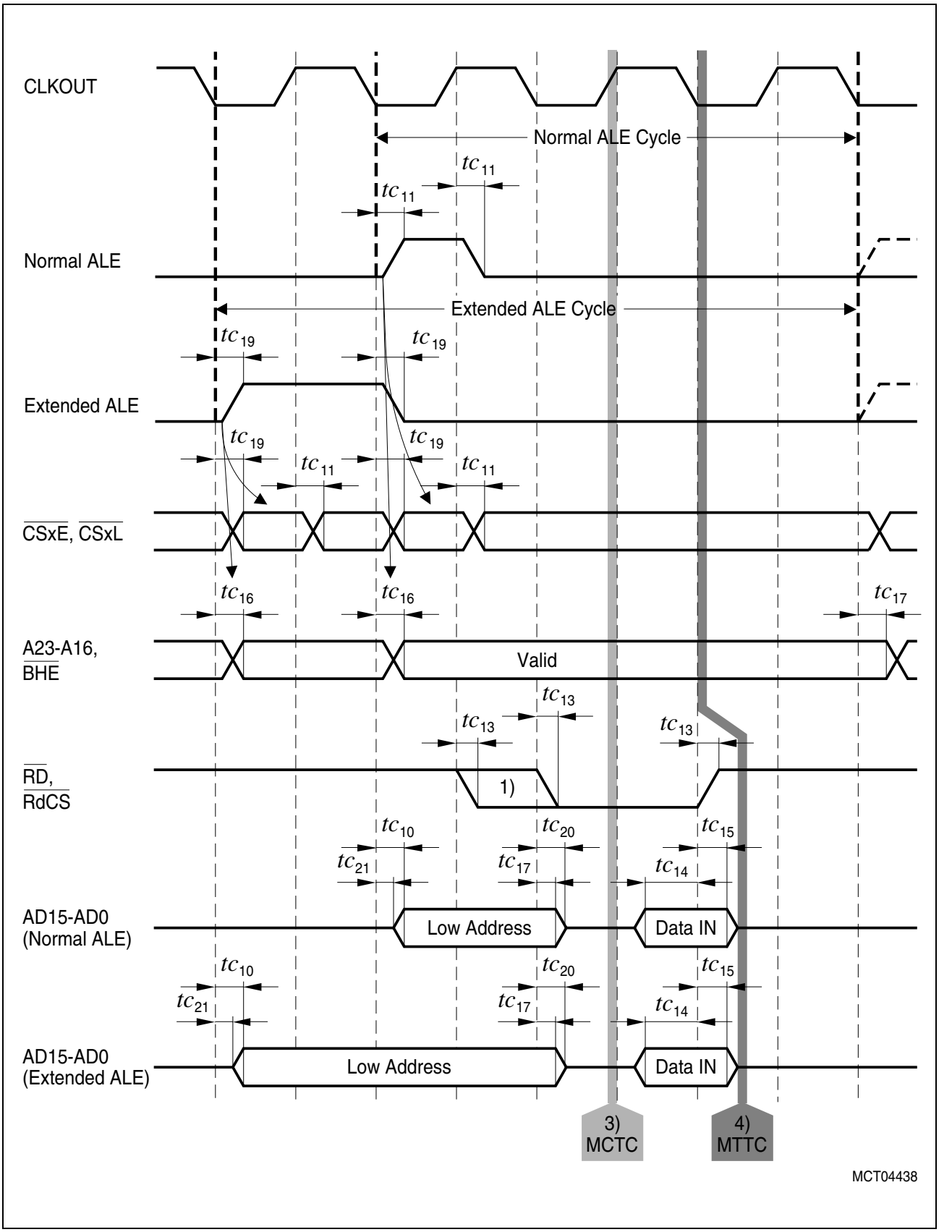
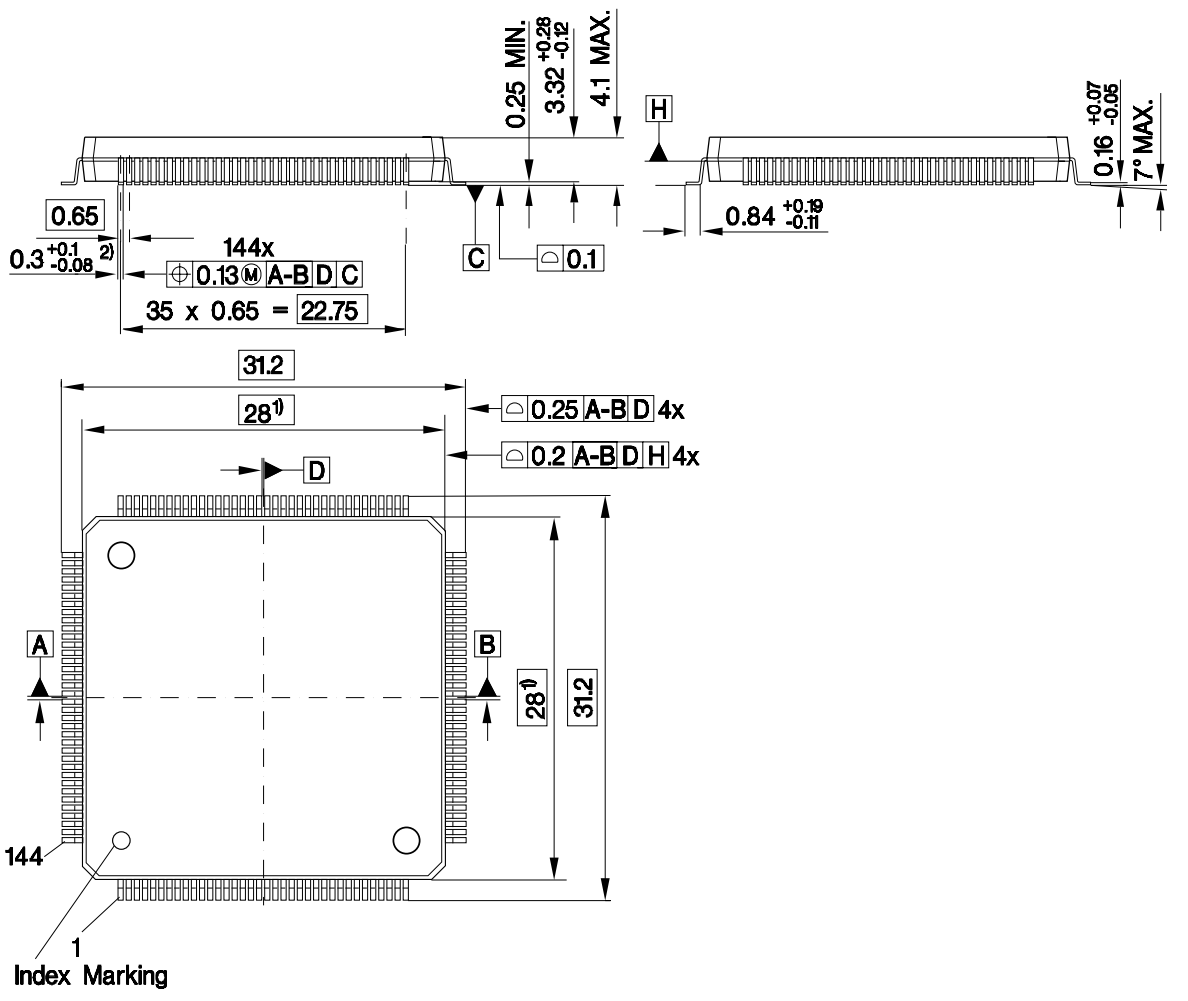


Figure 20 Multiplexed Bus, Read Access

Package Outlines

P-MQFP-144-6
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPM09391

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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