# Infineon Technologies - C167CSL40MCAKXQLA2 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166 |
| Core Size | 16-Bit |
| Speed | 40MHz |
| Connectivity | CANbus, EBI/EMI, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 111 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 11K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-BQFP |
| Supplier Device Package | P-MQFP-144-8 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/c167csl40mcakxqla2 |

**Edition 2001-08**

**Published by Infineon Technologies AG,**
**St.-Martin-Strasse 53,**
**D-81541 München, Germany**



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Data Sheet, V2.2, Aug. 2001

# C167CS-4R
# C167CS-L

## 16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

## Pin Configuration
(top view)

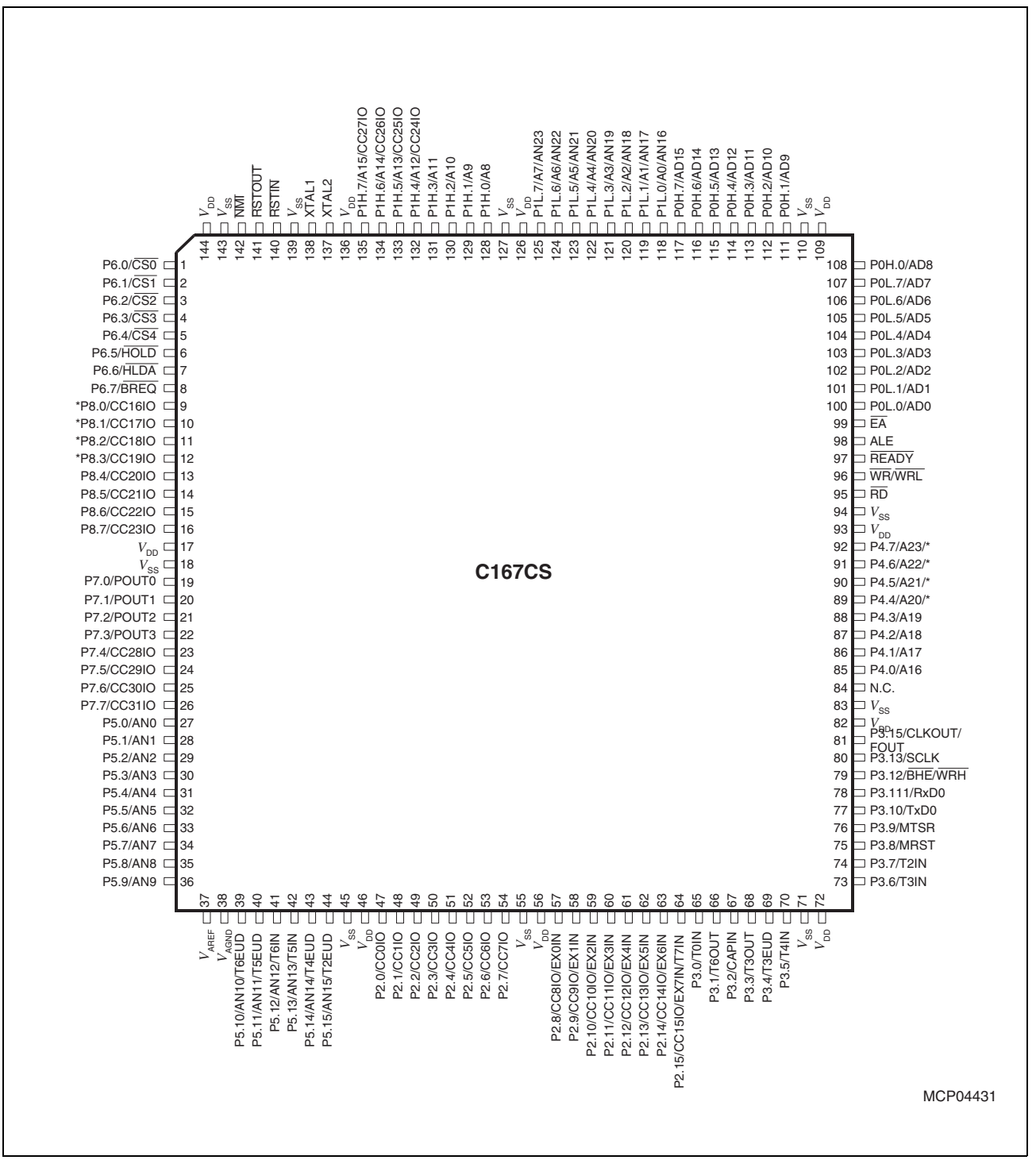


**Figure 2**

***)** The marked pins of Port 4 and Port 8 can have CAN interface lines assigned to them. **Table 2** on the pages below lists the possible assignments.

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **P2** | | IO | Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special).<br>The following Port 2 pins also serve for alternate functions: |
| P2.0 | 47 | I/O | CC0IO CAPCOM1: CC0 Capture Inp./Compare Output |
| P2.1 | 48 | I/O | CC1IO CAPCOM1: CC1 Capture Inp./Compare Output |
| P2.2 | 49 | I/O | CC2IO CAPCOM1: CC2 Capture Inp./Compare Output |
| P2.3 | 50 | I/O | CC3IO CAPCOM1: CC3 Capture Inp./Compare Output |
| P2.4 | 51 | I/O | CC4IO CAPCOM1: CC4 Capture Inp./Compare Output |
| P2.5 | 52 | I/O | CC5IO CAPCOM1: CC5 Capture Inp./Compare Output |
| P2.6 | 53 | I/O | CC6IO CAPCOM1: CC6 Capture Inp./Compare Output |
| P2.7 | 54 | I/O | CC7IO CAPCOM1: CC7 Capture Inp./Compare Output |
| P2.8 | 57 | I/O | CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, |
| | | I | EX0IN Fast External Interrupt 0 Input |
| P2.9 | 58 | I/O | CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, |
| | | I | EX1IN Fast External Interrupt 1 Input |
| P2.10 | 59 | I/O | CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., |
| | | I | EX2IN Fast External Interrupt 2 Input |
| P2.11 | 60 | I/O | CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., |
| | | I | EX3IN Fast External Interrupt 3 Input |
| P2.12 | 61 | I/O | CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., |
| | | I | EX4IN Fast External Interrupt 4 Input |
| P2.13 | 62 | I/O | CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., |
| | | I | EX5IN Fast External Interrupt 5 Input |
| P2.14 | 63 | I/O | CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., |
| | | I | EX6IN Fast External Interrupt 6 Input |
| P2.15 | 64 | I/O | CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., |
| | | I | EX7IN Fast External Interrupt 7 Input, |
| | | I | T7IN CAPCOM2: Timer T7 Count Input |
| | | | *Note: During Sleep Mode a spike filter on the EXnIN interrupt inputs suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter.* |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| $V_{DD}$ | 17, 46, 56, 72, 82, 93, 109, 126, 136, 144 | – | Digital Supply Voltage:<br>+5 V during normal operation and idle mode.<br>≥2.5 V during power down mode. |
| $V_{SS}$ | 18, 45, 55, 71, 83, 94, 110, 127, 139, 143 | – | Digital Ground. |

1) The CAN interface lines are assigned to ports P4 and P8 under software control. Within the CAN module several assignments can be selected.

*Note: The following behaviour differences must be observed when the bidirectional reset is active:*

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

## Functional Description

The architecture of the C167CS combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

**Figure 3** gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CS.

*Note: All time specifications refer to a CPU clock of 40 MHz (see definition in the AC Characteristics section).*

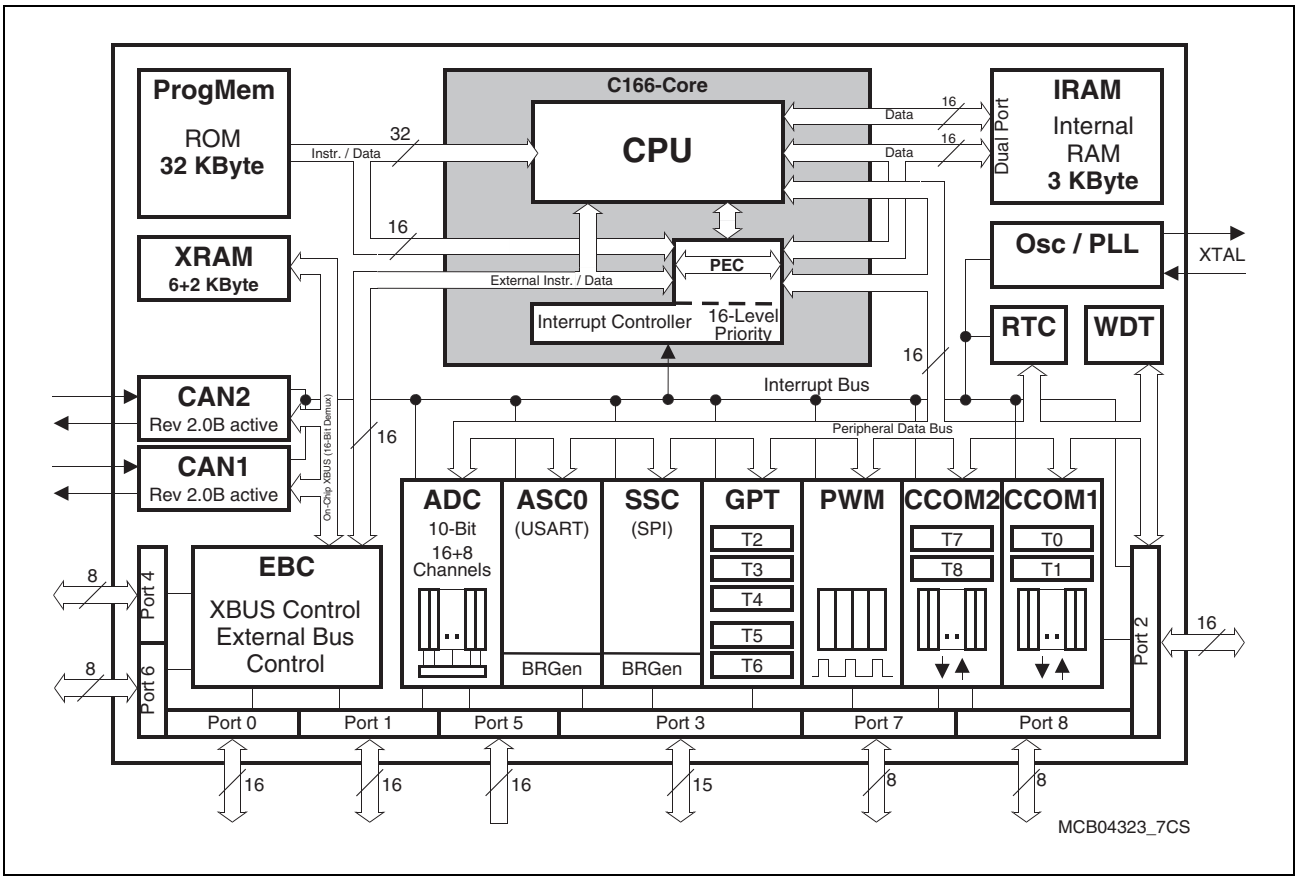


**Figure 3 Block Diagram**

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN) of the C167CS can be individually enabled or disabled during initialization. Register XPERCON selects the required modules which are then enabled by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.

*Note: The default value of register XPERCON after reset selects 2 KByte XRAM and module CAN1, so the default XBUS resources are compatible with the C167CR.*

*Note: When one or both of the on-chip CAN Modules are used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 ... A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.*

### Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CS's instructions can be executed in just one machine cycle which requires 50 ns at 40 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

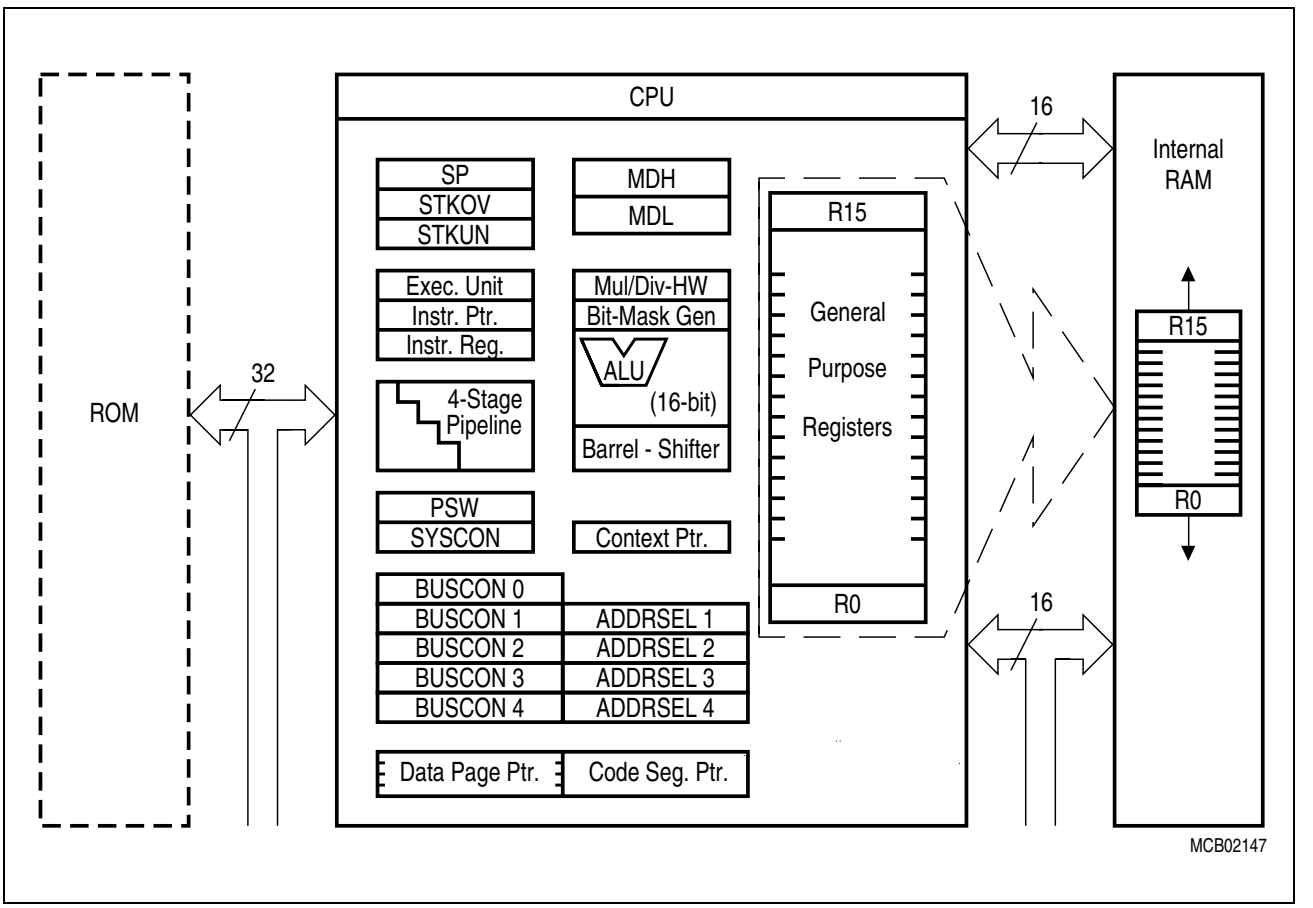


**Figure 4 CPU Block Diagram**

### Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘capture’d) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

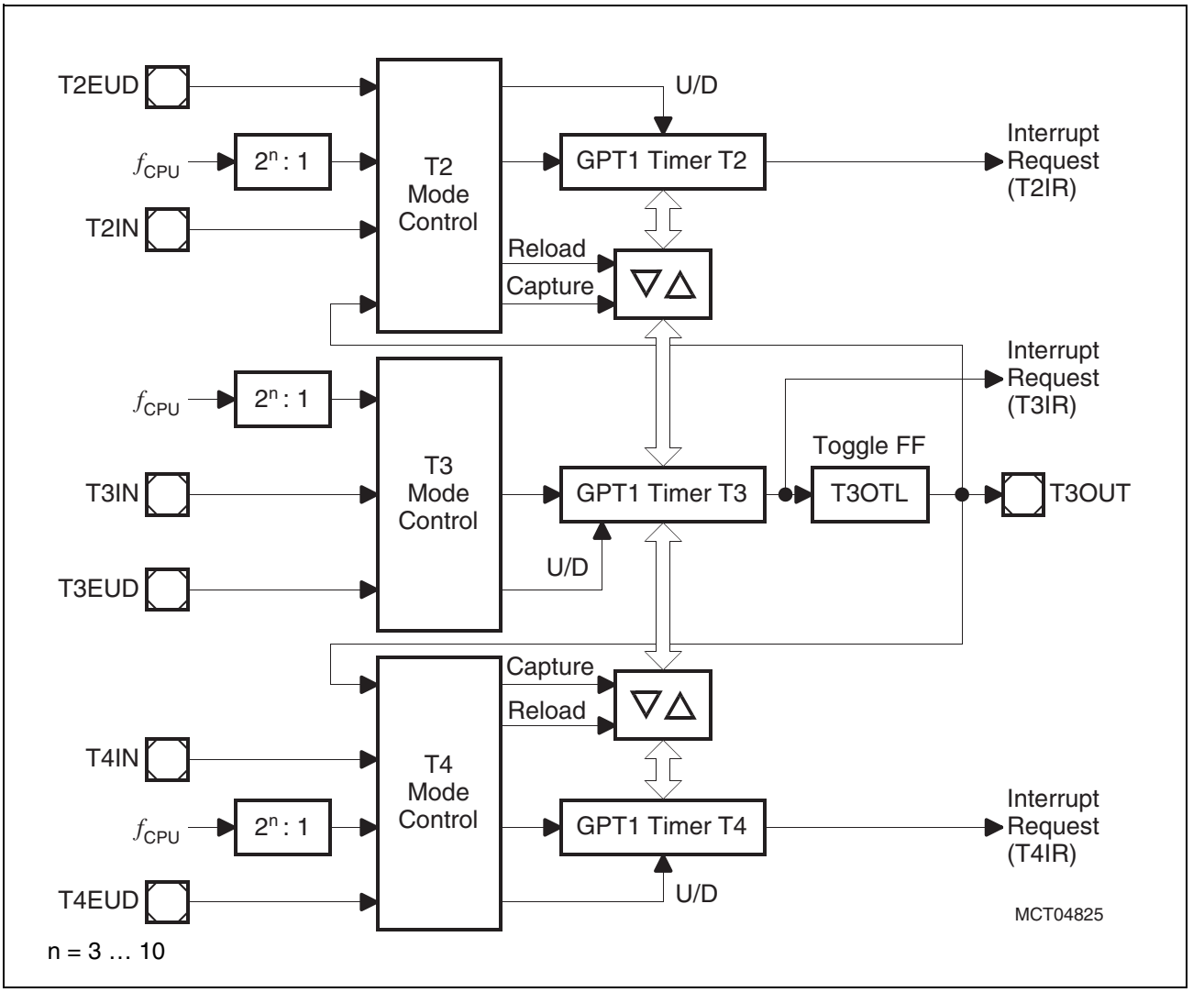


**Figure 6 Block Diagram of GPT1**

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared

### A/D Converter

For analog signal measurement, a 10-bit A/D converter with 24 multiplexed input channels (16 standard channels and 8 extension channels) and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 24 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CS supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels (standard or extension) are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via registers P5DIDIS (Port 5 Digital Input Disable) and P1DIDIS (PORT1 Digital Input Disable).

## Parallel Ports

The C167CS provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output CLKOUT (or the programmable frequency output FOUT).
Port 5 (and parts of PORT1) is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) and driver characteristics (output current) of the C167CS's port drivers can be selected via the Port Output Control registers (POCONx).

### Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly ($f_{CPU}$ = 2 … 5 MHz).
In prescaler mode the PLL base frequency is divided by 2 ($f_{CPU}$ = 1 … 2.5 MHz).

*Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.*

**The oscillator watchdog can be disabled** by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = ‘1’) the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

*Note: At the end of a reset bit OWDDIS reflects the inverted level of pin $\overline{RD}$ at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration via PORT0.*

## Instruction Set Summary

Table 6 lists the instructions of the C167CS in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"C166 Family Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

**Table 6 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16-16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise XOR, (word/byte operands) | 2 / 4 |
| BCLR | Clear direct bit | 2 |
| BSET | Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND, BOR, BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/L | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL / SHR | Shift left/right direct word GPR | 2 |
| ROL / ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |

## Absolute Maximum Ratings

**Table 8 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Storage temperature | $T_{ST}$ | -65 | 150 | °C | – |
| Junction temperature | $T_J$ | -40 | 150 | °C | under bias |
| Voltage on $V_{DD}$ pins with respect to ground ($V_{SS}$) | $V_{DD}$ | -0.5 | 6.5 | V | – |
| Voltage on any pin with respect to ground ($V_{SS}$) | $V_{IN}$ | -0.5 | $V_{DD}$ + 0.5 | V | – |
| Input current on any pin during overload condition | – | -10 | 10 | mA | – |
| Absolute sum of all input currents during overload condition | – | – | \|100\| | mA | – |
| Power dissipation | $P_{DISS}$ | – | 1.5 | W | – |

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DD}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.*

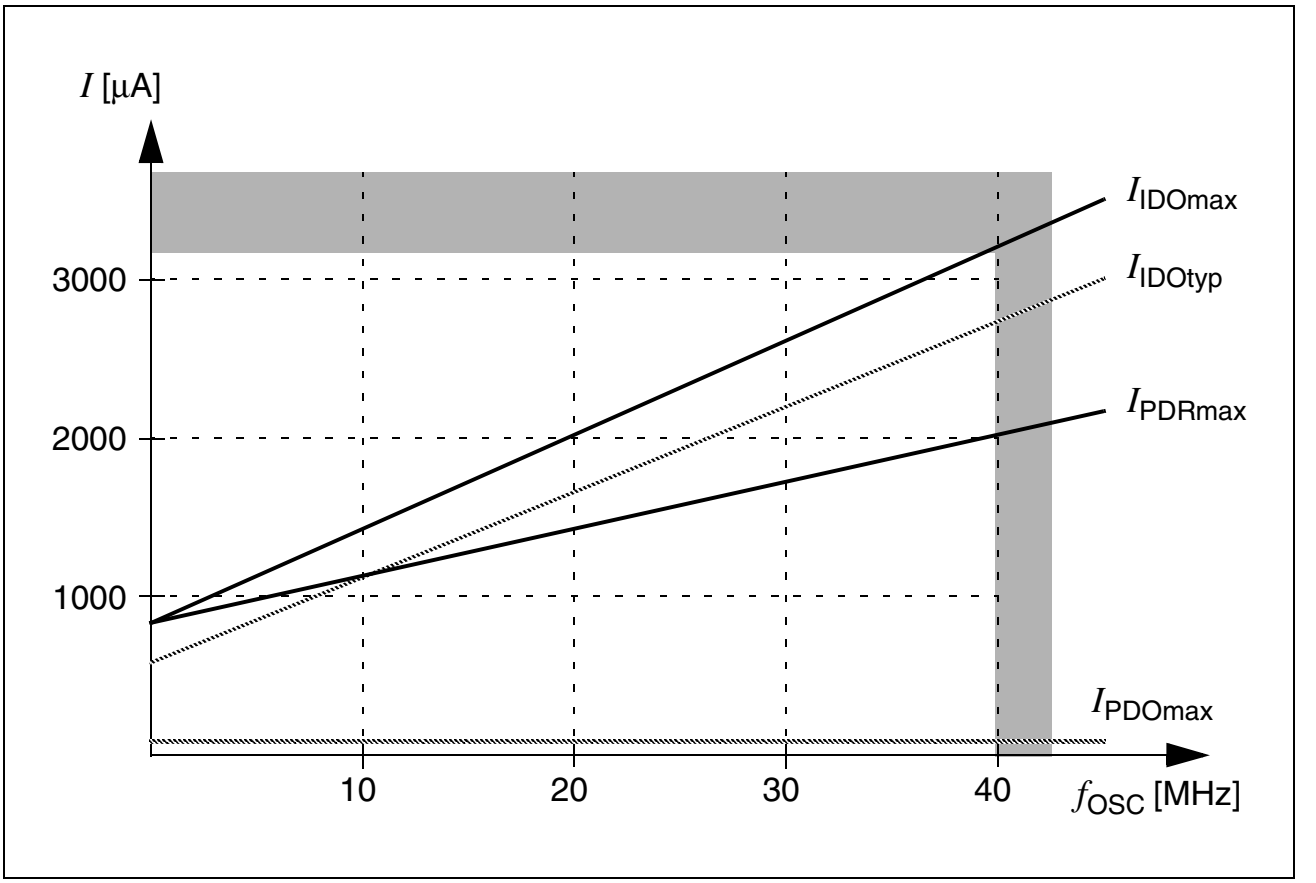


**Figure 9** **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

Due to this adaptation to the input clock the frequency of $f_{CPU}$ is constantly adjusted so it is locked to $f_{OSC}$. The slight variation causes a jitter of $f_{CPU}$ which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 12**).
For a period of $N \times$ TCL the minimum value is computed using the corresponding deviation $D_N$:

$$(N \times \text{TCL})_{min} = N \times \text{TCL}_{NOM} - D_N;\ D_N\ [\text{ns}] = \pm(13.3 + N \times 6.3) / f_{CPU}\ [\text{MHz}],$$

where $N$ = number of consecutive TCLs and $1 \le N \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 25 = 1.288$ ns, and $(3\text{TCL})_{min} = 3\text{TCL}_{NOM} - 1.288$ ns = 58.7 ns (@ $f_{CPU}$ = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

*Note: For all periods longer than 40 TCL the N = 40 value can be used (see **Figure 12**).*

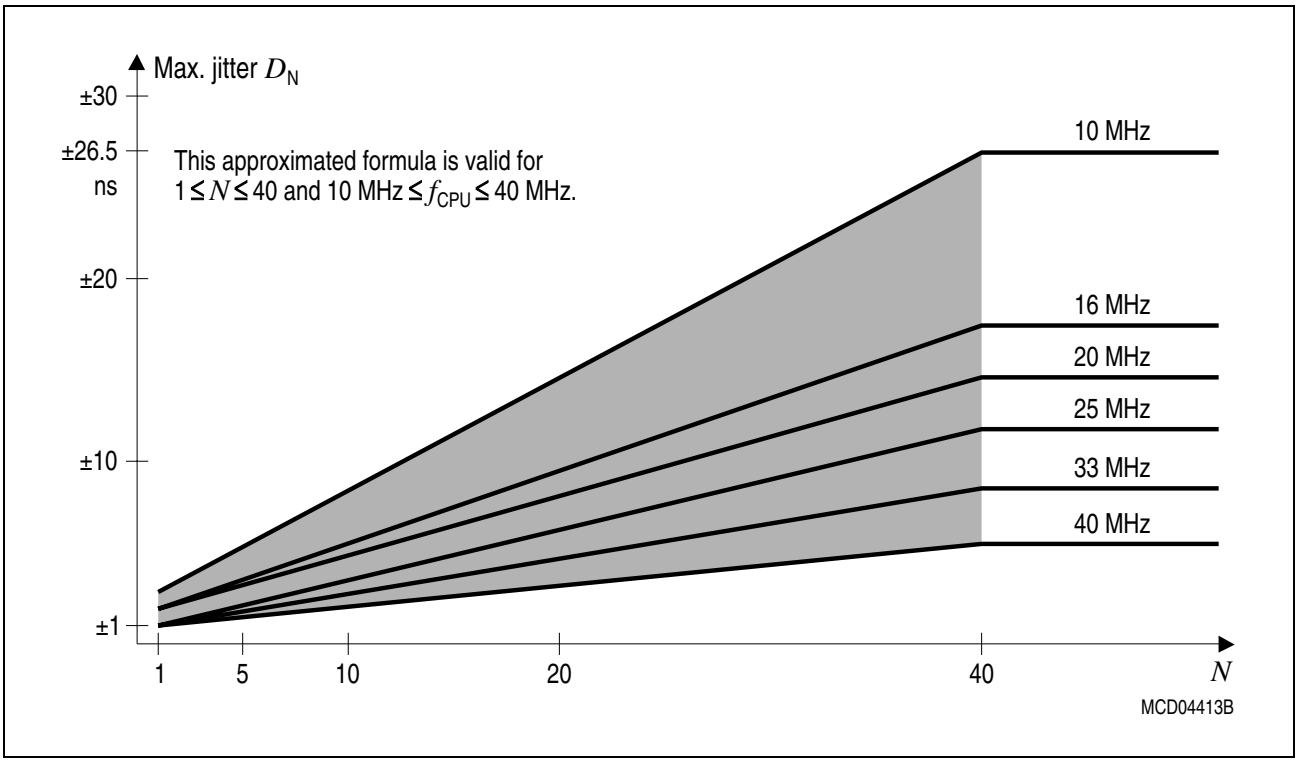


**Figure 12 Approximated Maximum Accumulated PLL Jitter**

## AC Characteristics
## External Clock Drive XTAL1
(Operating Conditions apply)

**Table 12 External Clock Drive Characteristics**

| Parameter | Symbol | | Direct Drive 1:1 | | Prescaler 2:1 | | PLL 1:N | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | min. | max. | min. | max. | min. | max. | |
| Oscillator period | $t_{OSC}$ | SR | 25 | – | 20 | – | 37[1] | 500[1] | ns |
| High time[2] | $t_1$ | SR | 12[3] | – | 5 | – | 10 | – | ns |
| Low time[2] | $t_2$ | SR | 12[3] | – | 5 | – | 10 | – | ns |
| Rise time[2] | $t_3$ | SR | – | 8 | – | 5 | – | 10 | ns |
| Fall time[2] | $t_4$ | SR | – | 8 | – | 5 | – | 10 | ns |

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels $V_{IL2}$ and $V_{IH2}$.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency ($f_{CPU}$) in direct drive mode depends on the duty cycle of the clock input signal.

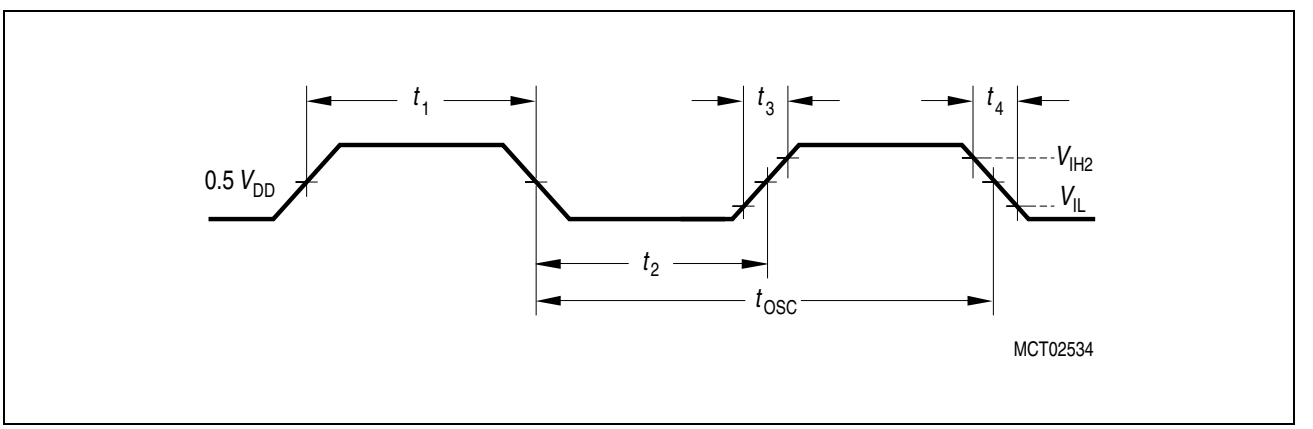


**Figure 13 External Clock Drive XTAL1**

*Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.*
*It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.*
*When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).*

## AC Characteristics

**Table 15 CLKOUT Reference Signal**

| Parameter | Symbol | | Limits | | Unit |
|---|---|---|---|---|---|
| | | | min. | max. | |
| CLKOUT cycle time | $tc_5$ | CC | 40/30/25[1)] | | ns |
| CLKOUT high time | $tc_6$ | CC | 8 | – | ns |
| CLKOUT low time | $tc_7$ | CC | 6 | – | ns |
| CLKOUT rise time | $tc_8$ | CC | – | 4 | ns |
| CLKOUT fall time | $tc_9$ | CC | – | 4 | ns |

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to $f_{CPU}$ = 25/33/40 MHz). For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for $f_{CPU}$ > 25 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

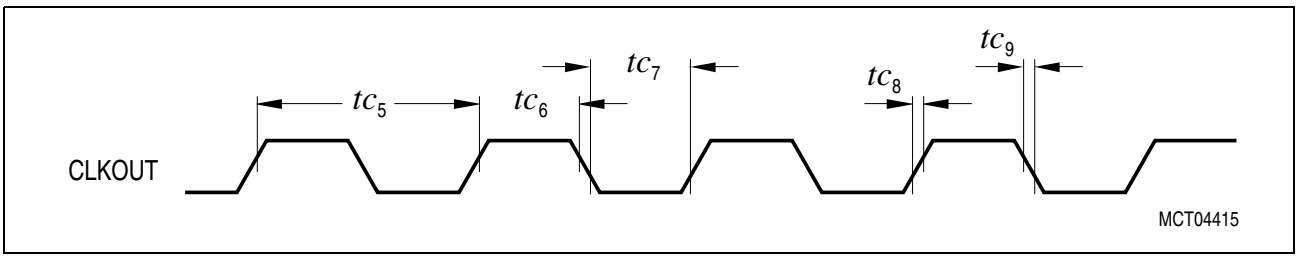


**Figure 16 CLKOUT Signal Timing**

### Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

**Table 16 Variable Memory Cycles**

| Bus Cycle Type | Bus Cycle Duration | Unit | 25/33/40 MHz, 0 Waitstates |
|---|---|---|---|
| Demultiplexed bus cycle with normal ALE | 4 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>) | TCL | 80 ns / 60.6 ns / 50 ns |
| Demultiplexed bus cycle with extended ALE | 6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>) | TCL | 120 ns / 90.9 ns / 75 ns |
| Multiplexed bus cycle with normal ALE | 6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>) | TCL | 120 ns / 90.9 ns / 75 ns |
| Multiplexed bus cycle with extended ALE | 8 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>) | TCL | 160 ns / 121.2 ns / 100 ns |

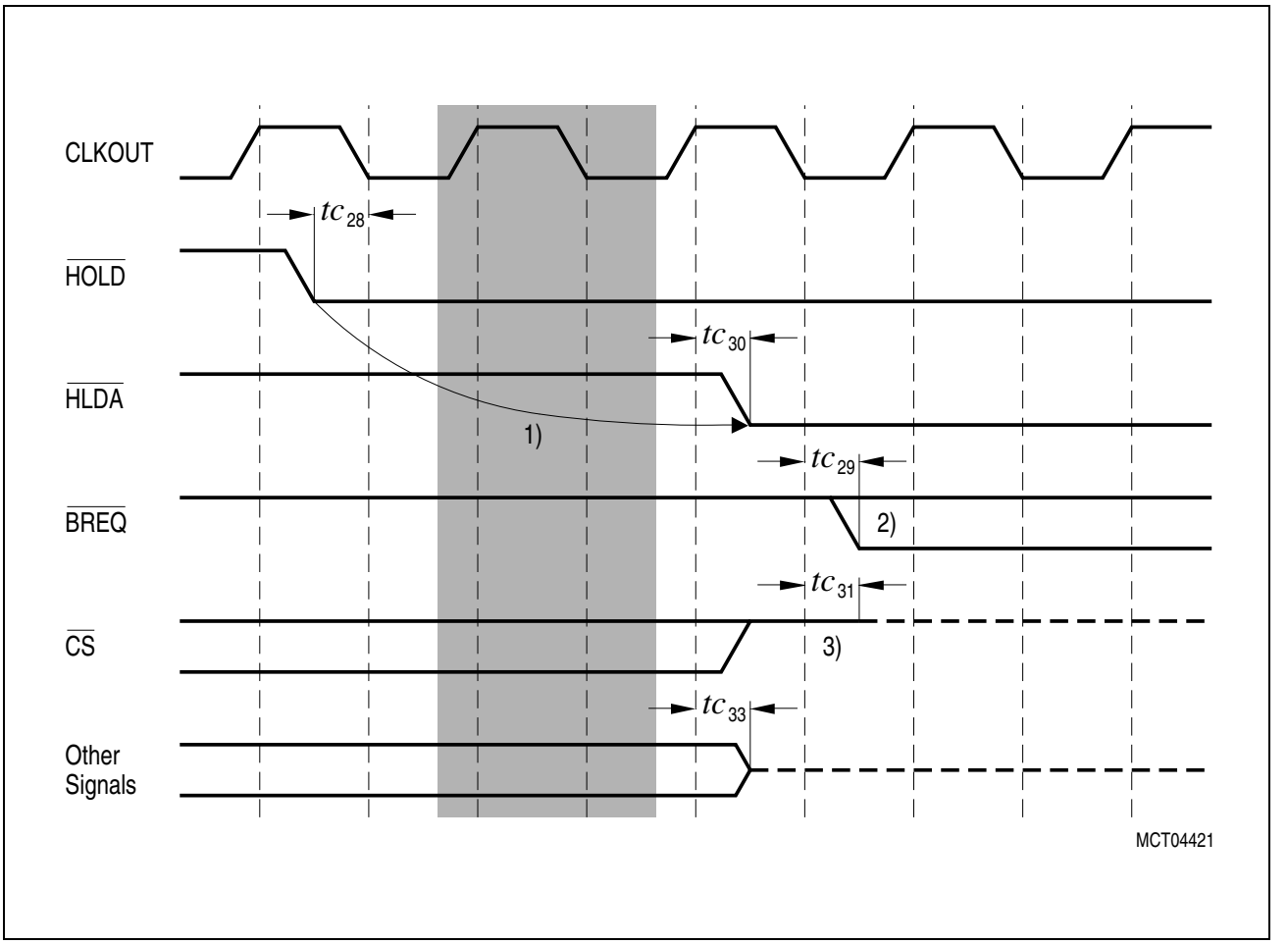


**Figure 22 External Bus Arbitration, Releasing the Bus**

**Notes**
1) The C167CS will complete the currently running bus cycle before granting bus access.
2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after $t_{33}$. Latched $\overline{\text{CS}}$ outputs are driven high for 1 TCL before the output drivers are switched off.

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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