Infineon Technologies - C167CSL40MCAKXUMA2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167csl40mcakxuma2

16-Bit Single-Chip Microcontroller **C167CS**
C166 Family

C167CS-4R, C167CS-L

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80/60/50 ns Instruction Cycle Time at 25/33/40 MHz CPU Clock
  - 400/303/250 ns Multiplication (16 × 16 bit), 800/606/500 ns Division (32-/16-bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40/30/25 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
  - 3 KBytes On-Chip Internal RAM (IRAM)
  - 8 KBytes On-Chip Extension RAM (XRAM)
  - 32 KBytes On-Chip Program Mask ROM
- On-Chip Peripheral Modules
  - 24-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - Two 16-Channel Capture/Compare Units
  - 4-Channel PWM Unit
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - Two On-Chip CAN Interfaces (Rev. 2.0B active) with 2 × 15 Message Objects (Full CAN/Basic CAN), can work on one bus with 30 objects
  - On-Chip Real Time Clock
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The Port 4 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 4 is selectable (TTL or special). Port 4 can be used to output the segment address lines and for serial interface lines:[1)]
P4.0	85	O	A16 Least Significant Segment Address Line
P4.1	86	O	A17 Segment Address Line
P4.2	87	O	A18 Segment Address Line
P4.3	88	O	A19 Segment Address Line
P4.4	89	O	A20 Segment Address Line,
		I	CAN2_RxD CAN 2 Receive Data Input
P4.5	90	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	91	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output,
		O	CAN2_TxD CAN 2 Transmit Data Output
P4.7	92	O	A23 Most Significant Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input,
		O	CAN2_TxD CAN 2 Transmit Data Output,
		I	CAN2_RxD CAN 2 Receive Data Input
$\overline{RD}$	95	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	96	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
P1L.0-7	118-125		
P1H.0-7	128-135		
P1L.0	118	I	AN16 Analog Input Channel 16
P1L.1	119	I	AN17 Analog Input Channel 17
P1L.2	120	I	AN18 Analog Input Channel 18
P1L.3	121	I	AN19 Analog Input Channel 19
P1L.4	122	I	AN20 Analog Input Channel 20
P1L.5	123	I	AN21 Analog Input Channel 21
P1L.6	124	I	AN22 Analog Input Channel 22
P1L.7	125	I	AN23 Analog Input Channel 23
P1H.4	132	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	133	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	134	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	135	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Functional Description

The architecture of the C167CS combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

Figure 3 gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CS.

Note: All time specifications refer to a CPU clock of 40 MHz (see definition in the AC Characteristics section).

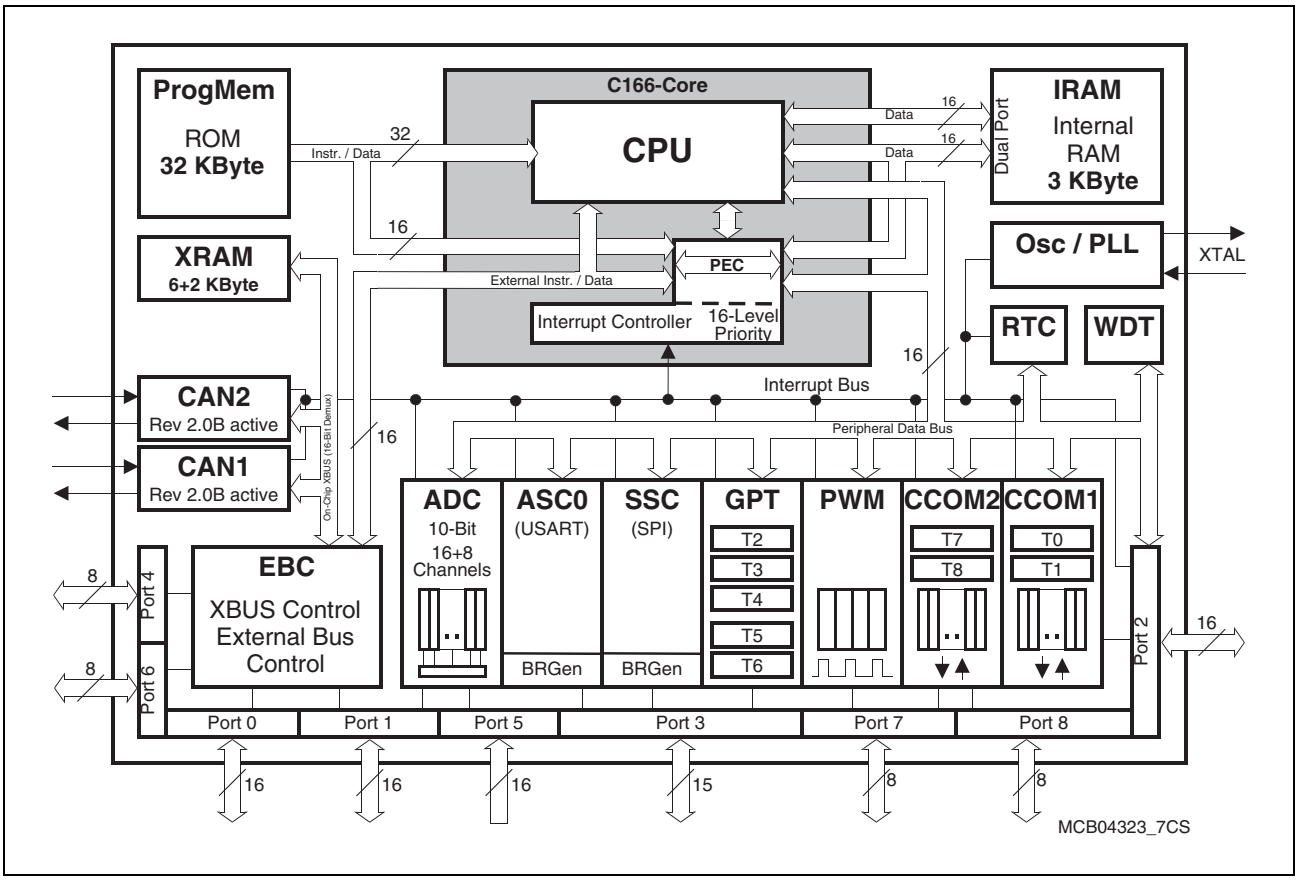


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN) of the C167CS can be individually enabled or disabled during initialization. Register XPERCON selects the required modules which are then enabled by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.

Note: The default value of register XPERCON after reset selects 2 KByte XRAM and module CAN1, so the default XBUS resources are compatible with the C167CR.

Memory Organization

The memory space of the C167CS is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C167CS incorporates 32 KBytes of on-chip mask-programmable ROM (not in the ROM-less derivative, of course) for code or constant data. The 32 KBytes of the on-chip ROM can be mapped either to segment 0 or segment 1.

3 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

8 KBytes of on-chip Extension RAM (XRAM), organized as two blocks of 2 KByte and 6 KByte, respectively, are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bitaddressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C167CS offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Note: When one or both of the on-chip CAN Modules are used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 ... A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CS's instructions can be executed in just one machine cycle which requires 50 ns at 40 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

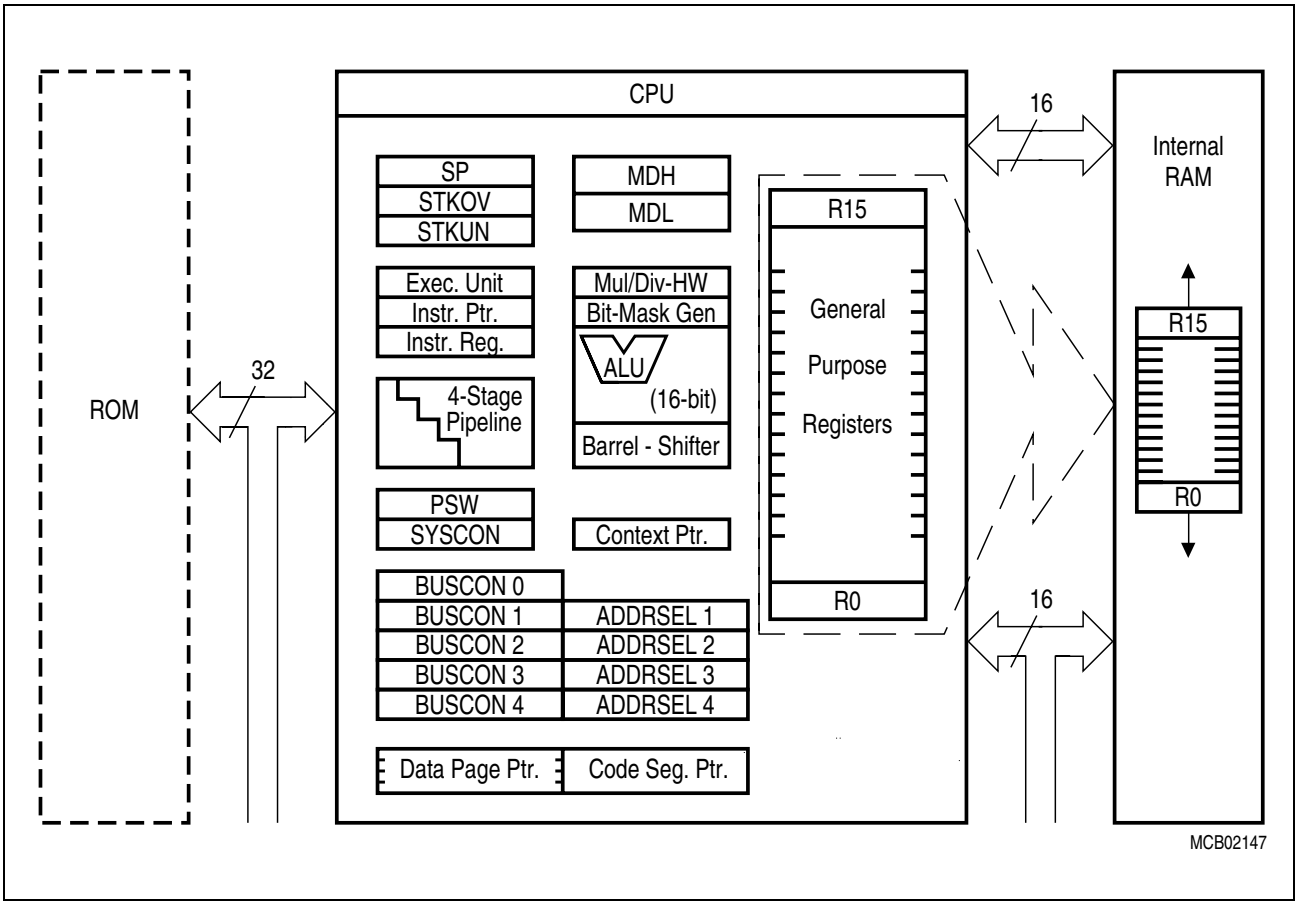


Figure 4 CPU Block Diagram

The C167CS also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	 RESET RESET RESET	 $00'0000_H$ $00'0000_H$ $00'0000_H$	 00_H 00_H 00_H	 III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 $00'0008_H$ $00'0010_H$ $00'0018_H$	 02_H 04_H 06_H	 II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	 UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP	 $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$	 $0A_H$ $0A_H$ $0A_H$ $0A_H$ $0A_H$	 I I I I I
Reserved	–	–	$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	–
Software Traps – TRAP Instruction	–	–	Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

Table 6 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

Table 7 lists all SFRs which are implemented in the C167CS in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 7 C167CS Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	---	CAN1 Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	---	CAN1 Control/Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	---	CAN1 Global Mask Short	$UFUU_H$
C1PCIR	$EF02_H$ **X**	---	CAN1 Port Control/Interrupt Register	$XXXX_H$
C1LGML	$EF0A_H$ **X**	---	CAN1 Lower Global Mask Long	$UUUU_H$
C1LMLM	$EF0E_H$ **X**	---	CAN1 Lower Mask of Last Message	$UUUU_H$

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
DP1L b	$F104_H$ E	82_H	P1L Direction Control Register	00_H
DP1H b	$F106_H$ E	83_H	P1H Direction Control Register	00_H
DP2 b	$FFC2_H$	$E1_H$	Port 2 Direction Control Register	0000_H
DP3 b	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 b	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP6 b	$FFCE_H$	$E7_H$	Port 6 Direction Control Register	00_H
DP7 b	$FFD2_H$	$E9_H$	Port 7 Direction Control Register	00_H
DP8 b	$FFD6_H$	EB_H	Port 8 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON b	$F1C0_H$ E	$E0_H$	External Interrupt Control Register	0000_H
EXISEL b	$F1DA_H$ E	ED_H	External Interrupt Source Select Reg.	0000_H
FOCON b	$FFAA_H$	$D5_H$	Frequency Output Control Register	0000_H
IDCHIP	$F07C_H$ E	$3E_H$	Identifier	$0CXX_H$
IDMANUF	$F07E_H$ E	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ E	$3D_H$	Identifier	$X040_H$
IDMEM2	$F076_H$ E	$3B_H$	Identifier	$XXXX_H$
IDPROG	$F078_H$ E	$3C_H$	Identifier	$XXXX_H$
ISNC b	$F1DE_H$ E	EF_H	Interrupt Subnode Control Register	0000_H
MDC b	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 b	$F1C2_H$ E	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 b	$F1C6_H$ E	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4 b	$F1CA_H$ E	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP6 b	$F1CE_H$ E	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7 b	$F1D2_H$ E	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8 b	$F1D6_H$ E	EB_H	Port 8 Open Drain Control Register	00_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Reg. (read only)	XX_H
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Register (write only)	00_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP		$FE12_H$		09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR		$F0B4_H$	**E**	$5A_H$	SSC Baudrate Register	0000_H
SSCCON	**b**	$FFB2_H$		$D9_H$	SSC Control Register	0000_H
SSCEIC	**b**	$FF76_H$		BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB		$F0B2_H$	**E**	59_H	SSC Receive Buffer	$XXXX_H$
SSCRIC	**b**	$FF74_H$		BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB		$F0B0_H$	**E**	58_H	SSC Transmit Buffer	0000_H
SSCTIC	**b**	$FF72_H$		$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV		$FE14_H$		$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN		$FE16_H$		$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON	**b**	$FF12_H$		89_H	CPU System Configuration Register	[1] $0XX0_H$
SYSCON1	**b**	$F1DC_H$	**E**	EE_H	CPU System Configuration Register 1	0000_H
SYSCON2	**b**	$F1D0_H$	**E**	$E8_H$	CPU System Configuration Register 2	0000_H
SYSCON3	**b**	$F1D4_H$	**E**	EA_H	CPU System Configuration Register 3	0000_H
T0		$FE50_H$		28_H	CAPCOM Timer 0 Register	0000_H
T01CON	**b**	$FF50_H$		$A8_H$	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000_H
T0IC	**b**	$FF9C_H$		CE_H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000_H
T0REL		$FE54_H$		$2A_H$	CAPCOM Timer 0 Reload Register	0000_H
T1		$FE52_H$		29_H	CAPCOM Timer 1 Register	0000_H
T1IC	**b**	$FF9E_H$		CF_H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000_H
T1REL		$FE56_H$		$2B_H$	CAPCOM Timer 1 Reload Register	0000_H

Table 10 Current Limits for Port Output Drivers

Port Output Driver	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
P2.7 - P2.0	10 mA	2.5 mA
(PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$, $\overline{RSTIN}$[2])	-----	2.5 mA
All other outputs	-----	1.6 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins (P2.7-P2.0 only) at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and/or $\Sigma -I_{OH}$) must remain below 50 mA.

2) Valid for V_{OL} in bidirectional reset mode only.

Power Consumption C167CS

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD5}	–	20 + 3.2 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX5}[2]	–	15 + 1.4 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[3][2]	–	800 + 60 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[3][2]	–	800 + 30 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][4]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[4]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) These values are not 100% tested but verified by means of system characterization.

3) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 9**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry (see also application notes AP2420: Crystal Oscillator, AP2424: Ceramic Resonator Oscillator).

4) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

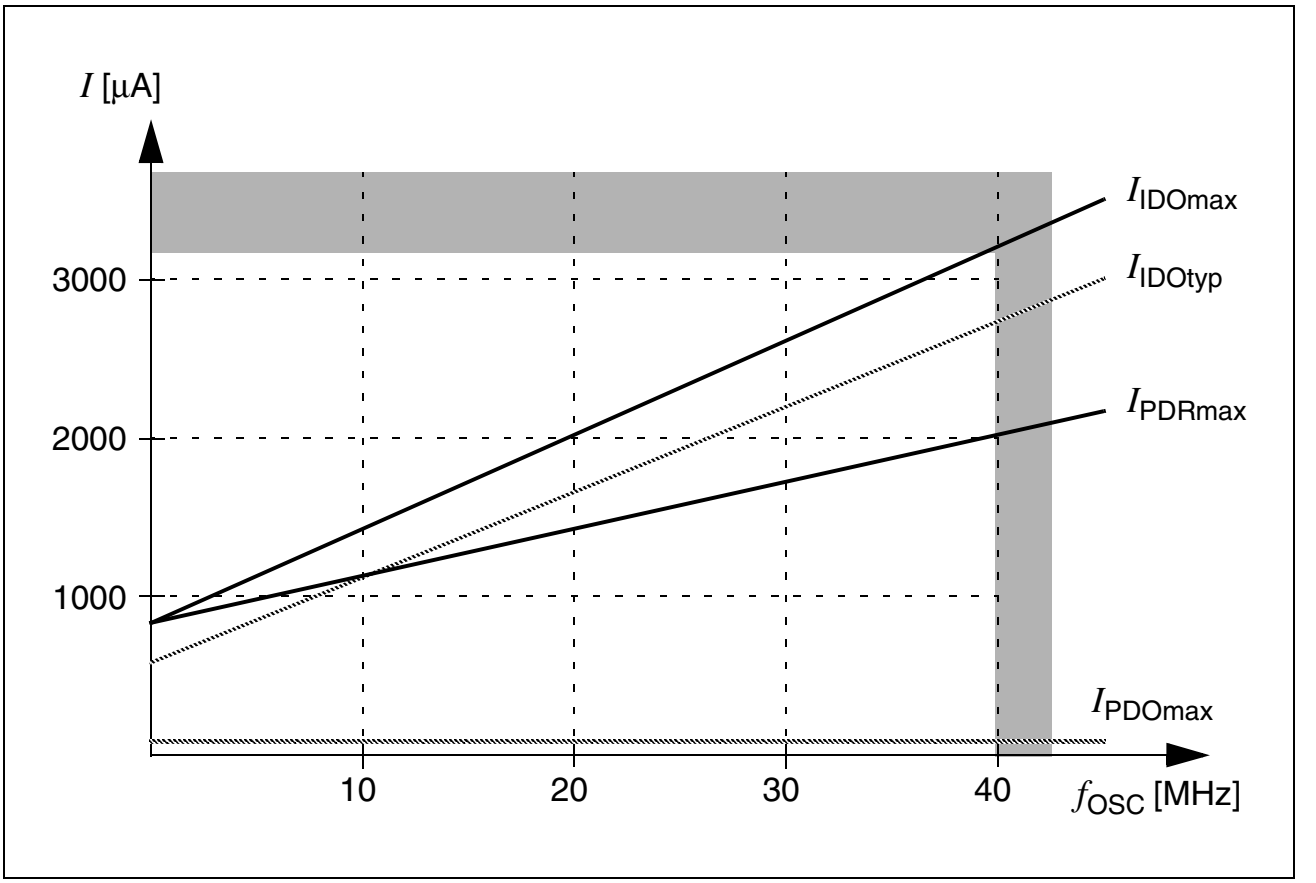


Figure 9 **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 12**).
For a period of $N \times$ TCL the minimum value is computed using the corresponding deviation D_N:

$$(N \times \text{TCL})_{min} = N \times \text{TCL}_{NOM} - D_N;\ D_N\ [\text{ns}] = \pm(13.3 + N \times 6.3) / f_{CPU}\ [\text{MHz}],$$

where N = number of consecutive TCLs and $1 \le N \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 25 = 1.288$ ns, and $(3\text{TCL})_{min} = 3\text{TCL}_{NOM} - 1.288$ ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

*Note: For all periods longer than 40 TCL the N = 40 value can be used (see **Figure 12**).*

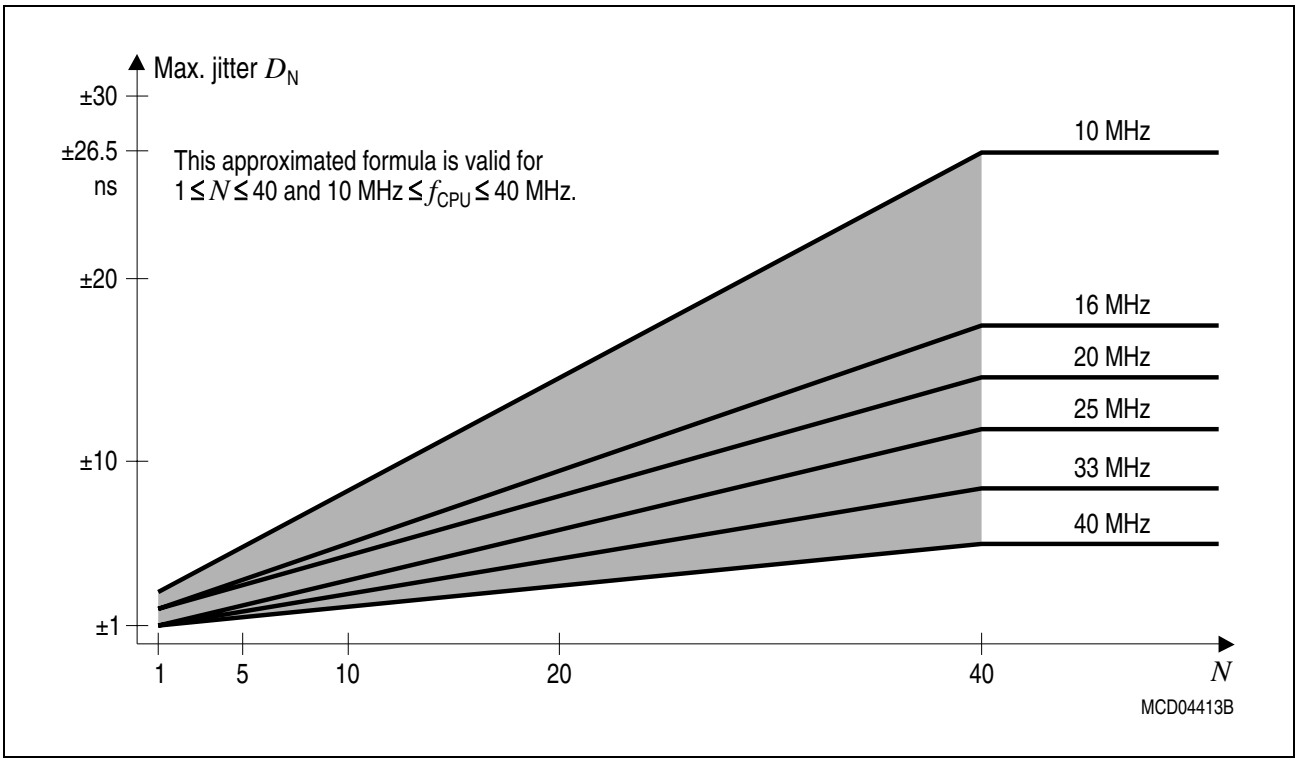
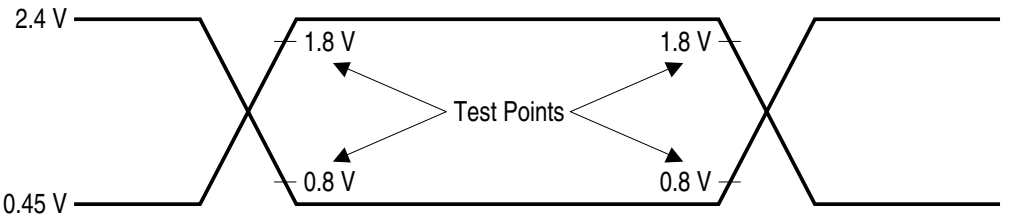


Figure 12 Approximated Maximum Accumulated PLL Jitter

Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.45 V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

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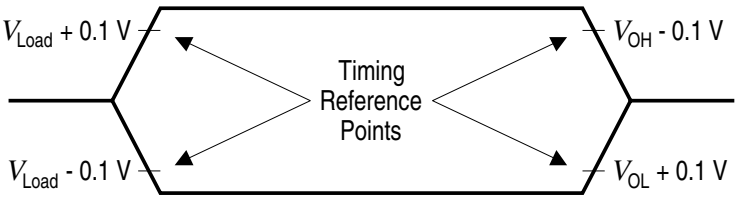
Figure 14 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

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Figure 15 Float Waveforms

AC Characteristics

Table 15 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			min.	max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1)]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for f_{CPU} > 25 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

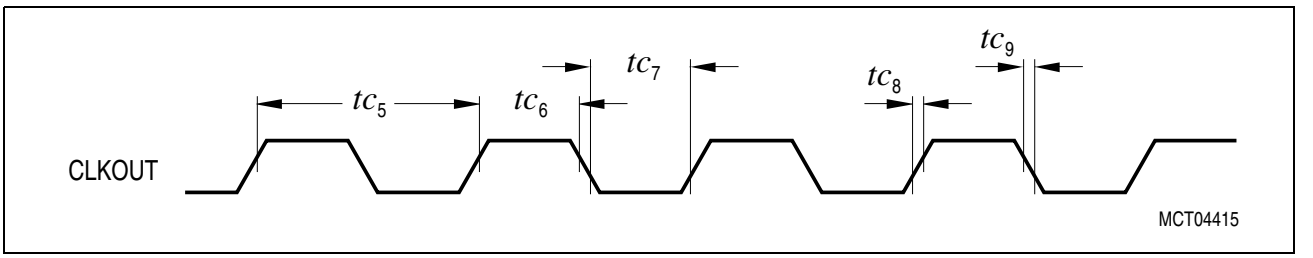


Figure 16 CLKOUT Signal Timing

Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

Table 16 Variable Memory Cycles

Bus Cycle Type	Bus Cycle Duration	Unit	25/33/40 MHz, 0 Waitstates
Demultiplexed bus cycle with normal ALE	4 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	80 ns / 60.6 ns / 50 ns
Demultiplexed bus cycle with extended ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns / 90.9 ns / 75 ns
Multiplexed bus cycle with normal ALE	6 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	120 ns / 90.9 ns / 75 ns
Multiplexed bus cycle with extended ALE	8 + 2 × (15 - <MCTC>) + 2 × (1 - <MTTC>)	TCL	160 ns / 121.2 ns / 100 ns

Bus Cycle Control via $\overline{\text{READY}}$ Input

The duration of an external bus cycle can be controlled by the external circuitry via the $\overline{\text{READY}}$ input signal.

Synchronous $\overline{\text{READY}}$ permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous $\overline{\text{READY}}$ puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage.

Table 19 $\overline{\text{READY}}$ Timing (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input setup time to CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{25} CC	12	–	ns
Input hold time after CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{26} CC	0	–	ns
Asynchronous $\overline{\text{READY}}$ input low time[3)]	tc_{27} CC	$tc_5 + tc_{25}$	–	ns

Notes (Valid for **Table 19** and **Figure 21**)

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus **with** MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus **without** MTTC waitstate this delay is zero.
3) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT, it must fulfill tc_{27} in order to be safely synchronized.
Proper deactivation of $\overline{\text{READY}}$ is guaranteed if $\overline{\text{READY}}$ is deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
4) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a $\overline{\text{READY}}$ controlled waitstate,
$\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
5) If the next following bus cycle is $\overline{\text{READY}}$ controlled, an active $\overline{\text{READY}}$ signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the MTTC waitstate of the current cycle, and on the MCTC waitstates and the ALE mode of the next following cycle. If the current cycle uses a multiplexed bus the intrinsic MUX waitstate adds another CLKOUT cycle to the $\overline{\text{READY}}$ deactivation time.

External Bus Arbitration

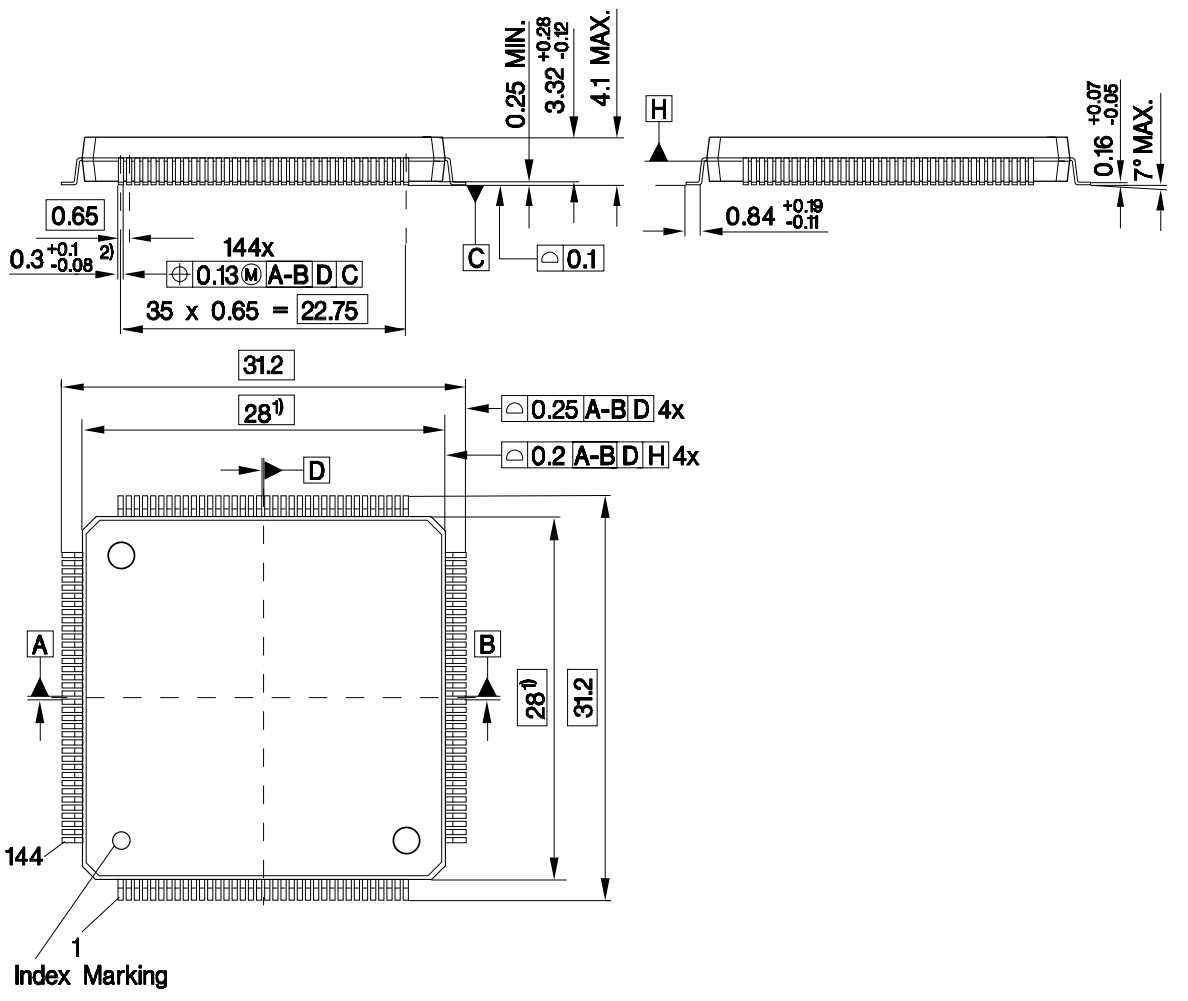
Table 20 Bus Arbitration Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT falling edge	tc_{28}	SR	14	–	ns
CLKOUT to $\overline{\text{BREQ}}$ delay	tc_{29}	CC	-3	6	ns
CLKOUT to $\overline{\text{HLDA}}$ delay	tc_{30}	CC	-2	6	ns
$\overline{\text{CSx}}$ release[1)]	tc_{31}	CC	0	10	ns
$\overline{\text{CSx}}$ drive	tc_{32}	CC	-3	4	ns
Other signals release[1)]	tc_{33}	CC	0	10	ns
Other signals drive[1)]	tc_{34}	CC	0	6	ns

1) Not 100% tested, guaranteed by design and characterization.

Package Outlines

P-MQFP-144-6
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPM09391

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm