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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167cslmcabxqla2

Revision History:	2001-08	V2.2
Previous Version:	2000-12	V2.1 (Intermediate version)
	2000-06	V2.0
	1999-06	
	1999-03	(Advance Information)

Page	Subjects (major changes from V2.1, 2000-12 to V2.2, 2001-08)
4	**Figure 2** corrected (pins 98, 99)
25, 27	**Figure 5** and **Figure 6** updated
50ff	Output voltage/current specification improved
52f	Limit values for I_{IDO} and I_{PDR} increased due to the usage of a standard oscillator
54	**Figure 10** corrected
57	**Figure 12** updated for 40 MHz
59	Clock parameters adjusted
60	TUE note includes P1H
76	Package drawing updated[1)]

Page	Subjects (major changes from V2.0, 2000-06 to V2.1, 2000-12)
All	Maximum operating frequency updated to 40 MHz
2	Derivative table updated
52	$\overline{\text{RSTIN}}$ level for I_{DD} corrected to V_{IL} (was V_{IL2})
53	Current unit corrected to µA
56	Input clock range adjusted
60f	Note 5 detailed
64	Parameters tc_{10}, tc_{12}, tc_{13}, tc_{14}, tc_{15}, tc_{16}, tc_{17}, tc_{18}, tc_{19} changed
65	Relative bus timing parameters added
70	Parameter tc_{25} changed, notes adapted
71	Notes adapted
72	Parameter tc_{28} changed
75	Parameters t_{42}, t_{43}, t_{44}, t_{46}, t_{47} changed

1) New package due to new assembly line. MQFP-144-1 for current deliveries only, will be discontinued.

Controller Area Network (CAN): License of Robert Bosch GmbH

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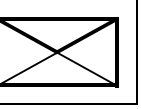

- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C167CS Derivative Synopsis

Derivative[1)]	Program Memory	Operating Frequency
SAK-C167CS-LM SAB-C167CS-LM	---	25 MHz
SAK-C167CS-L33M SAB-C167CS-L33M	---	33 MHz
SAK-C167CS-L40M SAB-C167CS-L40M	---	40 MHz
SAK-C167CS-4RM SAB-C167CS-4RM	32 KByte ROM	25 MHz
SAK-C167CS-4R33M SAB-C167CS-4R33M	32 KByte ROM	33 MHz
SAK-C167CS-4R40M SAB-C167CS-4R40M	32 KByte ROM	40 MHz

1) This Data Sheet is valid for devices starting with and including design step BA.

For simplicity all versions are referred to by the term **C167CS** throughout this document.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	T×D0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	R×D0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
		O	FOUT	Programmable Frequency Output
N.C.	84	–	This pin is not connected in the C167CS. No connection to the PCB is required.	

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CS to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
PORT0 P0L.0-7 P0H.0-7	 100-107 108, 111-117	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 – D7 P0H.0 – P0H.7: I/O D8 – D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15

Memory Organization

The memory space of the C167CS is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C167CS incorporates 32 KBytes of on-chip mask-programmable ROM (not in the ROM-less derivative, of course) for code or constant data. The 32 KBytes of the on-chip ROM can be mapped either to segment 0 or segment 1.

3 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

8 KBytes of on-chip Extension RAM (XRAM), organized as two blocks of 2 KByte and 6 KByte, respectively, are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bitaddressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C167CS instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 3 C167CS Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H

Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘capture’d) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

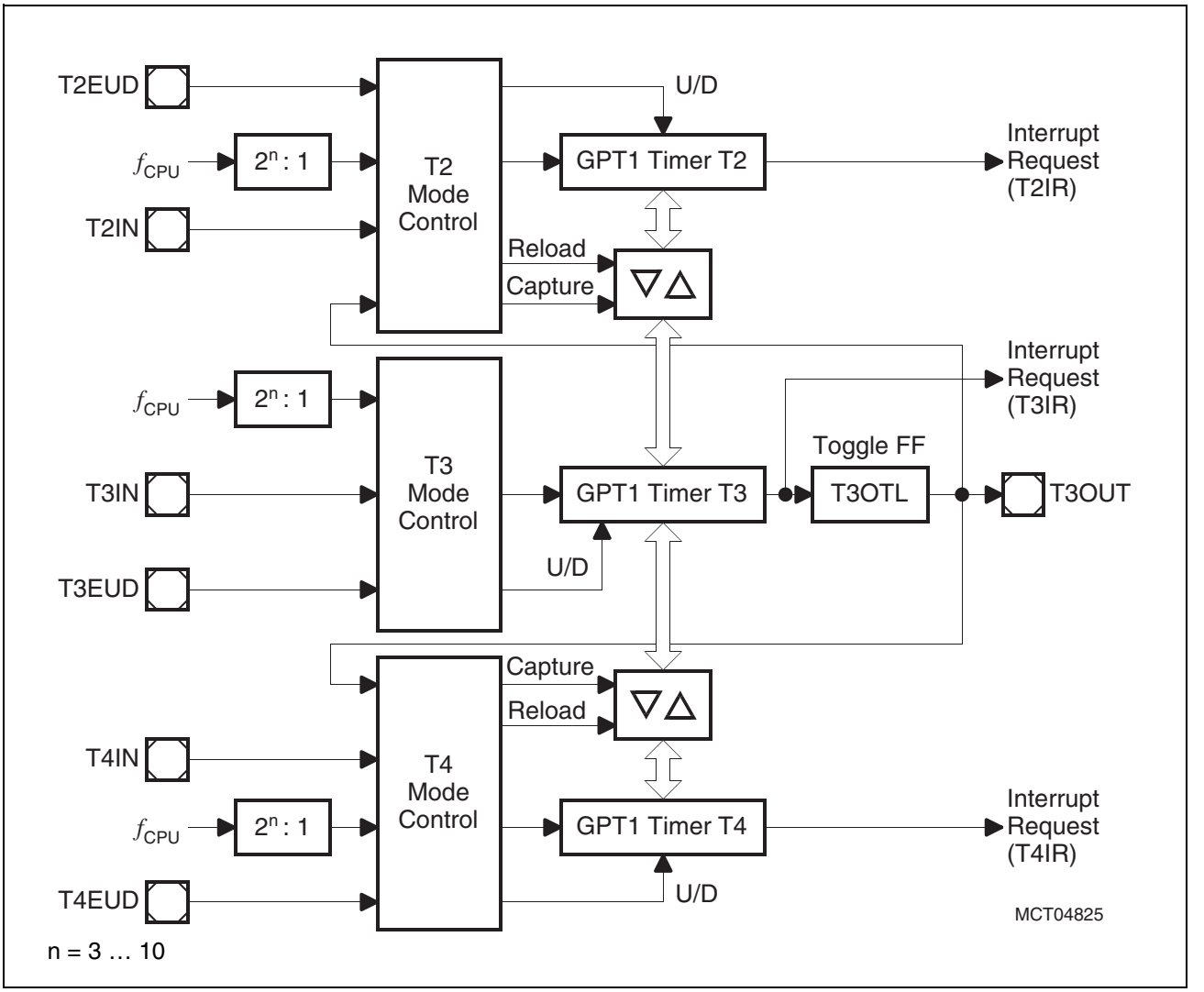

Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 24 multiplexed input channels (16 standard channels and 8 extension channels) and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 24 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CS supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels (standard or extension) are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via registers P5DIDIS (Port 5 Digital Input Disable) and P1DIDIS (PORT1 Digital Input Disable).

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 Kbit/s/ 1.03 Mbit/s/1.25 Mbit/s and half-duplex synchronous communication at up to 3.1/ 4.1 Mbit/s/5.0 Mbit/s (@ 25/33/40 MHz CPU clock).
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25/8.25/10 Mbit/s (@ 25/33/40 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 3 separate interrupt vectors are provided.
The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
DP1L b	$F104_H$ E	82_H	P1L Direction Control Register	00_H
DP1H b	$F106_H$ E	83_H	P1H Direction Control Register	00_H
DP2 b	$FFC2_H$	$E1_H$	Port 2 Direction Control Register	0000_H
DP3 b	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 b	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP6 b	$FFCE_H$	$E7_H$	Port 6 Direction Control Register	00_H
DP7 b	$FFD2_H$	$E9_H$	Port 7 Direction Control Register	00_H
DP8 b	$FFD6_H$	EB_H	Port 8 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON b	$F1C0_H$ E	$E0_H$	External Interrupt Control Register	0000_H
EXISEL b	$F1DA_H$ E	ED_H	External Interrupt Source Select Reg.	0000_H
FOCON b	$FFAA_H$	$D5_H$	Frequency Output Control Register	0000_H
IDCHIP	$F07C_H$ E	$3E_H$	Identifier	$0CXX_H$
IDMANUF	$F07E_H$ E	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ E	$3D_H$	Identifier	$X040_H$
IDMEM2	$F076_H$ E	$3B_H$	Identifier	$XXXX_H$
IDPROG	$F078_H$ E	$3C_H$	Identifier	$XXXX_H$
ISNC b	$F1DE_H$ E	EF_H	Interrupt Subnode Control Register	0000_H
MDC b	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 b	$F1C2_H$ E	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 b	$F1C6_H$ E	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4 b	$F1CA_H$ E	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP6 b	$F1CE_H$ E	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7 b	$F1D2_H$ E	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8 b	$F1D6_H$ E	EB_H	Port 8 Open Drain Control Register	00_H

Absolute Maximum Ratings

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics (cont'd)
(Operating Conditions apply)[1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{\text{RSTIN}}$ inactive current[6)]	I_{RSTH}[7)]	–	-10	µA	$V_{IN} = V_{IH1}$
$\overline{\text{RSTIN}}$ active current[6)]	I_{RSTL}[8)]	-100	–	µA	$V_{IN} = V_{IL}$
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ inact. current[9)]	I_{RWH}[7)]	–	-40	µA	V_{OUT} = 2.4 V
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ active current[9)]	I_{RWL}[8)]	-500	–	µA	$V_{OUT} = V_{OLmax}$
ALE inactive current[9)]	I_{ALEL}[7)]	–	40	µA	$V_{OUT} = V_{OLmax}$
ALE active current[9)]	I_{ALEH}[8)]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[9)]	I_{P6H}[7)]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current[9)]	I_{P6L}[8)]	-500	–	µA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current[10)]	I_{P0H}[7)]	–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{P0L}[8)]	-100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[11)] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) For pin $\overline{\text{RSTIN}}$ this specification is only valid in bidirectional reset mode.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 10**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DD}$). However, only the levels for nominal output currents are guaranteed.

5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

6) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

7) The maximum current may be drawn while the respective signal line remains inactive.

8) The minimum current must be drawn in order to drive the respective signal line active.

9) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$-pullup is always active, except for Powerdown mode.

10) This specification is valid during Reset and during Adapt-mode.

11) Not 100% tested, guaranteed by design and characterization.

Table 10 Current Limits for Port Output Drivers

Port Output Driver	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
P2.7 - P2.0	10 mA	2.5 mA
(PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$, $\overline{RSTIN}$[2])	-----	2.5 mA
All other outputs	-----	1.6 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins (P2.7-P2.0 only) at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and/or $\Sigma -I_{OH}$) must remain below 50 mA.

2) Valid for V_{OL} in bidirectional reset mode only.

Power Consumption C167CS

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD5}	–	20 + 3.2 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX5}[2]	–	15 + 1.4 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[3][2]	–	800 + 60 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[3][2]	–	800 + 30 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][4]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[4]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) These values are not 100% tested but verified by means of system characterization.

3) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 9**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry (see also application notes AP2420: Crystal Oscillator, AP2424: Ceramic Resonator Oscillator).

4) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

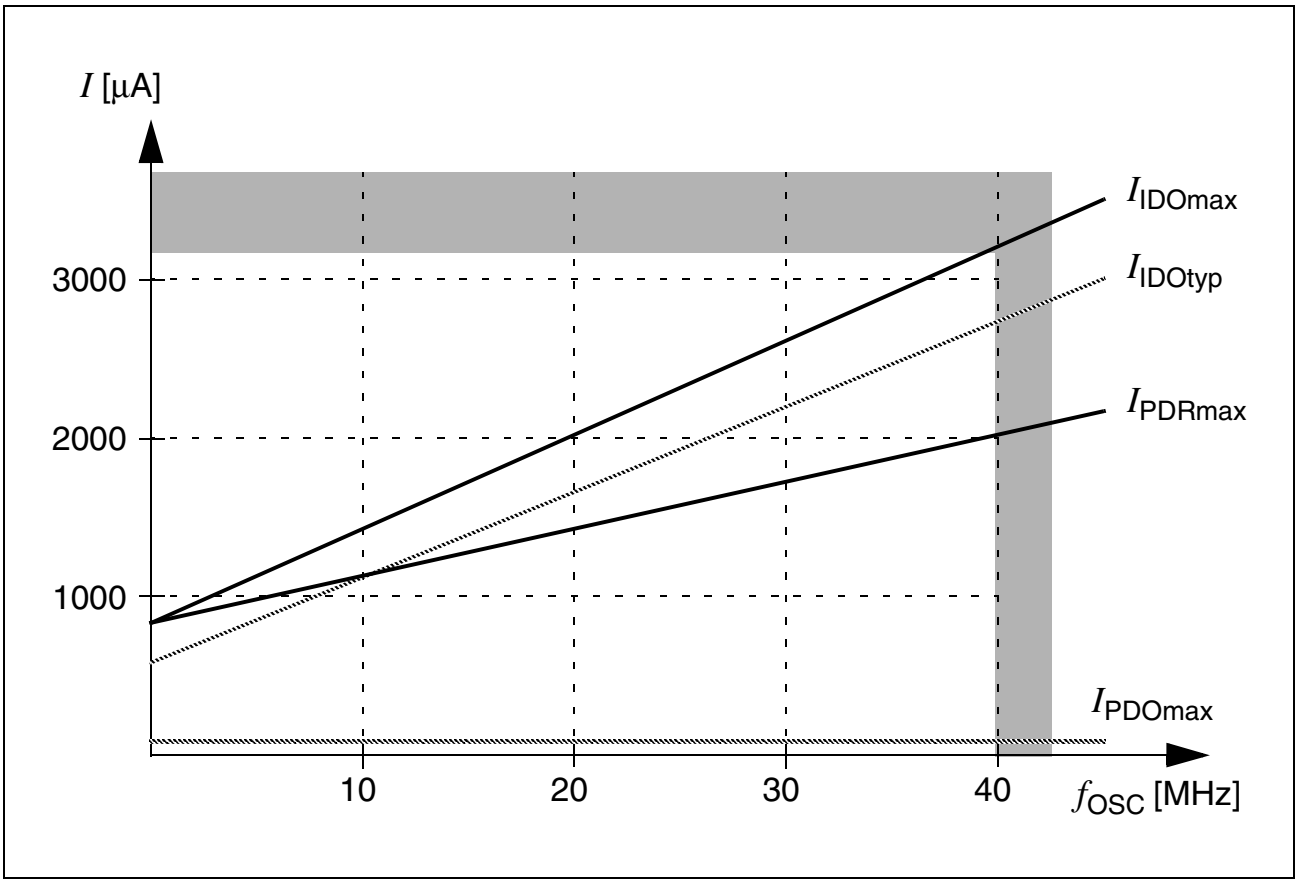

Figure 9 **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

Table 17 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			min.	max.	
Output delay from CLKOUT falling edge Valid for: address (MUX on PORT0), write data out	tc_{10}	CC	0	14	ns
Output delay from CLKOUT edge Valid for: latched $\overline{CS}$, ALE (normal)	tc_{11}	CC	-3	6	ns
Output delay from CLKOUT edge Valid for: $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{WrCS}$	tc_{12}	CC	-4	7	ns
Output delay from CLKOUT edge Valid for: $\overline{RD}$, $\overline{RdCS}$	tc_{13}	CC	-2	7	ns
Input setup time to CLKOUT falling edge Valid for: read data in	tc_{14}	SR	10	–	ns
Input hold time after CLKOUT falling edge Valid for: read data in[1)]	tc_{15}	SR	0	–	ns
Output delay from CLKOUT falling edge Valid for: address (on PORT1 and/or P4), $\overline{BHE}$	tc_{16}	CC	0	9[2)]	ns
Output hold time after CLKOUT falling edge Valid for: address, $\overline{BHE}$[3)]	tc_{17}	CC	-2	8	ns
Output hold time after CLKOUT edge[4)] Valid for: write data out	tc_{18}	CC	-1	–	ns
Output delay from CLKOUT falling edge Valid for: ALE (extended), early $\overline{CS}$	tc_{19}	CC	-4	4	ns
Turn off delay after CLKOUT edge[4)] Valid for: write data out	tc_{20}	CC	–	7	ns
Turn on delay after CLKOUT falling edge[4)] Valid for: write data out	tc_{21}	CC	-5	–	ns
Output hold time after CLKOUT edge Valid for: early $\overline{CS}$	tc_{22}	CC	-6	4	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of $\overline{RD}$. Therefore address changes before the end of $\overline{RD}$ have no impact on (demultiplexed) read cycles.

2) If the capacitive load on the respective output pins is limited to 30 pF the maximum output delay tc_{16} can be reduced to 8 ns.

3) Due to comparable propagation delays the address does not change before $\overline{WR}$ goes high. The minimum output delay (tc_{17min}) is therefore the actual value of tc_{12}.

4) Not 100% tested, guaranteed by design and characterization.

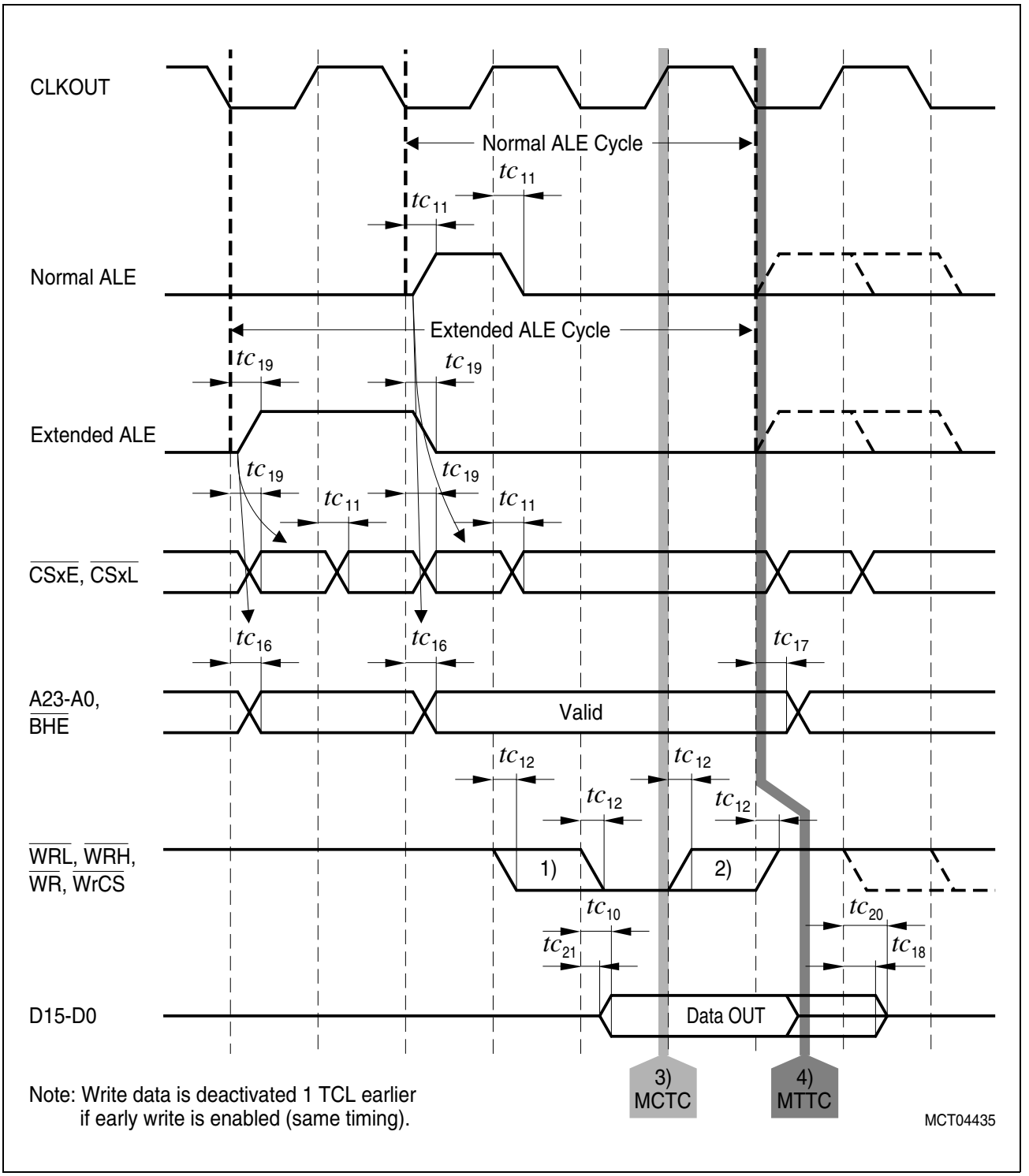

Figure 17 Demultiplexed Bus, Write Access

Bus Cycle Control via $\overline{\text{READY}}$ Input

The duration of an external bus cycle can be controlled by the external circuitry via the $\overline{\text{READY}}$ input signal.

Synchronous $\overline{\text{READY}}$ permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous $\overline{\text{READY}}$ puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage.

Table 19 $\overline{\text{READY}}$ Timing (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input setup time to CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{25} CC	12	–	ns
Input hold time after CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	tc_{26} CC	0	–	ns
Asynchronous $\overline{\text{READY}}$ input low time[3)]	tc_{27} CC	$tc_5 + tc_{25}$	–	ns

Notes (Valid for **Table 19** and **Figure 21**)

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus **with** MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus **without** MTTC waitstate this delay is zero.
3) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT, it must fulfill tc_{27} in order to be safely synchronized.
Proper deactivation of $\overline{\text{READY}}$ is guaranteed if $\overline{\text{READY}}$ is deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
4) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a $\overline{\text{READY}}$ controlled waitstate,
$\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
5) If the next following bus cycle is $\overline{\text{READY}}$ controlled, an active $\overline{\text{READY}}$ signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the MTTC waitstate of the current cycle, and on the MCTC waitstates and the ALE mode of the next following cycle. If the current cycle uses a multiplexed bus the intrinsic MUX waitstate adds another CLKOUT cycle to the $\overline{\text{READY}}$ deactivation time.