Infineon Technologies - C167CSLMCABXUMA2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167cslmcabxuma2

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Data Sheet, V2.2, Aug. 2001

C167CS-4R
C167CS-L

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CS please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C167CS derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

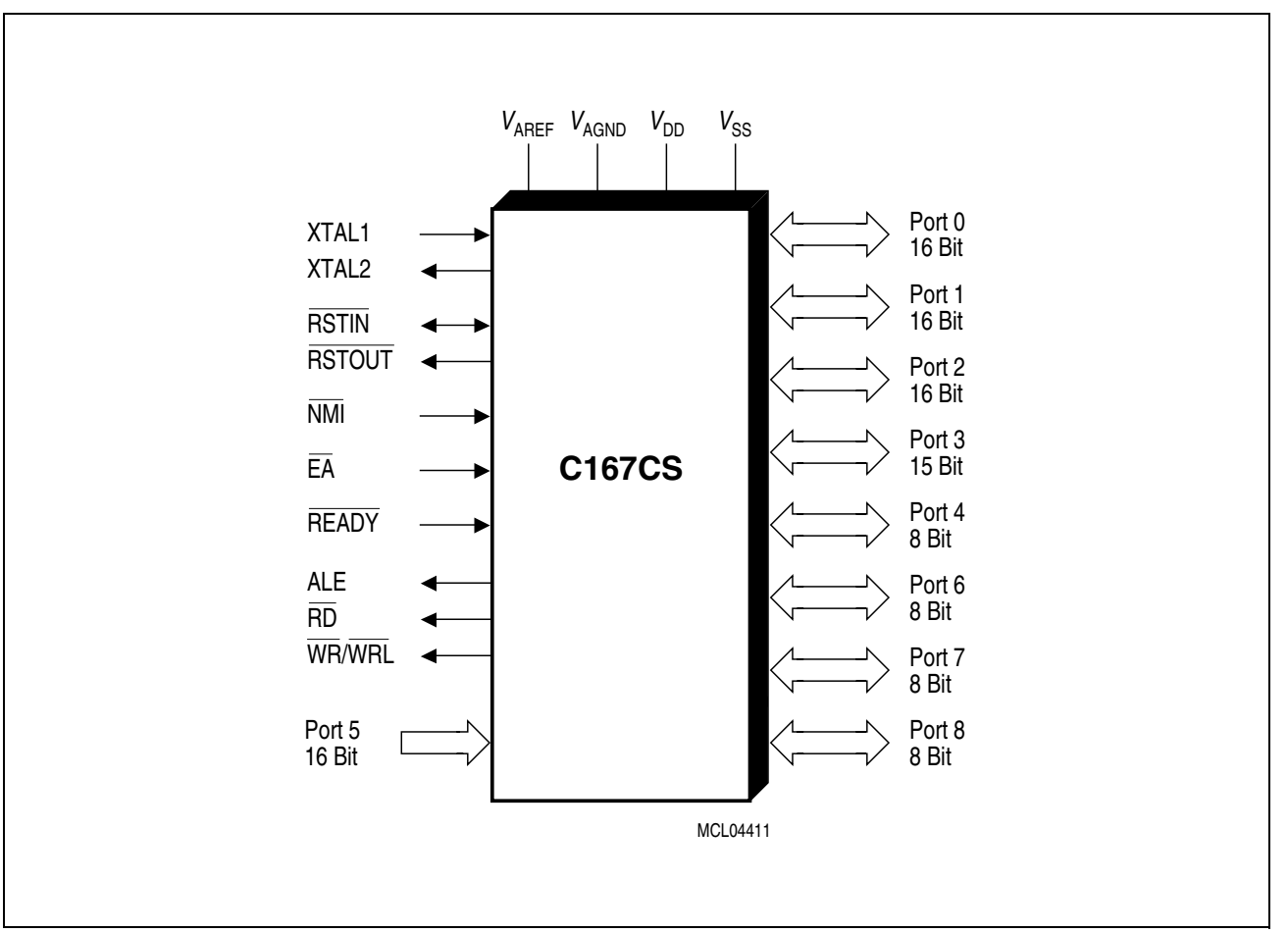


Figure 1 Logic Symbol

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Note: When one or both of the on-chip CAN Modules are used with the interface lines assigned to Port 4, the CAN lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 ... A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CS's instructions can be executed in just one machine cycle which requires 50 ns at 40 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

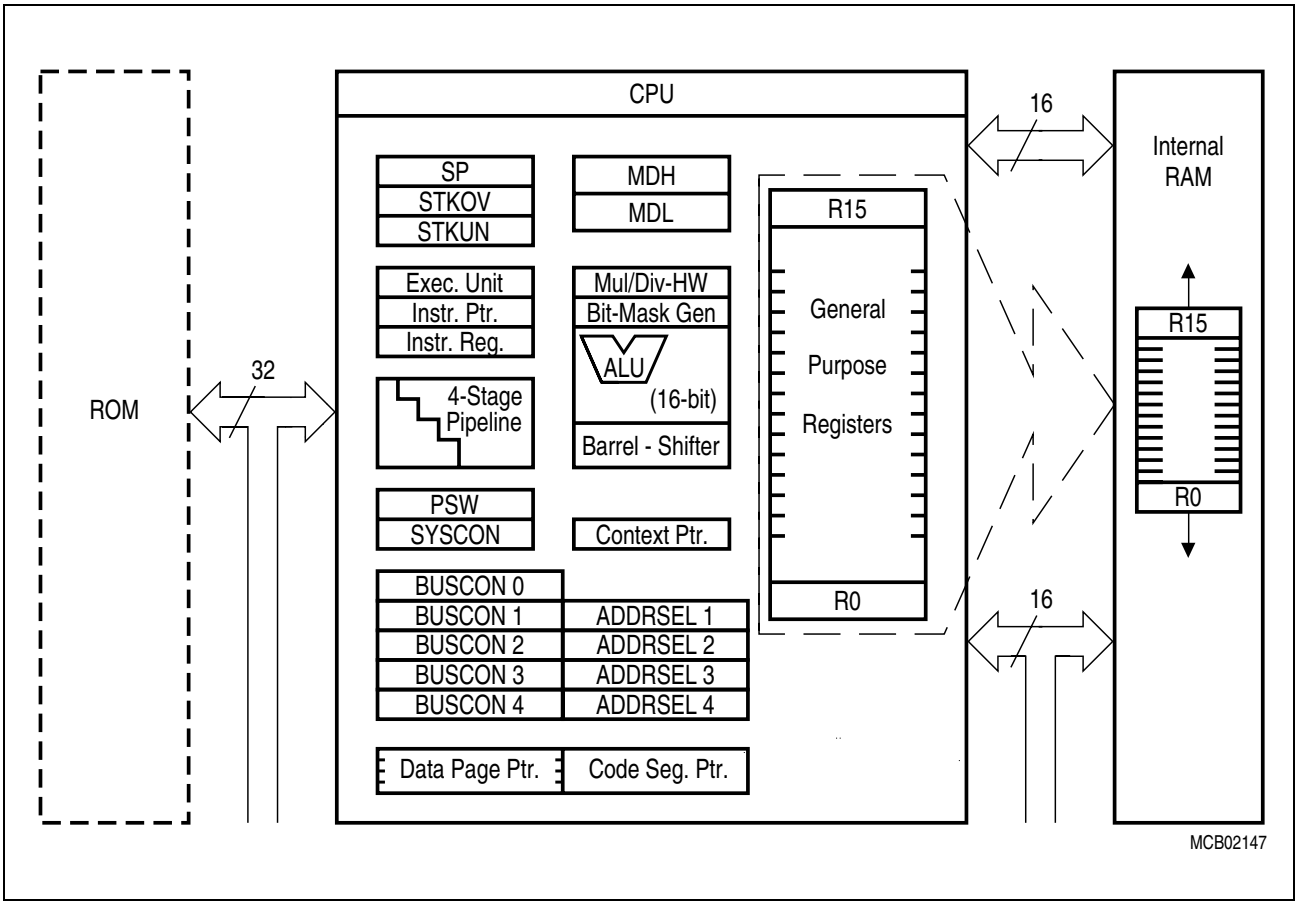


Figure 4 CPU Block Diagram

Table 3 C167CS Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	$00'0114_H$	45_H
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	$00'0118_H$	46_H
CAPCOM Timer 0	T0IR	T0IE	T0INT	$00'0080_H$	20_H
CAPCOM Timer 1	T1IR	T1IE	T1INT	$00'0084_H$	21_H
CAPCOM Timer 7	T7IR	T7IE	T7INT	$00'00F4_H$	$3D_H$
CAPCOM Timer 8	T8IR	T8IE	T8INT	$00'00F8_H$	$3E_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	$00'009C_H$	27_H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	$00'00A0_H$	28_H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	$00'00A4_H$	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
PWM Channel 0 … 3	PWMIR	PWMIE	PWMINT	$00'00FC_H$	$3F_H$
CAN Interface 1	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
CAN Interface 2	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
Unassigned node	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
PLL/OWD and RTC	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H

The C167CS also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	 RESET RESET RESET	 $00'0000_H$ $00'0000_H$ $00'0000_H$	 00_H 00_H 00_H	 III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 $00'0008_H$ $00'0010_H$ $00'0018_H$	 02_H 04_H 06_H	 II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	 UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP	 $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$	 $0A_H$ $0A_H$ $0A_H$ $0A_H$ $0A_H$	 I I I I I
Reserved	–	–	$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	–
Software Traps – TRAP Instruction	–	–	Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 24 multiplexed input channels (16 standard channels and 8 extension channels) and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 24 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CS supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels (standard or extension) are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via registers P5DIDIS (Port 5 Digital Input Disable) and P1DIDIS (PORT1 Digital Input Disable).

Parallel Ports

The C167CS provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.
Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.
Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output CLKOUT (or the programmable frequency output FOUT).
Port 5 (and parts of PORT1) is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) and driver characteristics (output current) of the C167CS's port drivers can be selected via the Port Output Control registers (POCONx).

Special Function Registers Overview

Table 7 lists all SFRs which are implemented in the C167CS in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 7 C167CS Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	---	CAN1 Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	---	CAN1 Control/Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	---	CAN1 Global Mask Short	$UFUU_H$
C1PCIR	$EF02_H$ **X**	---	CAN1 Port Control/Interrupt Register	$XXXX_H$
C1LGML	$EF0A_H$ **X**	---	CAN1 Lower Global Mask Long	$UUUU_H$
C1LMLM	$EF0E_H$ **X**	---	CAN1 Lower Mask of Last Message	$UUUU_H$

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
C1UAR	$EFn2_H$ **X**	---	CAN1 Upper Arbitration Reg. (msg. **n**)	$UUUU_H$
C1UGML	$EF08_H$ **X**	---	CAN1 Upper Global Mask Long	$UUUU_H$
C1UMLM	$EF0C_H$ **X**	---	CAN1 Upper Mask of Last Message	$UUUU_H$
C2BTR	$EE04_H$ **X**	---	CAN2 Bit Timing Register	$UUUU_H$
C2CSR	$EE00_H$ **X**	---	CAN2 Control/Status Register	$XX01_H$
C2GMS	$EE06_H$ **X**	---	CAN2 Global Mask Short	$UFUU_H$
C2PCIR	$EE02_H$ **X**	---	CAN2 Port Control/Interrupt Register	$XXXX_H$
C2LGML	$EE0A_H$ **X**	---	CAN2 Lower Global Mask Long	$UUUU_H$
C2LMLM	$EE0E_H$ **X**	---	CAN2 Lower Mask of Last Message	$UUUU_H$
C2UAR	$EEn2_H$ **X**	---	CAN2 Upper Arbitration Reg. (msg. **n**)	$UUUU_H$
C2UGML	$EE08_H$ **X**	---	CAN2 Upper Global Mask Long	$UUUU_H$
C2UMLM	$EE0C_H$ **X**	---	CAN2 Upper Mask of Last Message	$UUUU_H$
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC0	$FE80_H$	40_H	CAPCOM Register 0	0000_H
CC0IC **b**	$FF78_H$	BC_H	CAPCOM Reg. 0 Interrupt Ctrl. Reg.	0000_H
CC1	$FE82_H$	41_H	CAPCOM Register 1	0000_H
CC10	$FE94_H$	$4A_H$	CAPCOM Register 10	0000_H
CC10IC **b**	$FF8C_H$	$C6_H$	CAPCOM Reg. 10 Interrupt Ctrl. Reg.	0000_H
CC11	$FE96_H$	$4B_H$	CAPCOM Register 11	0000_H
CC11IC **b**	$FF8E_H$	$C7_H$	CAPCOM Reg. 11 Interrupt Ctrl. Reg.	0000_H
CC12	$FE98_H$	$4C_H$	CAPCOM Register 12	0000_H
CC12IC **b**	$FF90_H$	$C8_H$	CAPCOM Reg. 12 Interrupt Ctrl. Reg.	0000_H
CC13	$FE9A_H$	$4D_H$	CAPCOM Register 13	0000_H
CC13IC **b**	$FF92_H$	$C9_H$	CAPCOM Reg. 13 Interrupt Ctrl. Reg.	0000_H
CC14	$FE9C_H$	$4E_H$	CAPCOM Register 14	0000_H
CC14IC **b**	$FF94_H$	CA_H	CAPCOM Reg. 14 Interrupt Ctrl. Reg.	0000_H
CC15	$FE9E_H$	$4F_H$	CAPCOM Register 15	0000_H
CC15IC **b**	$FF96_H$	CB_H	CAPCOM Reg. 15 Interrupt Ctrl. Reg.	0000_H
CC16	$FE60_H$	30_H	CAPCOM Register 16	0000_H
CC16IC **b**	$F160_H$ **E**	$B0_H$	CAPCOM Reg. 16 Interrupt Ctrl. Reg.	0000_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
DP1L b	$F104_H$ E	82_H	P1L Direction Control Register	00_H
DP1H b	$F106_H$ E	83_H	P1H Direction Control Register	00_H
DP2 b	$FFC2_H$	$E1_H$	Port 2 Direction Control Register	0000_H
DP3 b	$FFC6_H$	$E3_H$	Port 3 Direction Control Register	0000_H
DP4 b	$FFCA_H$	$E5_H$	Port 4 Direction Control Register	00_H
DP6 b	$FFCE_H$	$E7_H$	Port 6 Direction Control Register	00_H
DP7 b	$FFD2_H$	$E9_H$	Port 7 Direction Control Register	00_H
DP8 b	$FFD6_H$	EB_H	Port 8 Direction Control Register	00_H
DPP0	$FE00_H$	00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1	$FE02_H$	01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2	$FE04_H$	02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3	$FE06_H$	03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON b	$F1C0_H$ E	$E0_H$	External Interrupt Control Register	0000_H
EXISEL b	$F1DA_H$ E	ED_H	External Interrupt Source Select Reg.	0000_H
FOCON b	$FFAA_H$	$D5_H$	Frequency Output Control Register	0000_H
IDCHIP	$F07C_H$ E	$3E_H$	Identifier	$0CXX_H$
IDMANUF	$F07E_H$ E	$3F_H$	Identifier	1820_H
IDMEM	$F07A_H$ E	$3D_H$	Identifier	$X040_H$
IDMEM2	$F076_H$ E	$3B_H$	Identifier	$XXXX_H$
IDPROG	$F078_H$ E	$3C_H$	Identifier	$XXXX_H$
ISNC b	$F1DE_H$ E	EF_H	Interrupt Subnode Control Register	0000_H
MDC b	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 b	$F1C2_H$ E	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 b	$F1C6_H$ E	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4 b	$F1CA_H$ E	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP6 b	$F1CE_H$ E	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7 b	$F1D2_H$ E	$E9_H$	Port 7 Open Drain Control Register	00_H
ODP8 b	$F1D6_H$ E	EB_H	Port 8 Open Drain Control Register	00_H

Table 7 C167CS Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
T14		$F0D2_H$	**E**	69_H	RTC Timer 14 Register	$XXXX_H$
T14REL		$F0D0_H$	**E**	68_H	RTC Timer 14 Reload Register	$XXXX_H$
T2		$FE40_H$		20_H	GPT1 Timer 2 Register	0000_H
T2CON	**b**	$FF40_H$		$A0_H$	GPT1 Timer 2 Control Register	0000_H
T2IC	**b**	$FF60_H$		$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3		$FE42_H$		21_H	GPT1 Timer 3 Register	0000_H
T3CON	**b**	$FF42_H$		$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC	**b**	$FF62_H$		$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4		$FE44_H$		22_H	GPT1 Timer 4 Register	0000_H
T4CON	**b**	$FF44_H$		$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC	**b**	$FF64_H$		$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5		$FE46_H$		23_H	GPT2 Timer 5 Register	0000_H
T5CON	**b**	$FF46_H$		$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC	**b**	$FF66_H$		$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6		$FE48_H$		24_H	GPT2 Timer 6 Register	0000_H
T6CON	**b**	$FF48_H$		$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC	**b**	$FF68_H$		$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
T7		$F050_H$	**E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON	**b**	$FF20_H$		90_H	CAPCOM Timer 7 and 8 Control Reg.	0000_H
T7IC	**b**	$F17A_H$	**E**	BE_H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000_H
T7REL		$F054_H$	**E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H
T8		$F052_H$	**E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC	**b**	$F17C_H$	**E**	BF_H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000_H
T8REL		$F056_H$	**E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR	**b**	$FFAC_H$		$D6_H$	Trap Flag Register	0000_H
WDT		$FEAE_H$		57_H	Watchdog Timer Register (read only)	0000_H
WDTCON	**b**	$FFAE_H$		$D7_H$	Watchdog Timer Control Register	[2] $00XX_H$
XP0IC	**b**	$F186_H$	**E**	$C3_H$	CAN1 Module Interrupt Control Register	0000_H
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	CAN2 Module Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Unassigned Interrupt Control Register	0000_H

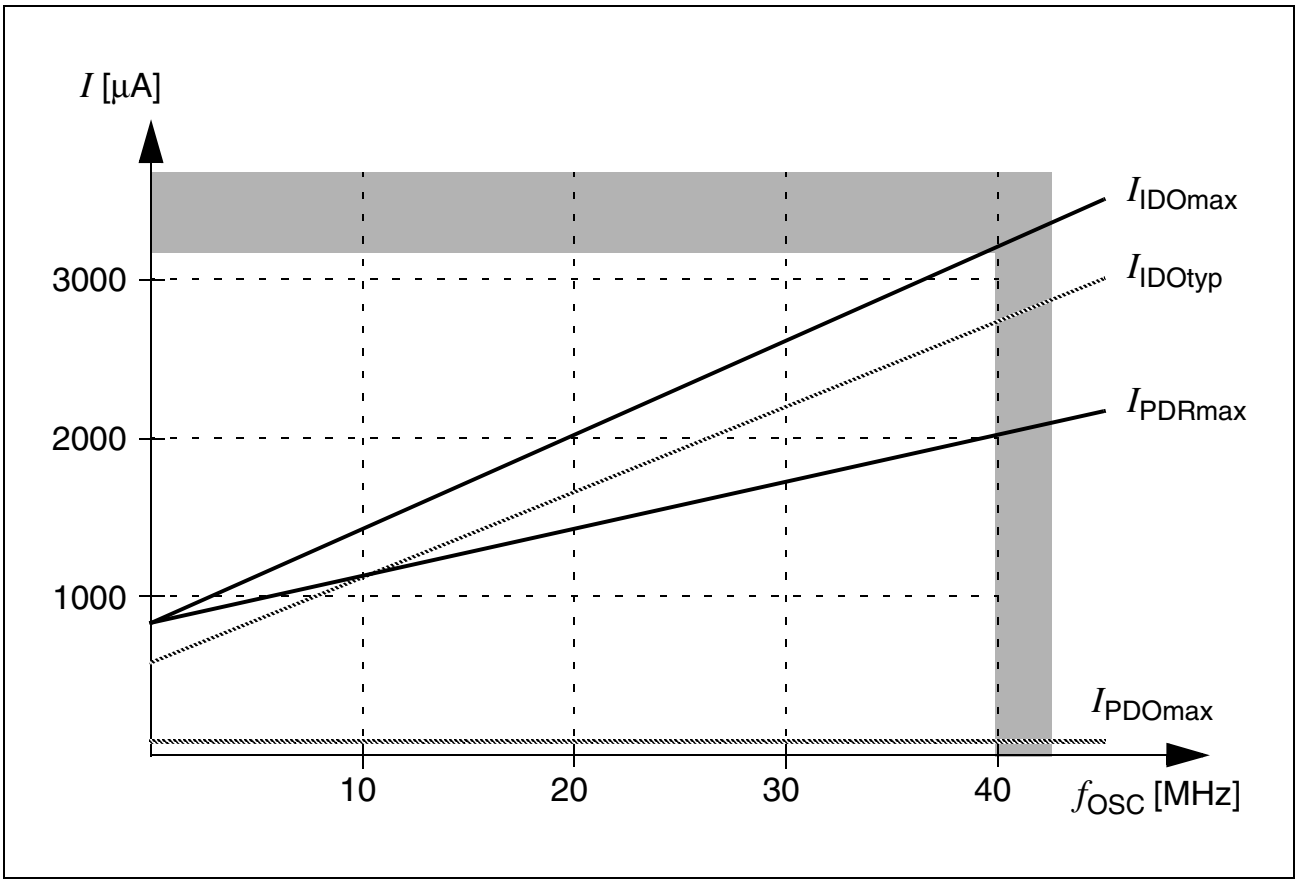


Figure 9 **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

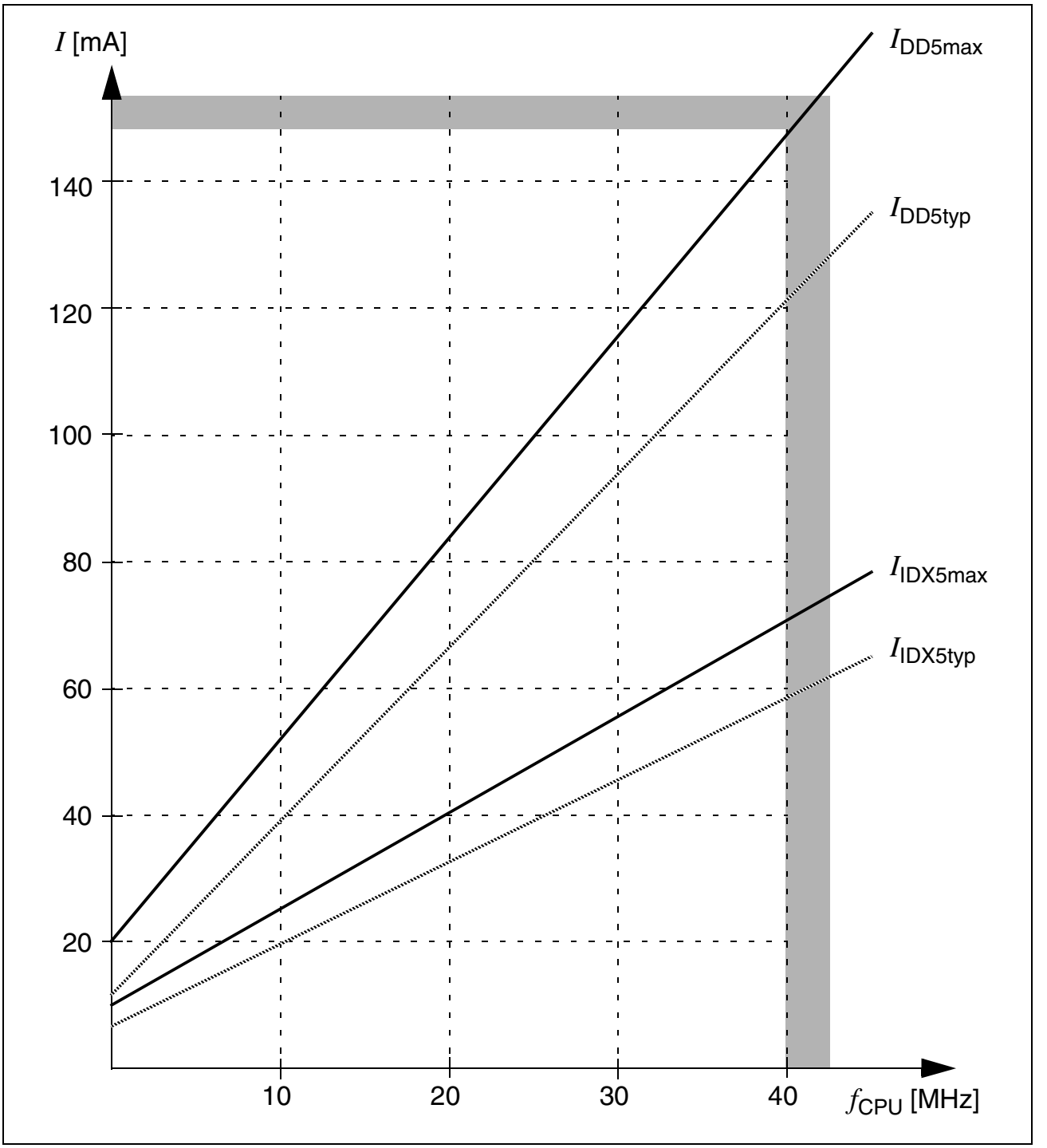


Figure 10 Supply/Idle Current as a Function of Operating Frequency

P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 11 associates the combinations of these three bits with the respective clock generation mode.

Table 11 C167CS Clock Generation Modes

CLKCFG (RP0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[1)]	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 10 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 13.33 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 20 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 8 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 40 MHz	Direct drive[2)]
0 1 0	$f_{OSC} \times 1.5$	6.66 to 26.66 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 50 MHz[3)]	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 16 MHz	–

1) The external clock input range refers to a CPU clock range of 10 … 40 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

3) In prescaler mode the full CPU clock range cannot be used.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see **Table 11**). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times$ **F**). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

AC Characteristics
External Clock Drive XTAL1
(Operating Conditions apply)

Table 12 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	25	–	20	–	37[1]	500[1]	ns
High time[2]	t_1	SR	12[3]	–	5	–	10	–	ns
Low time[2]	t_2	SR	12[3]	–	5	–	10	–	ns
Rise time[2]	t_3	SR	–	8	–	5	–	10	ns
Fall time[2]	t_4	SR	–	8	–	5	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

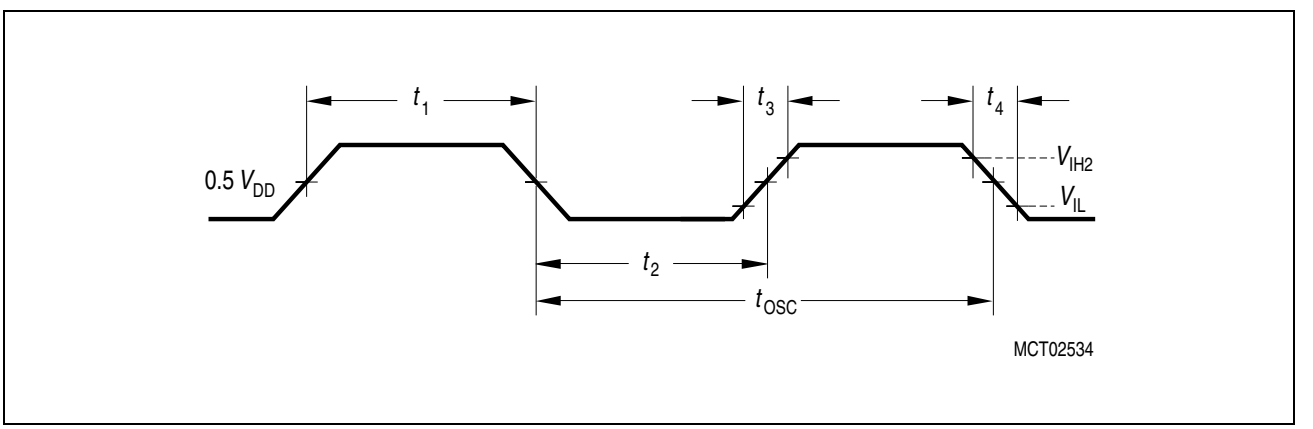


Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

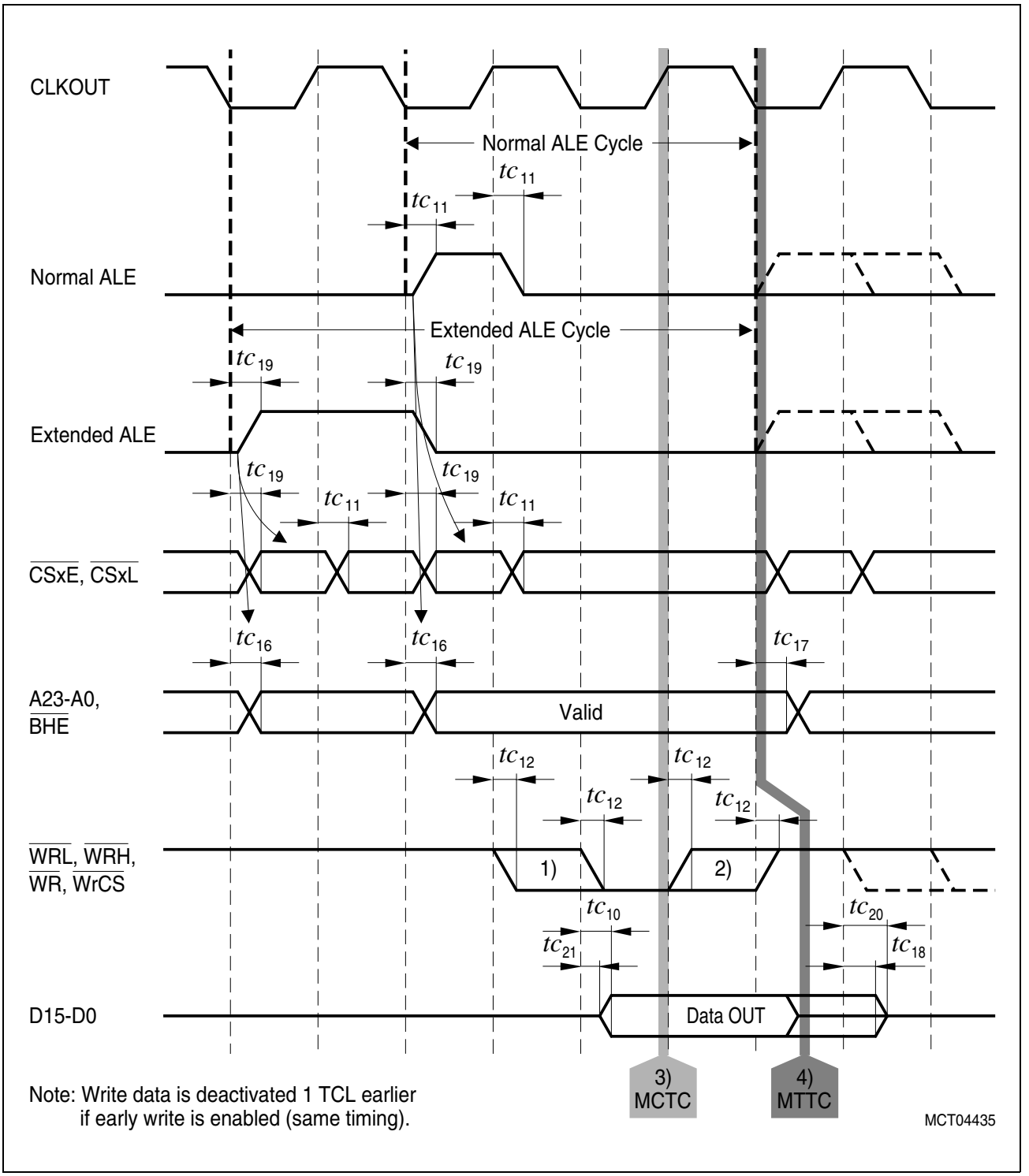
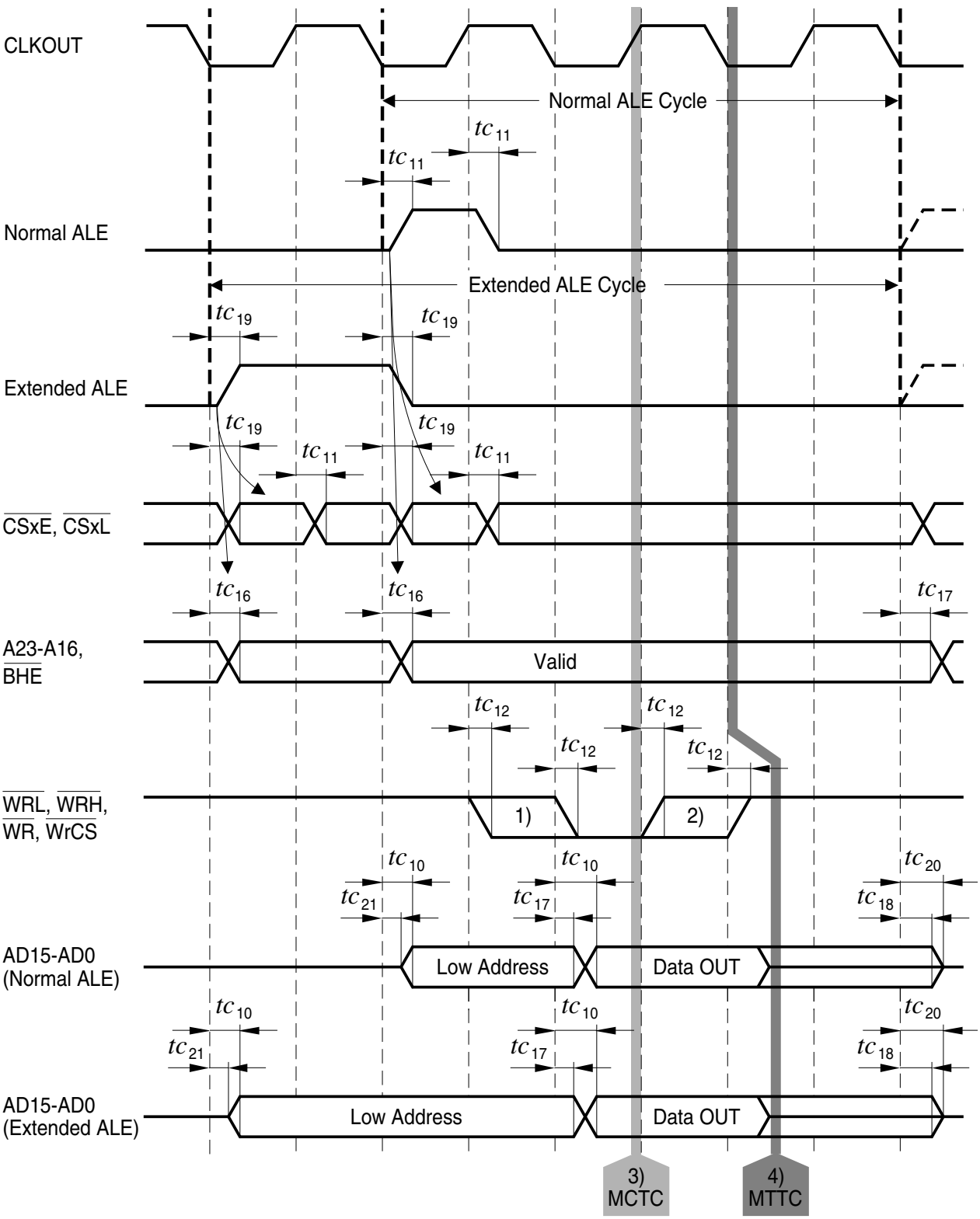


Figure 17 Demultiplexed Bus, Write Access



Note: Write data is deactivated 2 TCL earlier if early write is enabled (same timing).

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Figure 19 Multiplexed Bus, Write Access

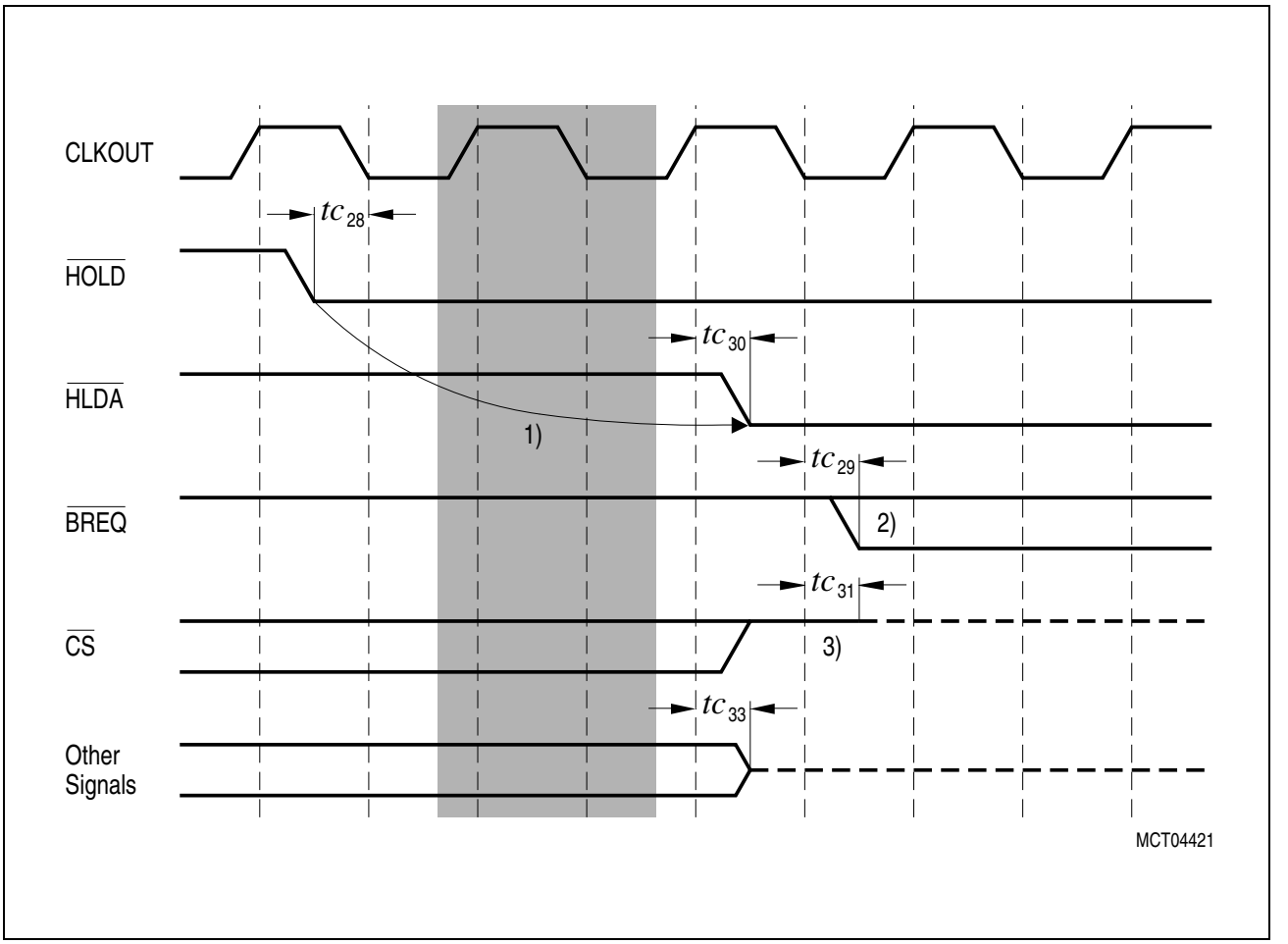

Figure 22 External Bus Arbitration, Releasing the Bus

Notes
1) The C167CS will complete the currently running bus cycle before granting bus access.
2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{33}. Latched $\overline{\text{CS}}$ outputs are driven high for 1 TCL before the output drivers are switched off.