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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc811m001fdh16fp

- Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- CRC engine.
- Windowed Watchdog timer (WWDT).

- Analog peripherals:
  - Comparator with external voltage reference with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
  - Three USART interfaces with pin functions assigned through the switch matrix.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I2C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Available as SO20 package, TSSOP20 package, TSSOP16, and DIP8 package.

3. Applications

- 8/16-bit applications
- Consumer
- Climate control
- Lighting
- Motor control
- Fire and security applications

6. Pinning information

6.1 Pinning

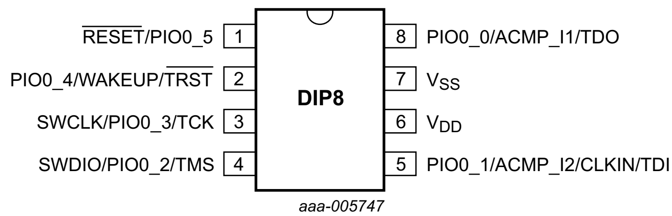


Fig 2. Pin configuration DIP8 package (LPC810M021FN8)

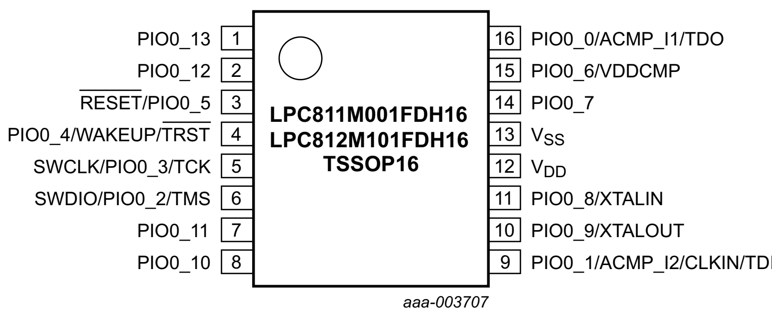


Fig 3. Pin configuration TSSOP16 package

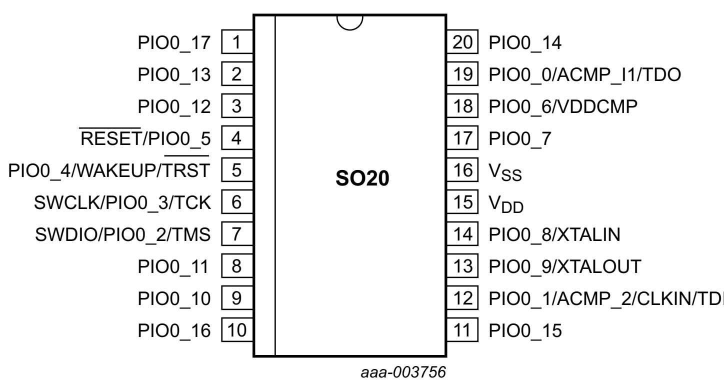


Fig 4. Pin configuration SO20 package (LPC812M101FD20)

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 9 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 7.9 for details.

7.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

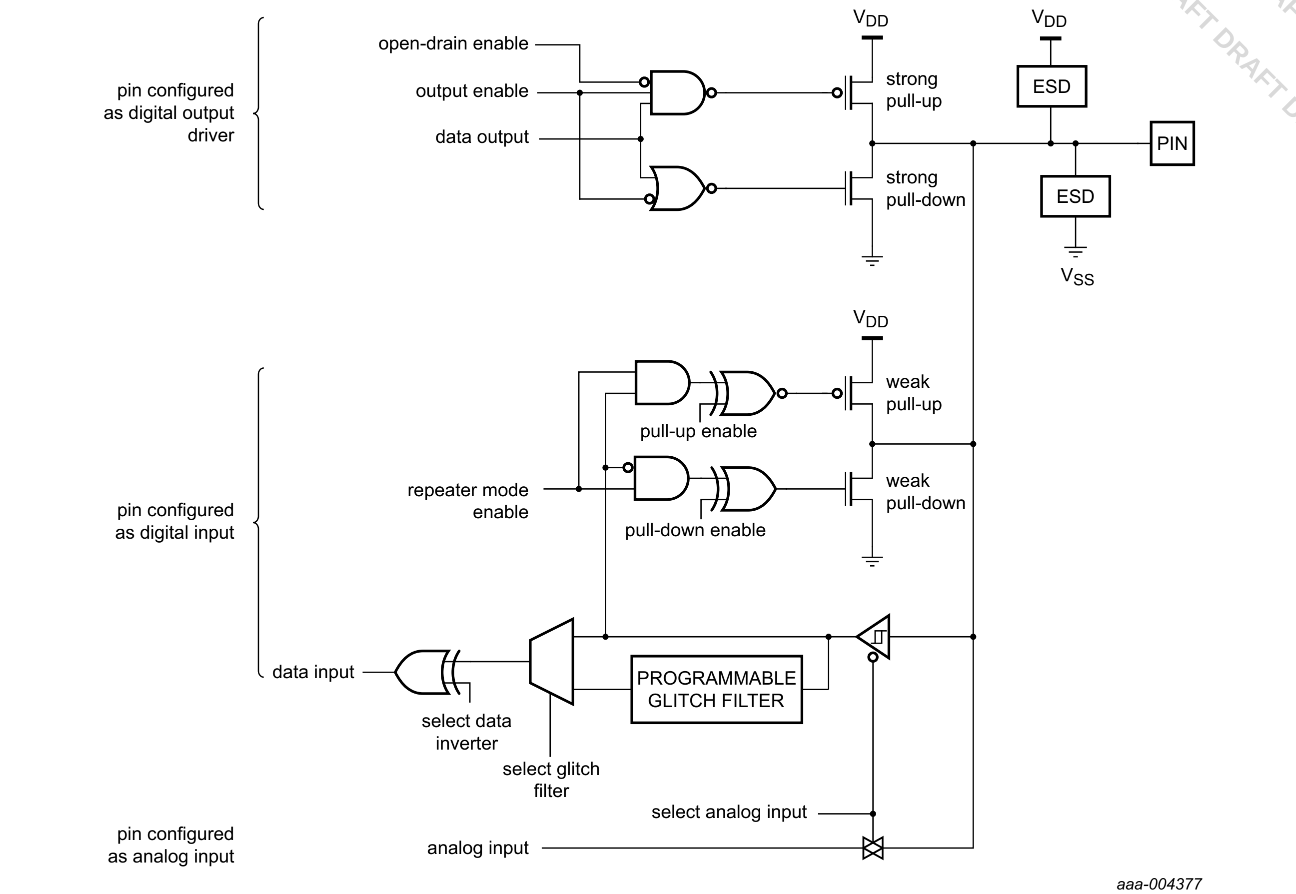


Fig 7. Standard I/O pad configuration

7.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

7.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing.

7.13.1 Features

- Maximum data rates of 30 Mbit/s in slave and master mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see Ref. 1).

7.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.
- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:
  - Fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C-bus are floating and do not disturb the bus.
  - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

7.15 State-Configurable Timer (SCT)

The state configurable timer can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCT can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

All inputs and outputs of the SCT are movable functions and are assigned to pins through the switch matrix.

7.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
  – Match register 0 can be used as an automatic limit.
  – In bi-directional mode, events can be enabled based on the count direction.
  – Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  – 4 inputs
  – 4 outputs
  – 5 match/capture registers
  – 6 events
  – 2 states

7.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.16.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

7.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

7.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{RESET}$ pin selects between the JTAG boundary scan ($\overline{RESET}$ = LOW) and the ARM SWD debug ($\overline{RESET}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{RESET}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{RESET}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{TRST}$ pin to enable the SWD debug mode, and release the $\overline{RESET}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[3]	–0.5	+5.5	V
		5 V open-drain pins PIO0_10 and PIO0_11	[4]	–0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[5]	–0.5	+3.6	V
V_{IA}	analog input voltage		[6] [7]	–0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	–0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[8]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	<tbd>	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	-	<tbd>	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

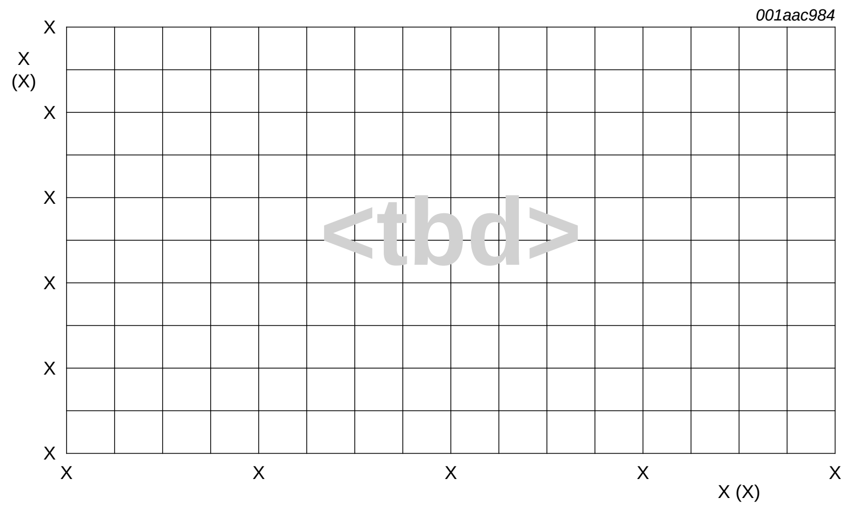
[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I²C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] V_{DD} present or not present.

[6] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.



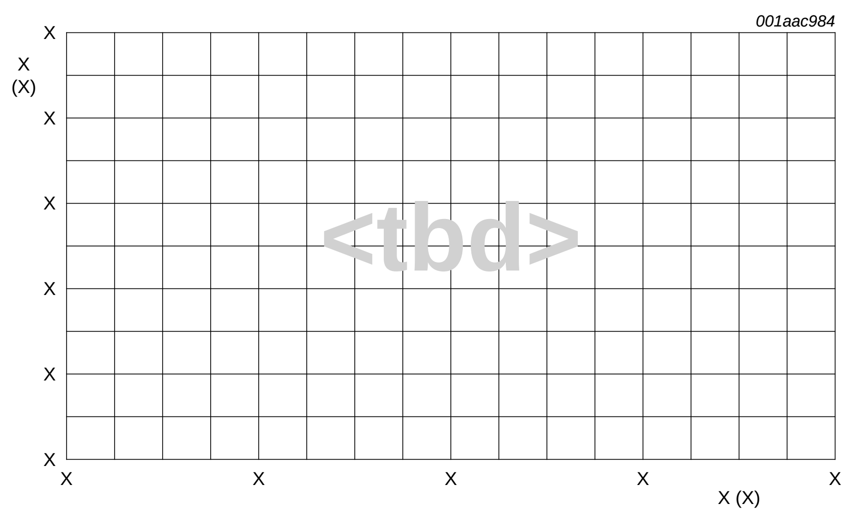
Conditions: V_{DD} = 3.3 V; active mode entered executing code while(1){} from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

3 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz - 30 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 13. Active mode: Typical supply current I_{DD} versus temperature



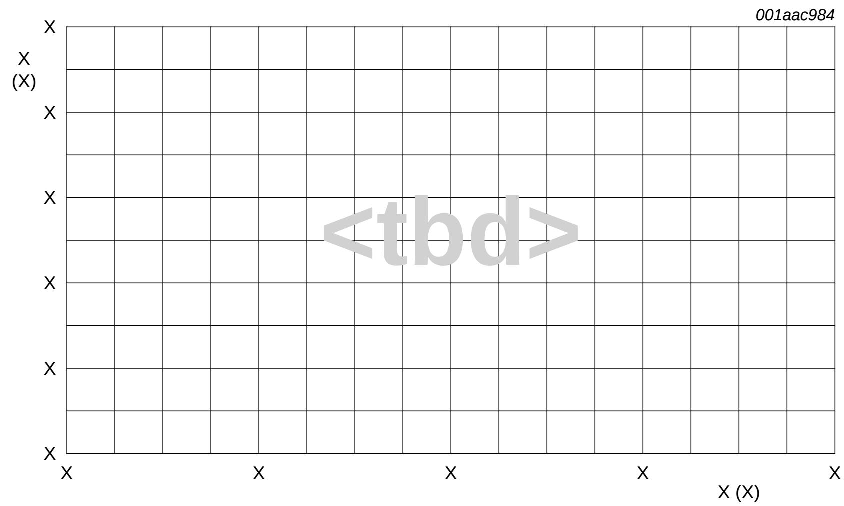
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

3 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

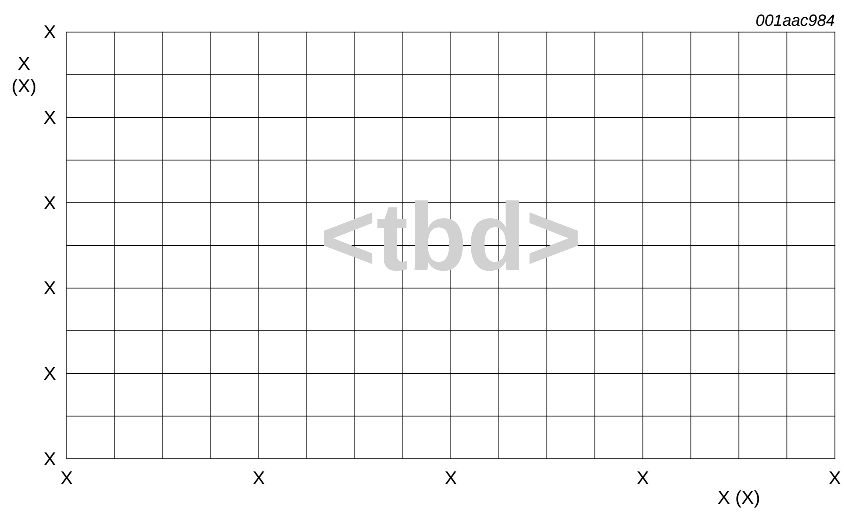
24 MHz - 30 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 14. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



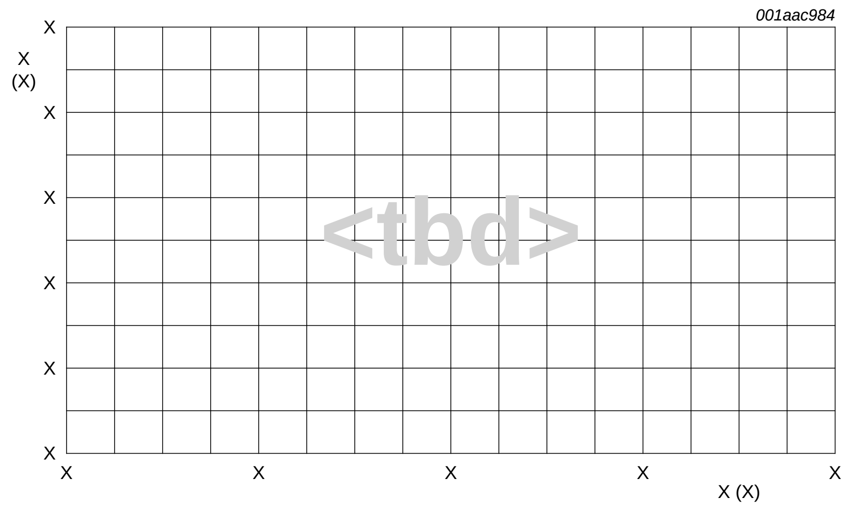
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

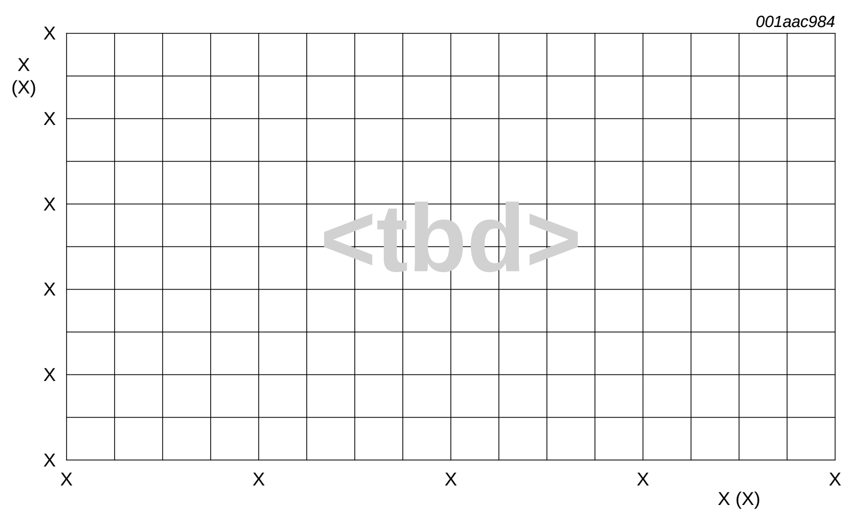


(1) WKT running.

(1) WKT not running.

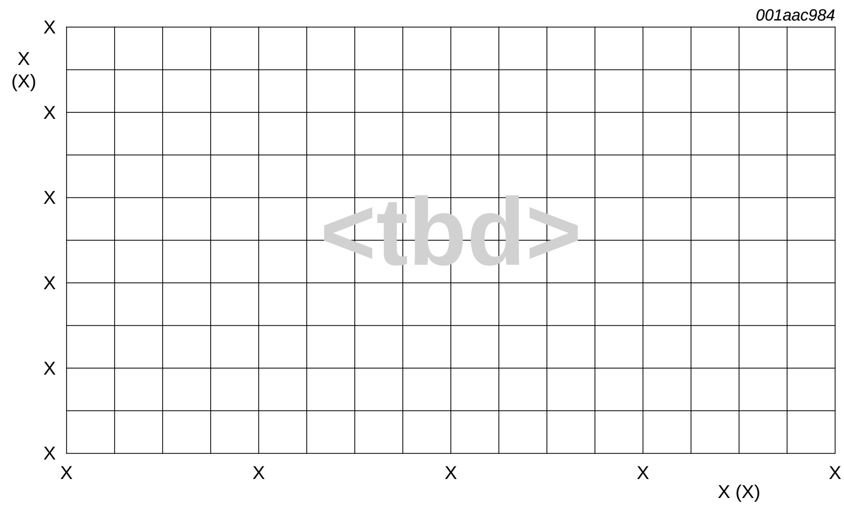
Fig 17. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

10.2 CoreMark data



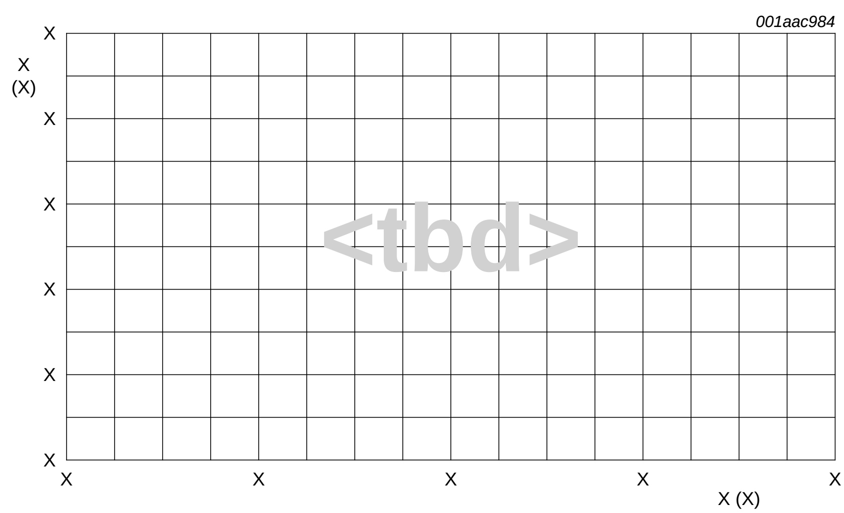
External signal generator providing 1 MHz to 20 MHz signal drives the XTALIN input; when testing 1 MHz to 19 MHz the system PLL is OFF, SYSAHBCLKDIV = 1; when testing 20 MHz to 30 MHz the system PLL is configured so that SYSAHBCLKDIV = 1.

Fig 18. CoreMark current consumption for power modes 0, 1, 2, and 3



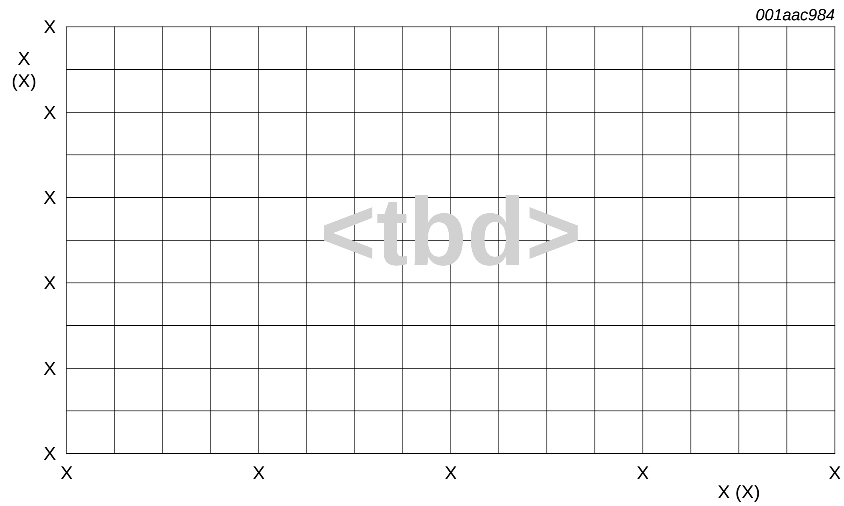
Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins and <tbd>.

Fig 21. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



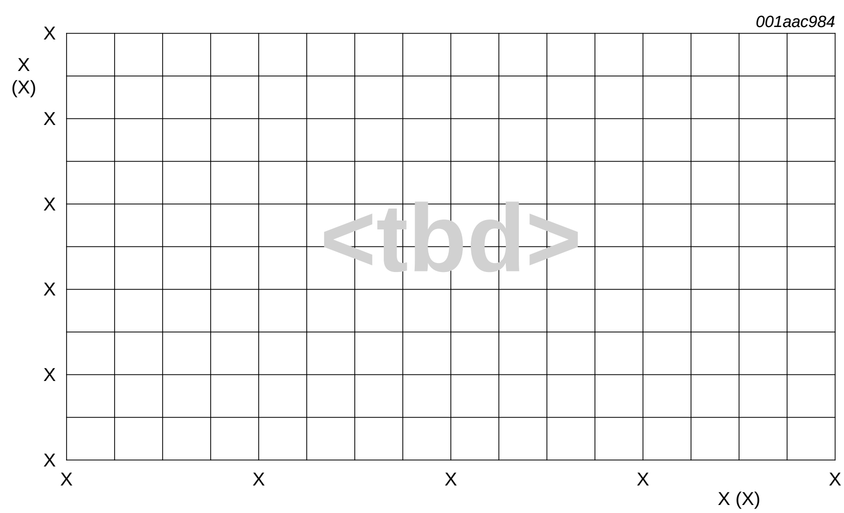
Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 22. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 23. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 24. Typical pull-down current I_{pd} versus input voltage V_I

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

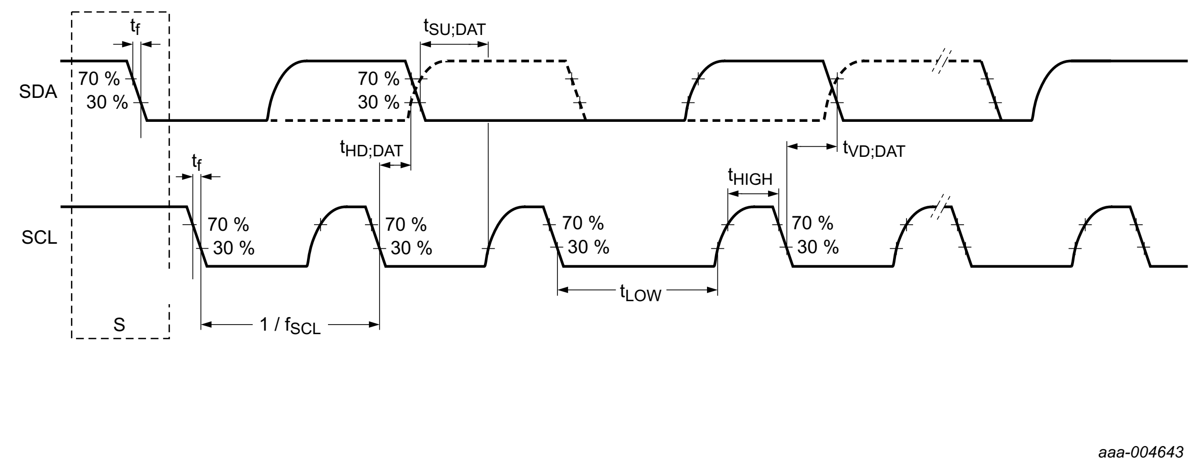


Fig 27. I^2C-bus pins clock timing

11.7 SPI interfaces

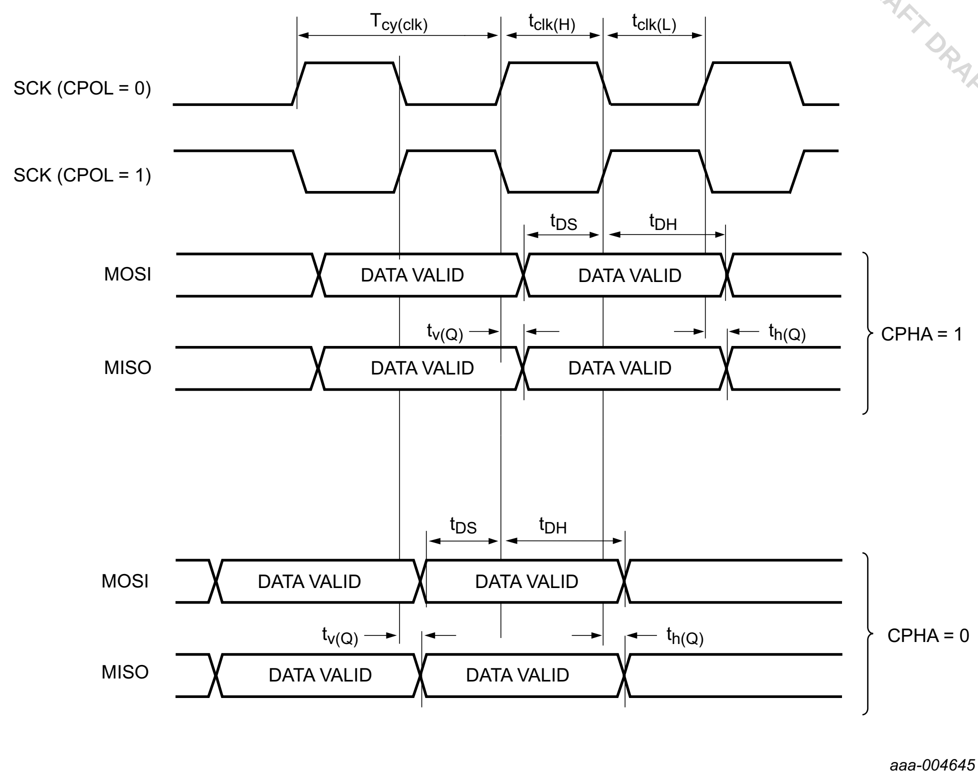
The maximum data bit rate is 30 Mbit/s in slave and master modes.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 18. Dynamic characteristics of SPI pins

T_{amb} = −40 °C to 85 °C; C_L = <tbd>; 1.8 V <= V_{DD} <= 3.6 V. Simulated parameters; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode [1]	<tbd>	-	-	ns
		when only transmitting [1]	<tbd>			ns
t_{DS}	data set-up time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	<tbd>	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V	<tbd>			ns
		1.8 V ≤ V_{DD} < 2.0 V	<tbd>	-	-	ns
t_{DH}	data hold time	in SPI mode	<tbd>	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	-	<tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	<tbd>	-	-	ns



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 29. SPI slave timing in SPI mode

11.8 USART interface

The maximum USART bit rate is 1.875 Mbit/s in asynchronous mode and 30 Mbit/s in synchronous mode slave and master mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 19. Dynamic characteristics: USART interface in synchronous master mode
T_{amb} = −40 °C to 85 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V; C_L = <tbd> pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pins Ux_SCLK	-	<tbd>	-	μs
output						
$t_{v(Q)}$	data output valid time	on pin Ux_TXD	-	<tbd>	-	ns

All information provided in this document is subject to legal disclaimers.

12. Analog characteristics

12.1 BOD

Table 20. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 0				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL.

12.2 POR

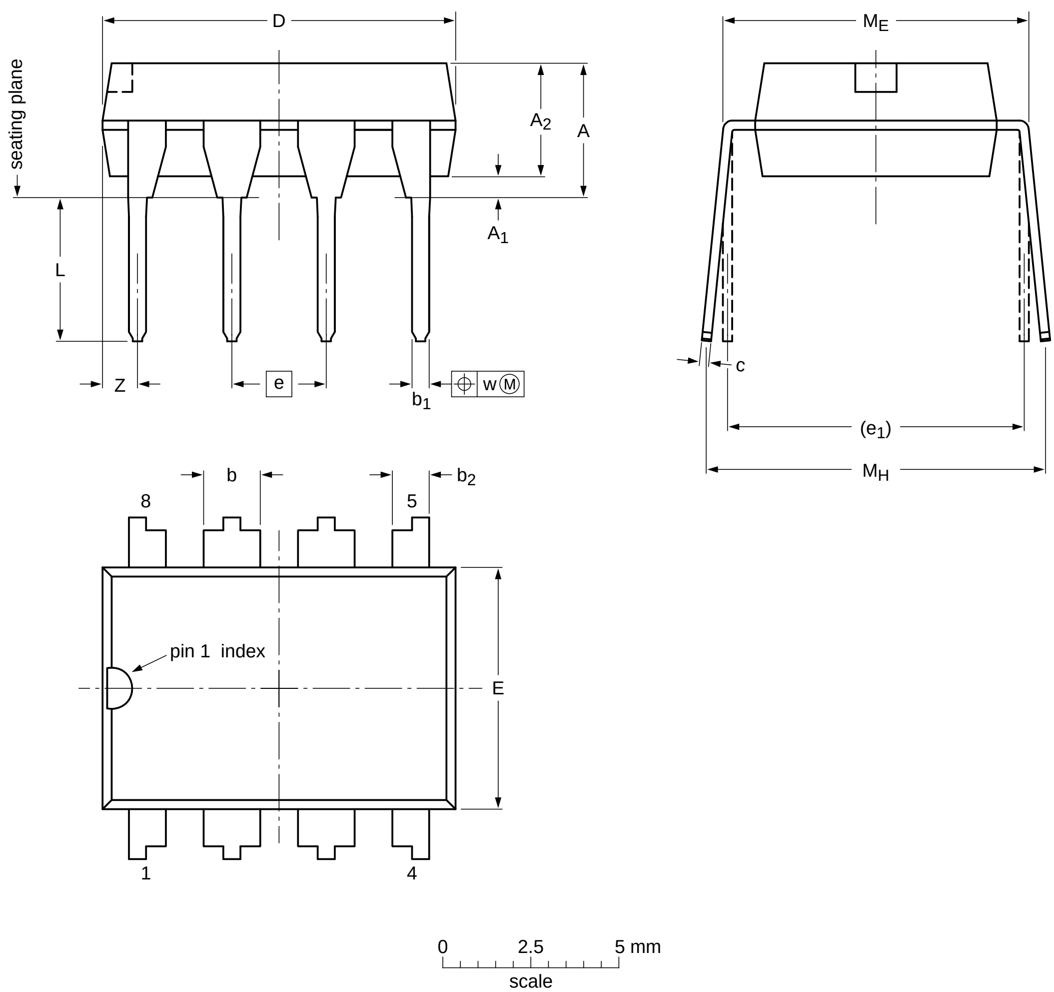
Table 21. POR static characteristics

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}		V_{DD} rising<tbd>				
		V_{DD} falling<tbd>	-	<tbd>	-	V

14. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit(1)		A	A_1	A_2	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1)
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

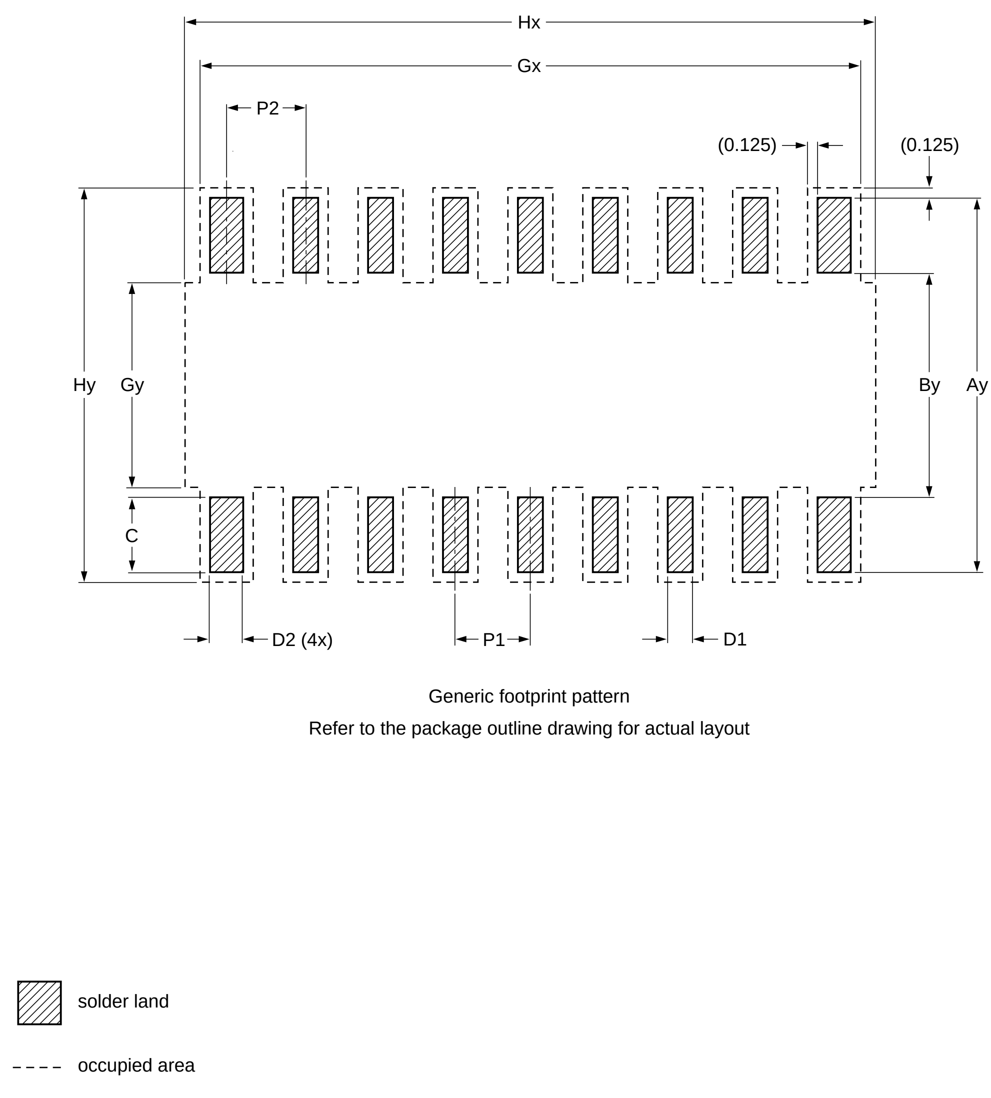
sot097-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 32. Package outline SOT097-2 (DIP8)

15. Soldering

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 36. Reflow soldering of the TSSOP16 package

16. Abbreviations

Table 28. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

17. References

[1] I2C-bus specification *UM10204*.

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