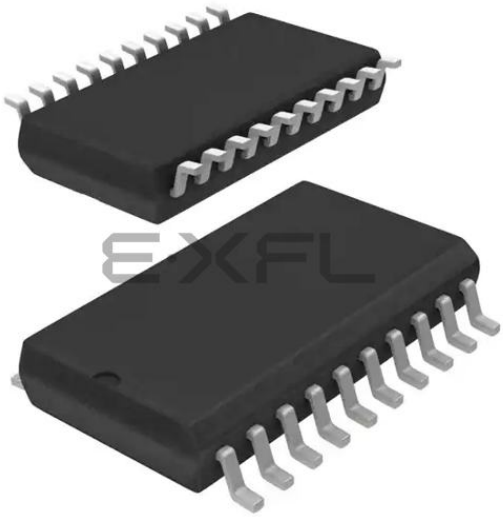

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101fd20fp

5. Block diagram

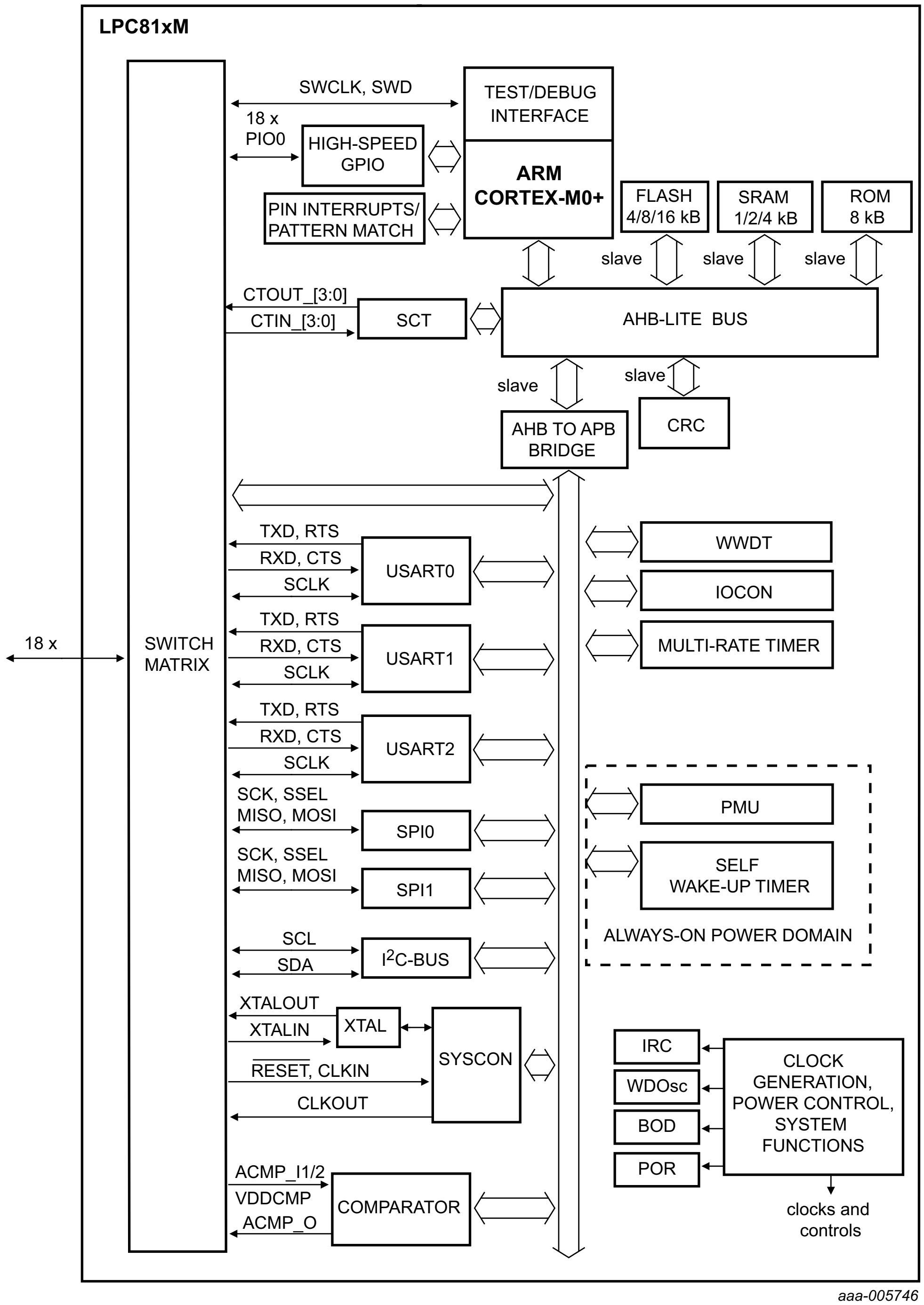


Fig 1. LPC81xM block diagram

Table 3. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	DIP8		Type	Reset state [1]	Description
PIO0_4/WAKEUP/ $\overline{\text{TRST}}$	5	4	2	[6]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally to enter Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
$\overline{\text{RESET}}$/PIO0_5	4	3	1	[4]	I/O	I; PU	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
					I	-	**PIO0_5 —** General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	-	[9]	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
					AI	-	**VDDCMP —** Alternate reference voltage for the analog comparator.
PIO0_7	17	14	-	[2]	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	-	[8]	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
					I	-	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	-	[8]	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
					O	-	**XTALOUT —** Output from the oscillator circuit.
PIO0_10	9	8	-	[3]	I	IA	**PIO0_10 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	-	[3]	I	IA	**PIO0_11 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_12	3	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin.
PIO0_13	2	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	7			-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART.

Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

7.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

7.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

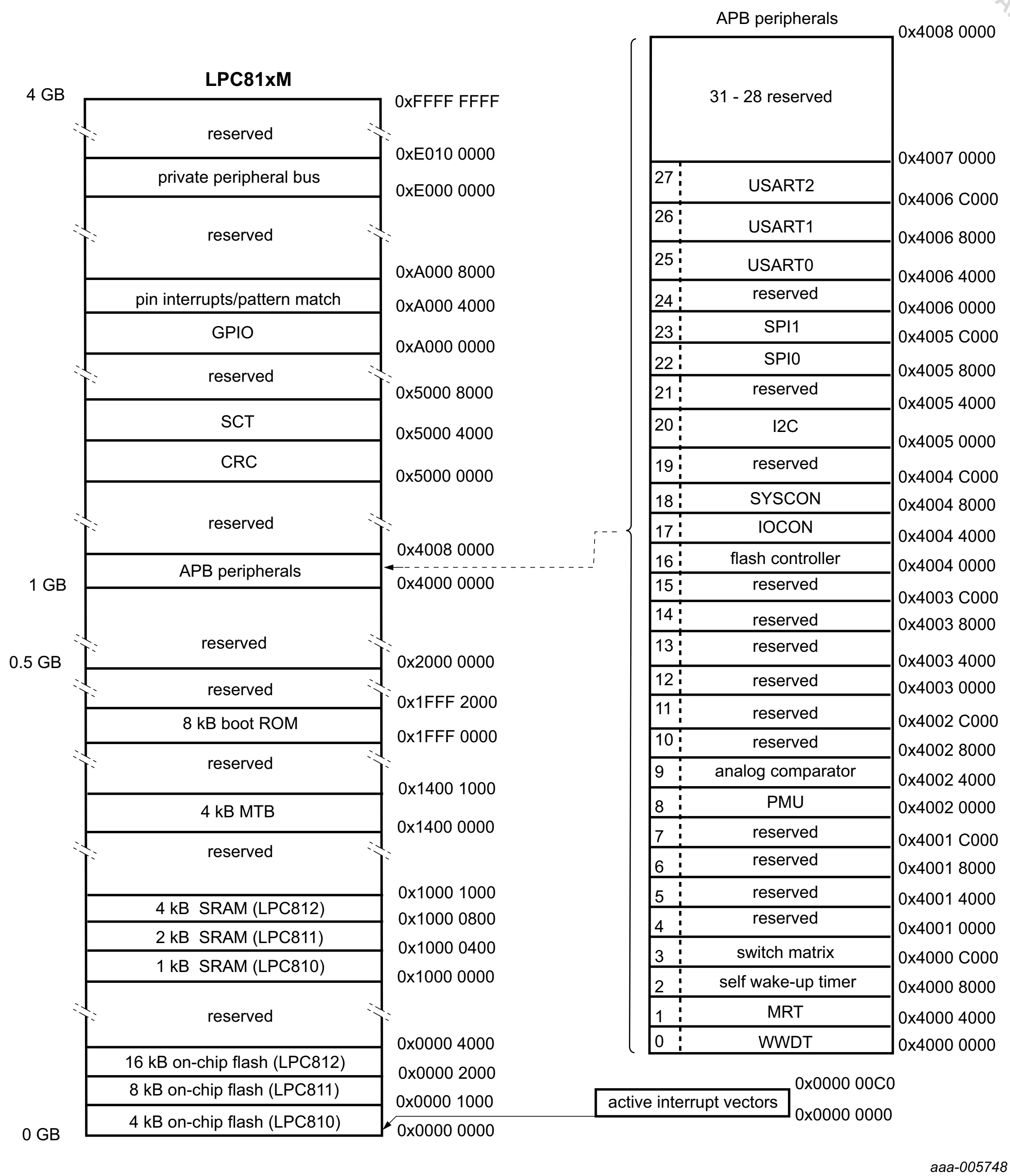


Fig 6. LPC81xM Memory map

7.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 3 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}.

7.13.1 Features

- Maximum data rates of 30 Mbit/s in slave and master mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14 I2C-bus interface

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see Ref. 1).

7.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^{2}C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^{2}C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.
- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:
  - Fail-safe operation: When the power to an I^{2}C-bus device is switched off, the SDA and SCL pins connected to the I^{2}C-bus are floating and do not disturb the bus.
  - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

7.15 State-Configurable Timer (SCT)

The state configurable timer can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCT can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

All inputs and outputs of the SCT are movable functions and are assigned to pins through the switch matrix.

7.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
  – Match register 0 can be used as an automatic limit.
  – In bi-directional mode, events can be enabled based on the count direction.
  – Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  – 4 inputs
  – 4 outputs
  – 5 match/capture registers
  – 6 events
  – 2 states

7.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.16.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

7.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

7.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources. One clock source originates from the always-on power domain.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

7.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

7.20 Clocking and power control

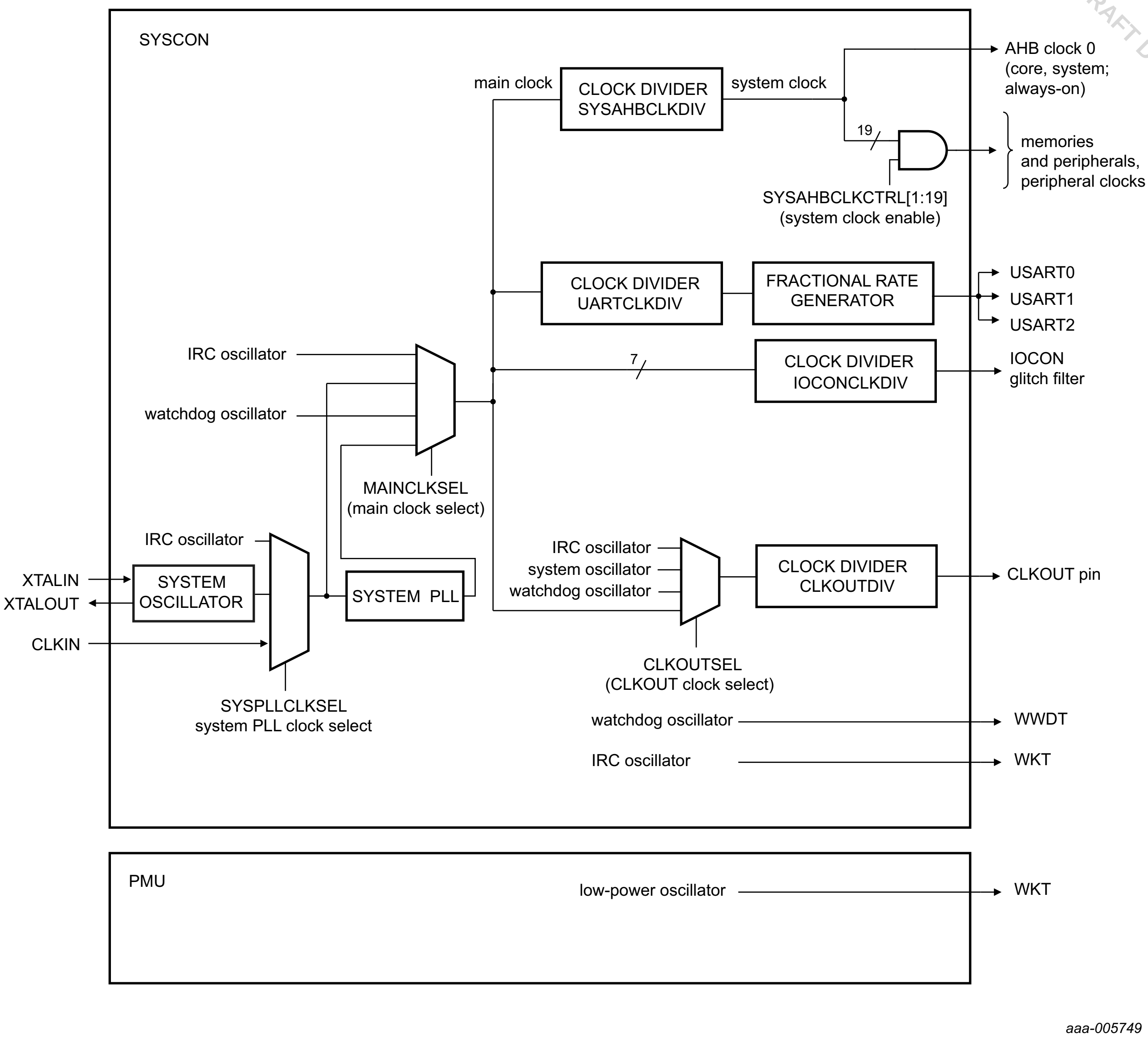


Fig 9. LPC81xM clock generation

7.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

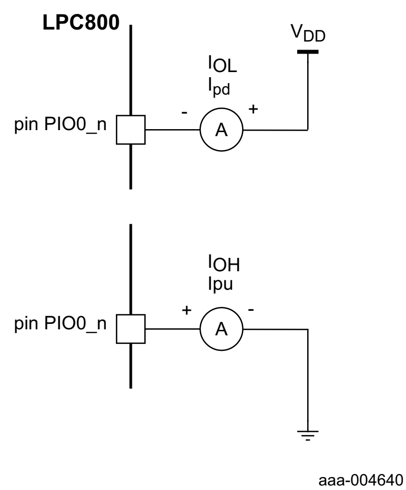
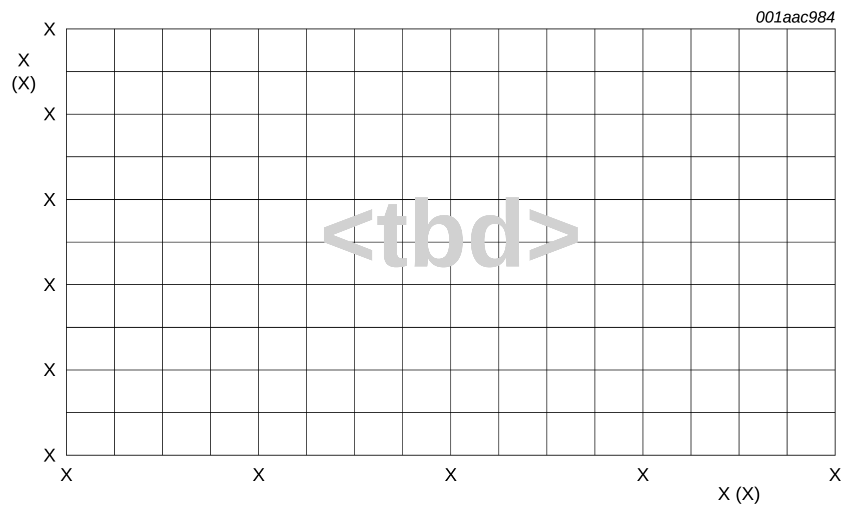


Fig 11. Pin input/output current measurement

10.1 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 0 to all GPIO DATA register to drive the outputs LOW.



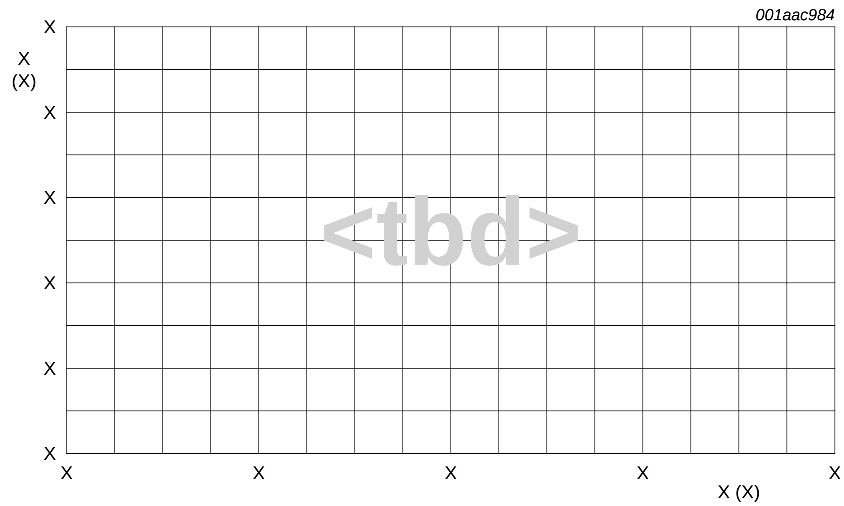
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = <tbd>); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

3 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

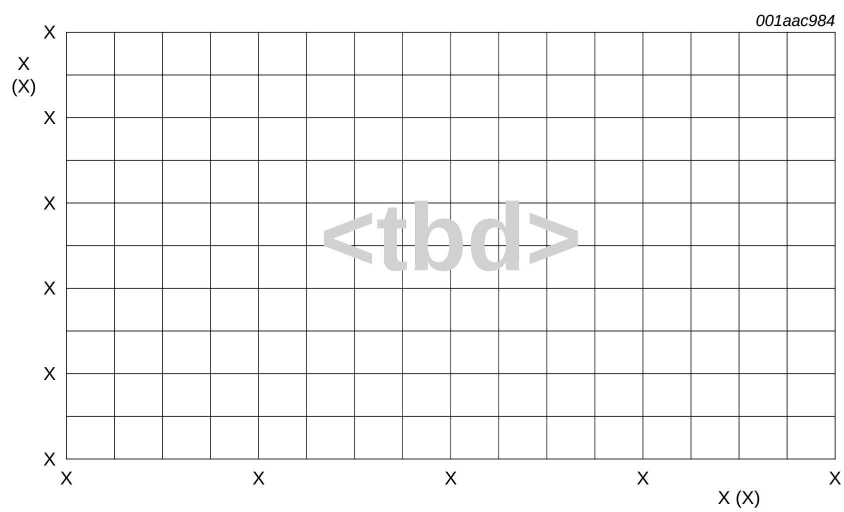
24 MHz - 30 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 12. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

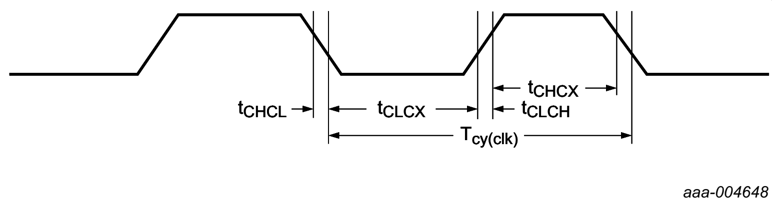


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

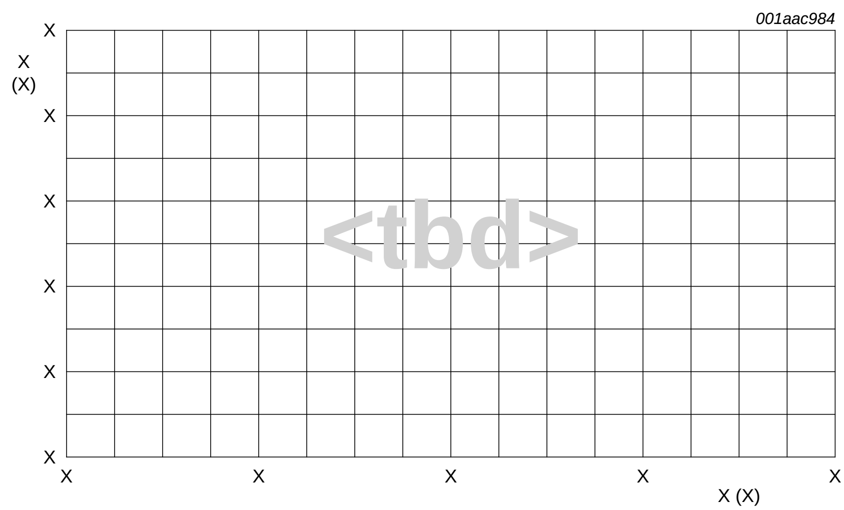
11.4 Internal oscillators

Table 13. Dynamic characteristic: internal oscillators
T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. <tbd>.

Fig 26. Internal RC oscillator frequency versus temperature

11.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

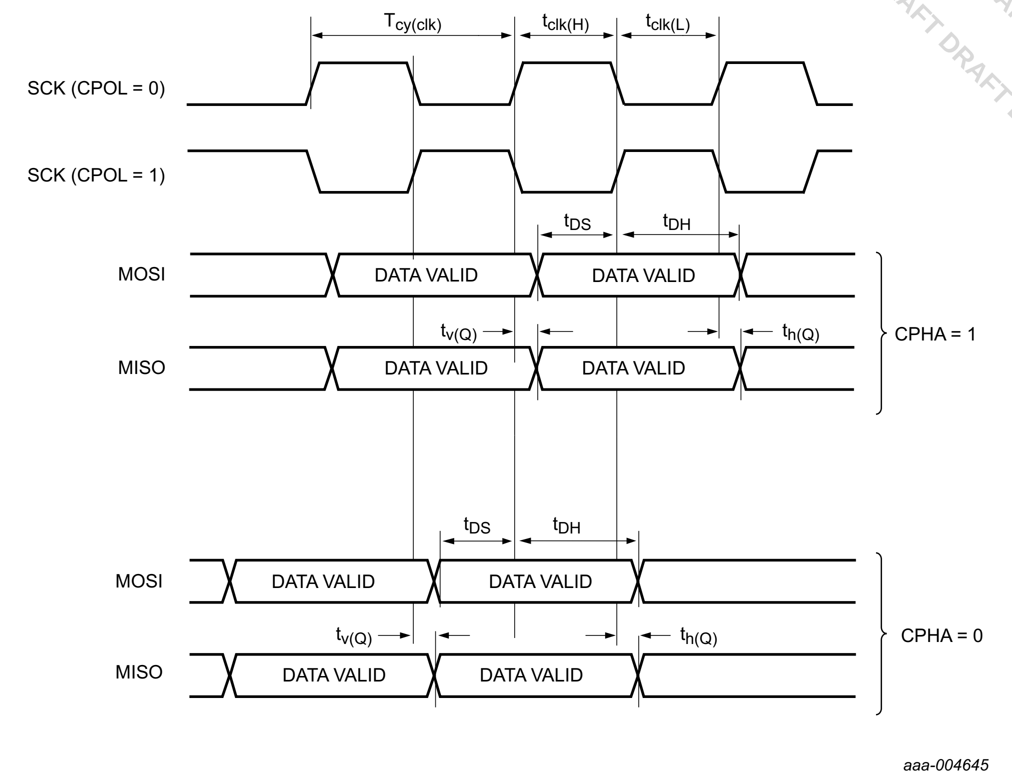
[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 29. SPI slave timing in SPI mode

11.8 USART interface

The maximum USART bit rate is 1.875 Mbit/s in asynchronous mode and 30 Mbit/s in synchronous mode slave and master mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 19. Dynamic characteristics: USART interface in synchronous master mode
T_{amb} = −40 °C to 85 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V; C_L = <tbd> pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pins Ux_SCLK	-	<tbd>	-	μs
output						
$t_{v(Q)}$	data output valid time	on pin Ux_TXD	-	<tbd>	-	ns

12. Analog characteristics

12.1 BOD

Table 20. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 0				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V

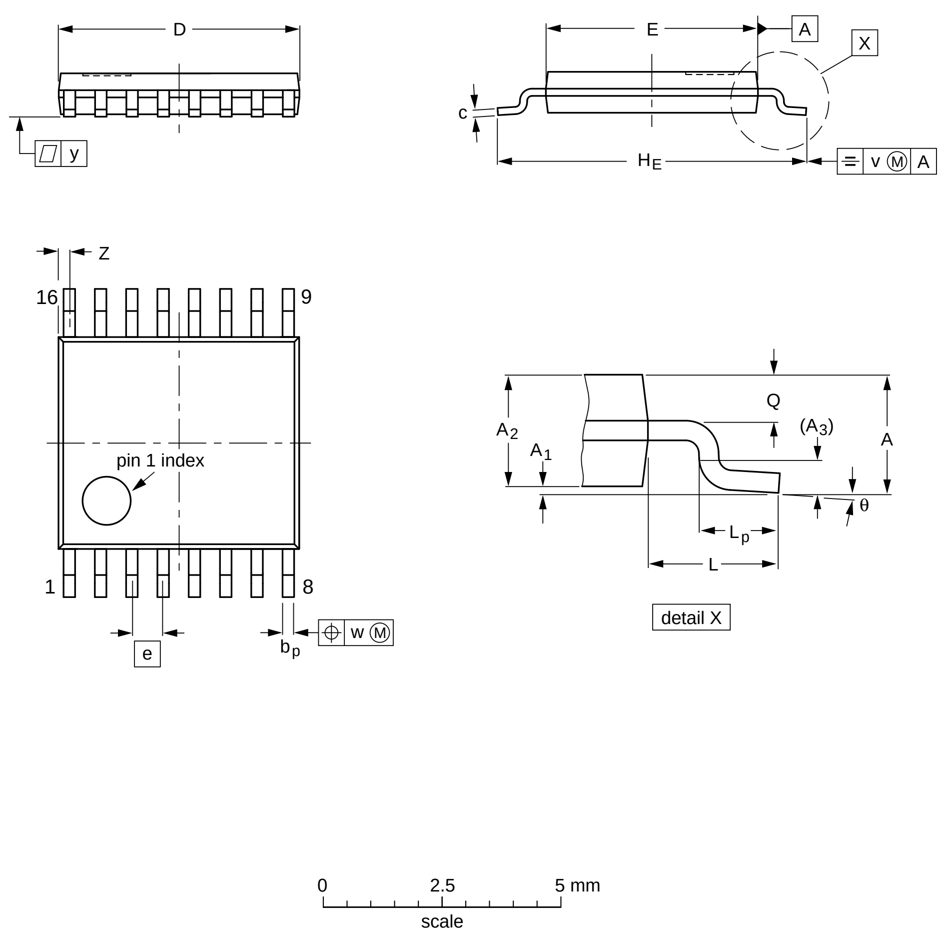
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL.

12.2 POR

Table 21. POR static characteristics
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}		V_{DD} rising<tbd>				
		V_{DD} falling<tbd>	-	<tbd>	-	V

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

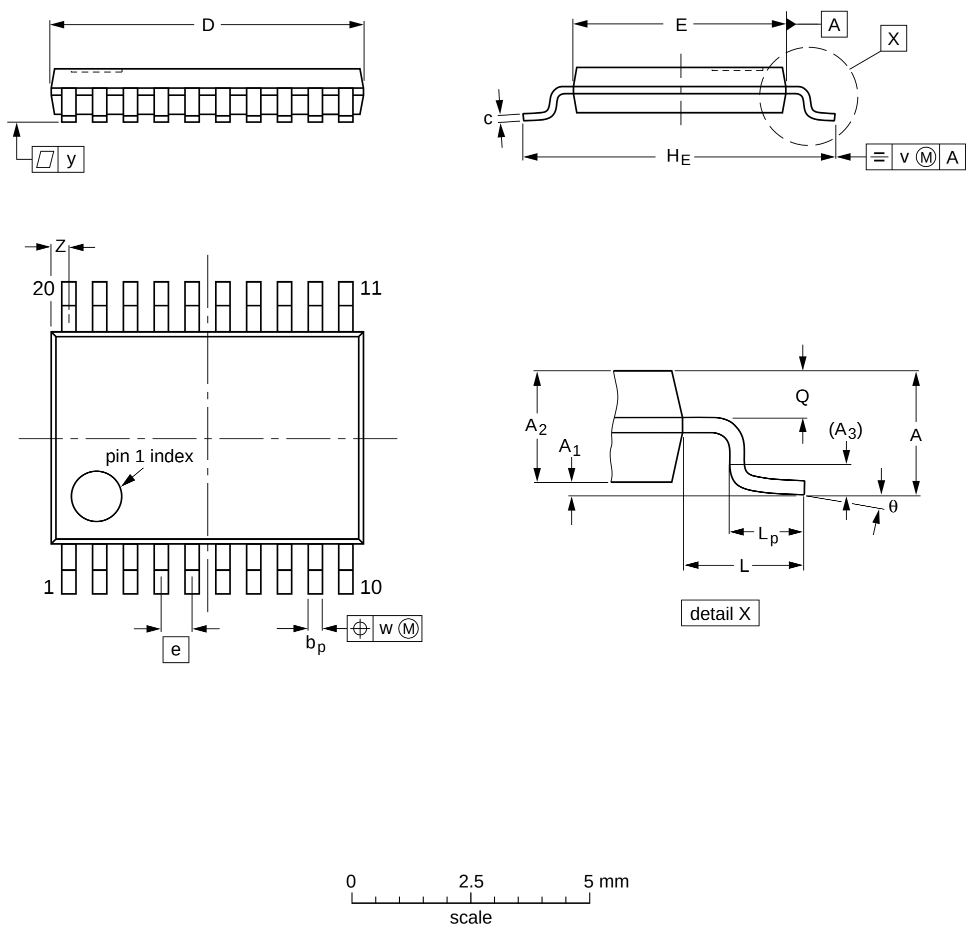
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 33. Package outline SOT403-1 (TSSOP16)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 35. Package outline SOT360-1 (TSSOP20)

18. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81xM v.1	<tbd>	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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