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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101fdh16fp

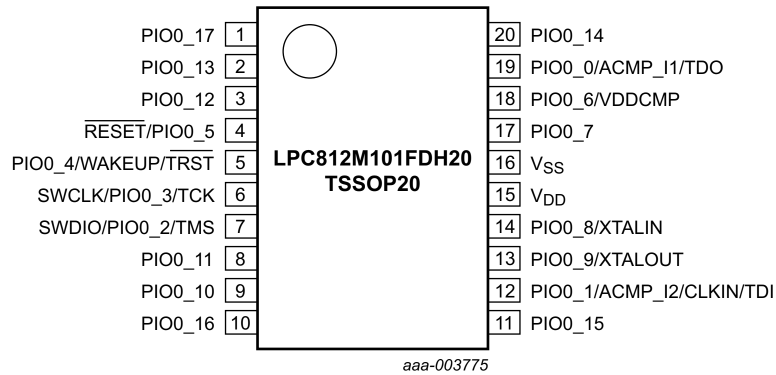


Fig 5. Pin configuration TSSOP20 package

6.2 Pin description

The pin description table Table 3 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between the GPIO, comparator, SWD, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable function for the I2C, USART, SPI, and SCT pin functions can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 3. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	DIP8		Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	8	[5]	I/O	I; PU	**PIO0_0 —** General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
					AI	-	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	5	[5]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler. In boundary scan mode: TDI (Test Data In).
					AI	-	**ACMP_I2 —** Analog comparator input 2.
					I	-	**CLKIN —** External clock input.
SWDIO/PIO0_2/TMS	7	6	4	[2]	I/O	I; PU	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
					I/O	-	**PIO0_2 —** General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	3	[2]	I/O	I; PU	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					I/O	-	**PIO0_3 —** General purpose digital input/output pin.

Table 4. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I^2C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I^2C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 9 "LPC81xM clock generation"). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 7.9 for details.

7.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

7.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 7).
- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

7.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and deep power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minters (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

7.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources. One clock source originates from the always-on power domain.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

7.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

7.20.4 Clock output

The LPC81xM features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

7.20.5 Wake-up process

The LPC81xM begin operation at power-up by using the IRC as the clock source. This allows chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL is needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

7.20.6 Power control

The LPC81xM supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.20.6.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile API. The API is accessible through the on-chip ROM.

The power configuration routine configures the LPC81xM for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.20.6.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.21 System control

7.21.1 Reset

Reset has four sources on the LPC81xM: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

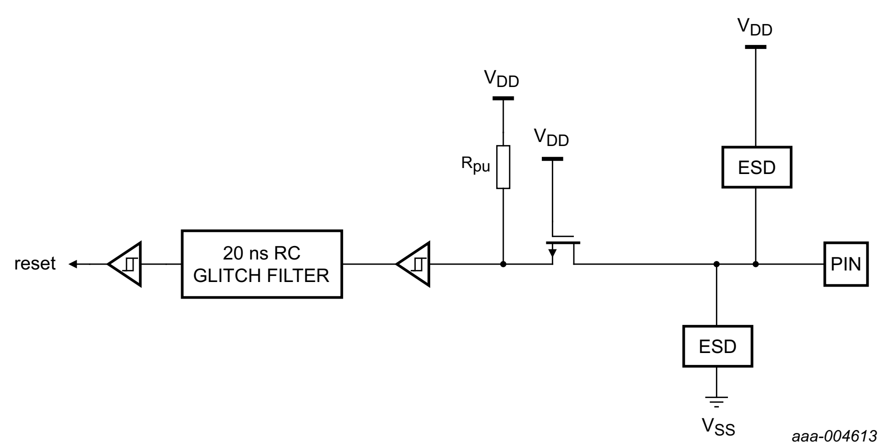


Fig 10. Reset pad configuration

7.21.2 Brownout detection

The LPC81xM includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.21.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC800 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC800 user manual*.

7.21.4 APB interface

The APB peripherals are located on one APB bus.

7.21.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, and the ROM.

7.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[3]	–0.5	+5.5	V
		5 V open-drain pins PIO0_10 and PIO0_11	[4]	–0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[5]	–0.5	+3.6	V
V_{IA}	analog input voltage		[6] [7]	–0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	–0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[8]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	<tbd>	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	-	<tbd>	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I²C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] V_{DD} present or not present.

[6] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

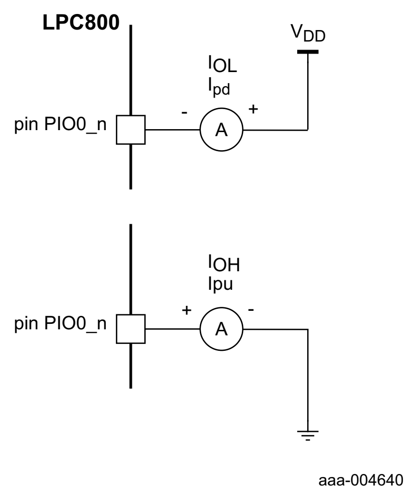
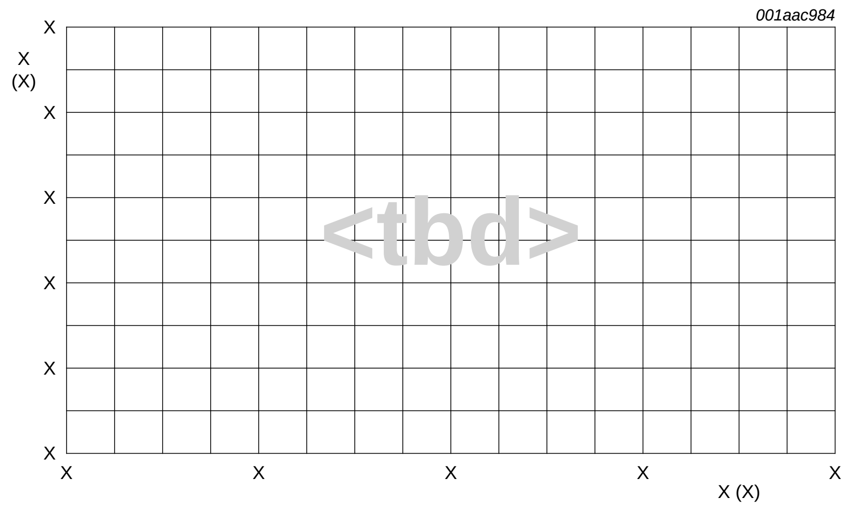
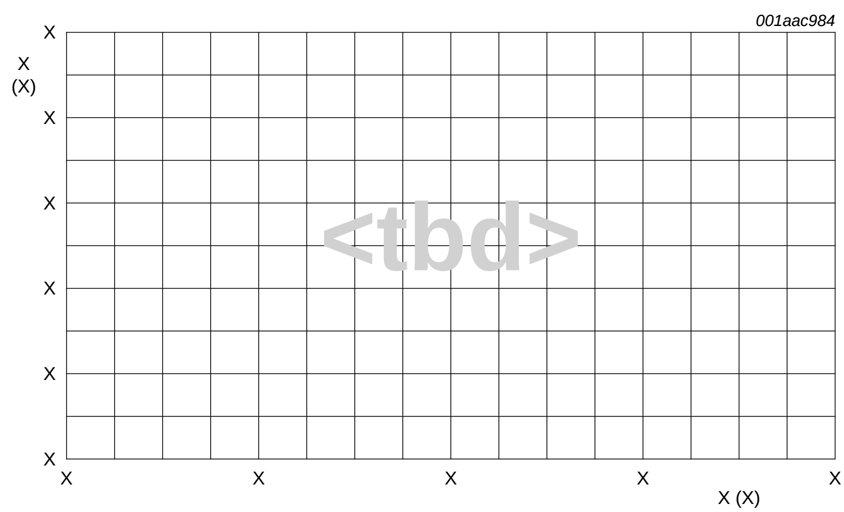


Fig 11. Pin input/output current measurement



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

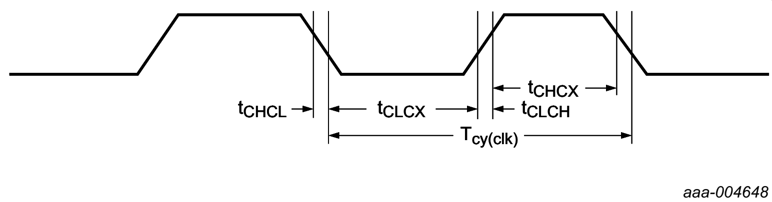


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

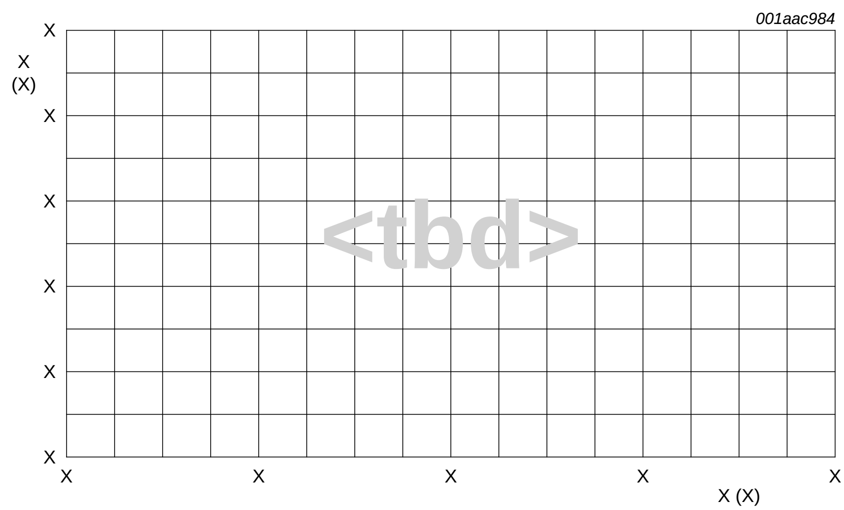
Table 13. Dynamic characteristic: internal oscillators

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. <tbd>.

Fig 26. Internal RC oscillator frequency versus temperature

11.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

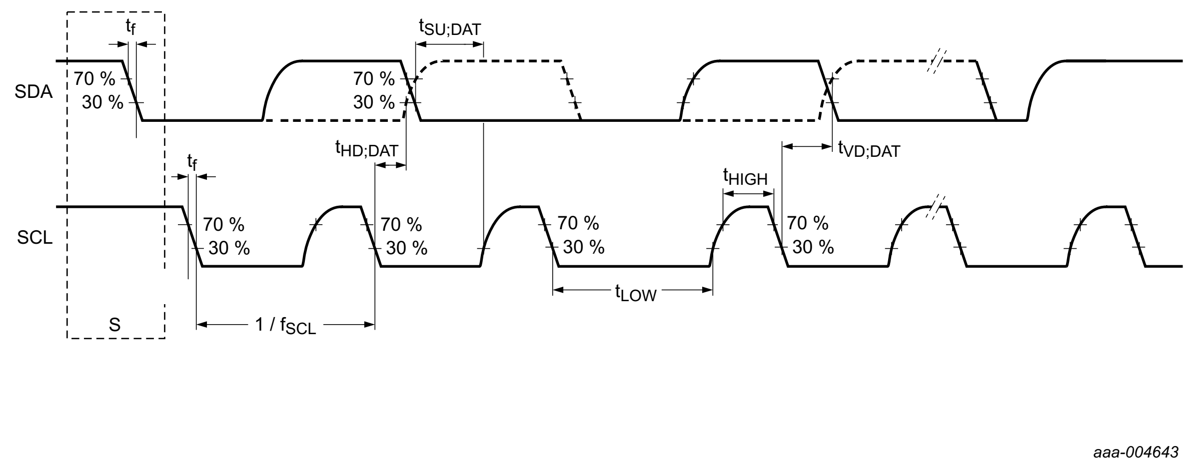


Fig 27. I²C-bus pins clock timing

11.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in slave and master modes.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 18. Dynamic characteristics of SPI pins

T_{amb} = −40 °C to 85 °C; C_L = <tbd>; 1.8 V <= V_{DD} <= 3.6 V. Simulated parameters; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode [1]	<tbd>	-	-	ns
		when only transmitting [1]	<tbd>			ns
t_{DS}	data set-up time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	<tbd>	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V	<tbd>			ns
		1.8 V ≤ V_{DD} < 2.0 V	<tbd>	-	-	ns
t_{DH}	data hold time	in SPI mode	<tbd>	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	-	<tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	<tbd>	-	-	ns

12.3 Comparator

Table 22. Comparator characteristics

$V_{DD(3V3)}$= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{DD}	supply current			-	<tbd>	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_{O}	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	<tbd>	-	mV
		V_{IC} = 1.5 V		-	<tbd>	-	mV
		V_{IC} = 2.8 V		-	<tbd>		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	<tbd>	-	µs
t_{PD}	propagation delay	HIGH to LOW; $V_{DD(3V3)}$ = 3.0 V;		-	<tbd>	<tbd>	
		V_{IC} = 0.1 V; 50 mV overdrive input	[1]				ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
t_{PD}	propagation delay	LOW to HIGH; $V_{DD(3V3)}$ = 3.0 V;		-	<tbd>	<tbd>	
		V_{IC} = 0.1 V; 50 mV overdrive input	[1]				ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	<tbd>	<tbd>	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	<tbd>	<tbd>	ns
V_{hys}	hysteresis voltage	positive hysteresis; $V_{DD(3V3)}$ = 3.0 V; V_{IC} = 1.5 V	[2]	-	<tbd>	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; $V_{DD(3V3)}$ = 3.0 V; V_{IC} = 1.5 V	[2]	-	<tbd>	-	mV
R_{lad}	ladder resistance	-		-	<tbd>	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	<tbd>	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	<tbd>	µs

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

13.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC800<tbd> in Table 27.

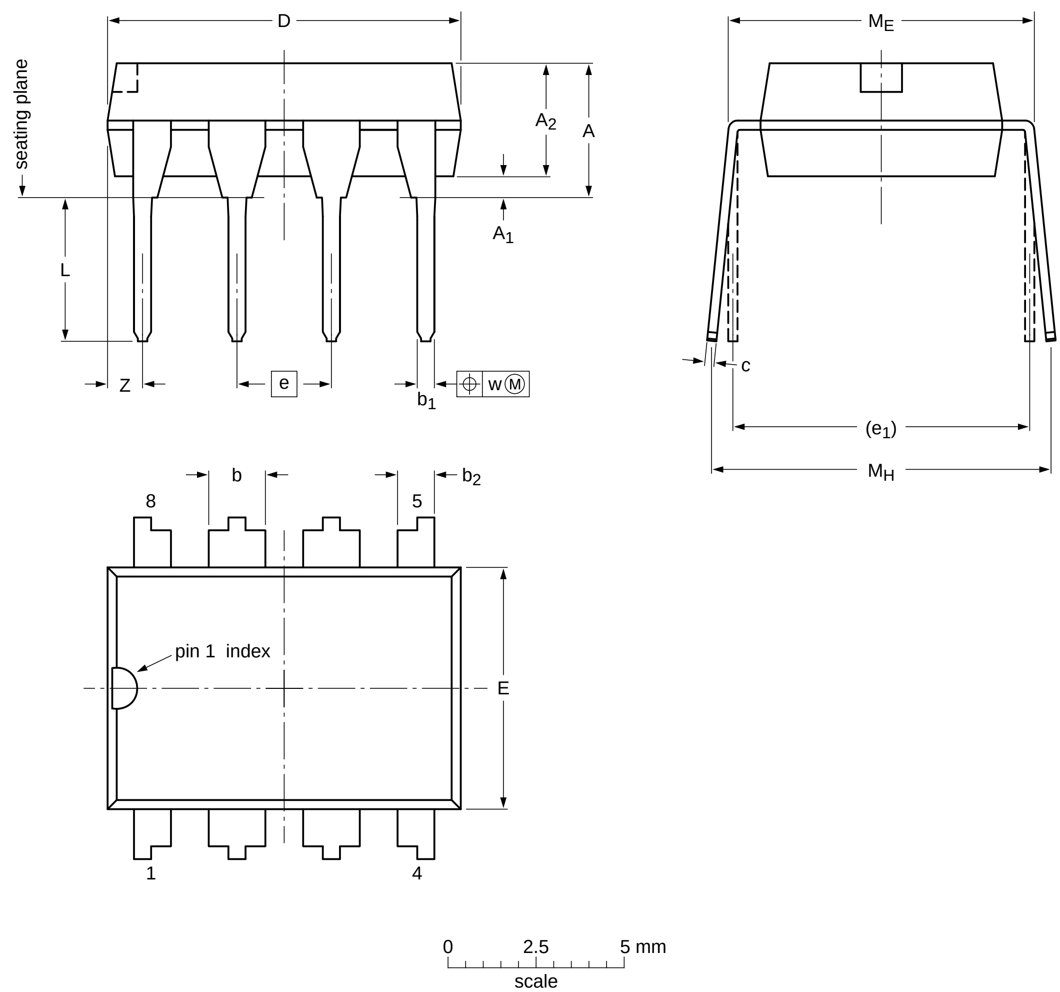
Table 27. ElectroMagnetic Compatibility (EMC) for part LPC800<tbd> (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	48 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz to 30 MHz	<tbd>	<tbd>	<tbd>	dBμV
	30 MHz to 150 MHz	<tbd>	<tbd>	<tbd>	dBμV
	150 MHz to 1 GHz	<tbd>	<tbd>	<tbd>	dBμV
IEC level[1]	-	<tbd>	<tbd>	<tbd>	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz to 30 MHz	<tbd>	<tbd>	<tbd>	dBμV
	30 MHz to 150 MHz	<tbd>	<tbd>	<tbd>	dBμV
	150 MHz to 1 GHz	<tbd>	<tbd>	<tbd>	dBμV
IEC level[1]	-	<tbd>	<tbd>	<tbd>	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

14. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit(1)		A	A_1	A_2	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1)
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

sot097-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 32. Package outline SOT097-2 (DIP8)

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