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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	30MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc812m101fdh20fp

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5. Block diagram

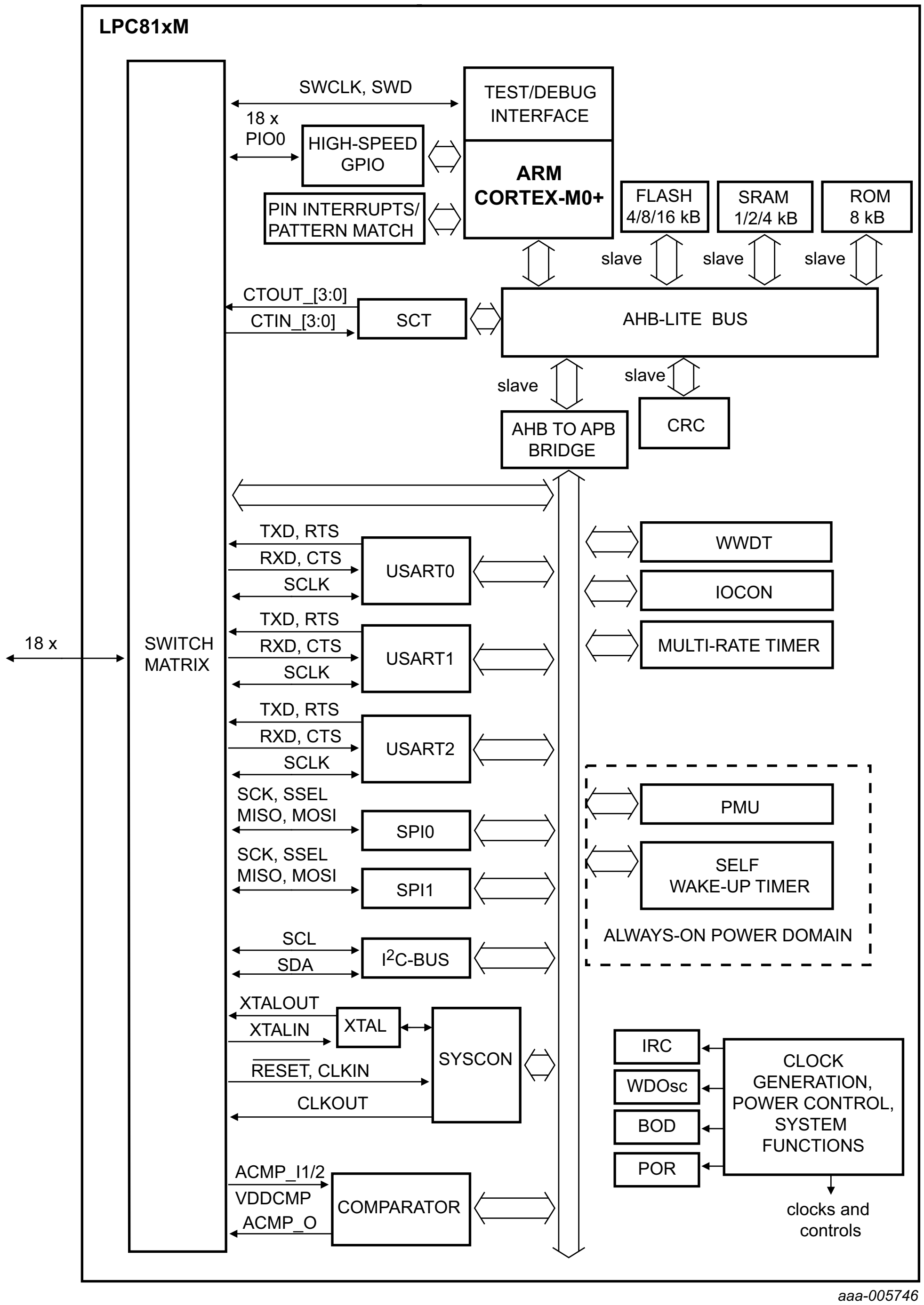

Fig 1. LPC81xM block diagram

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6. Pinning information

6.1 Pinning

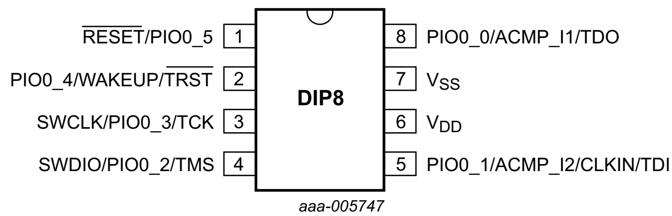

Fig 2. Pin configuration DIP8 package (LPC810M021FN8)

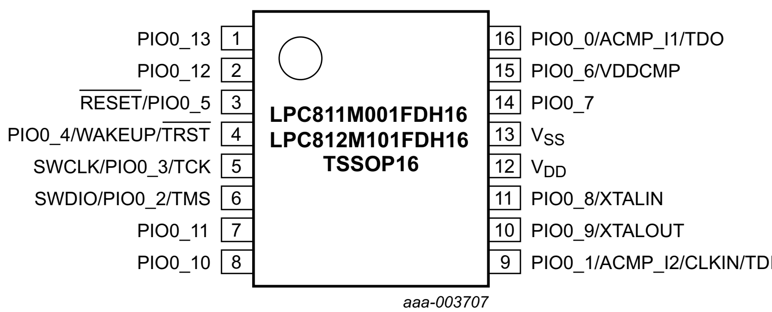

Fig 3. Pin configuration TSSOP16 package

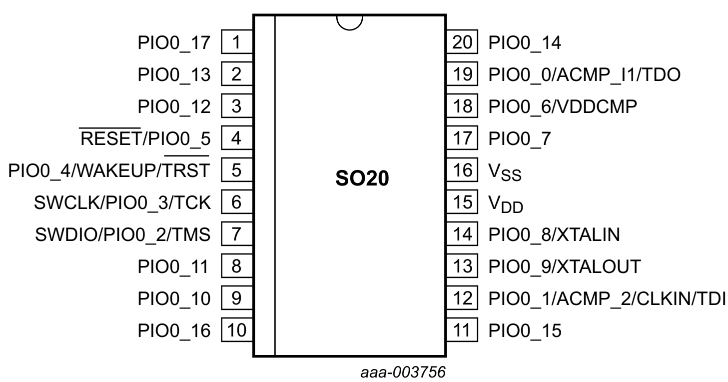

Fig 4. Pin configuration SO20 package (LPC812M101FD20)

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- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 9 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 7.9 for details.

7.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

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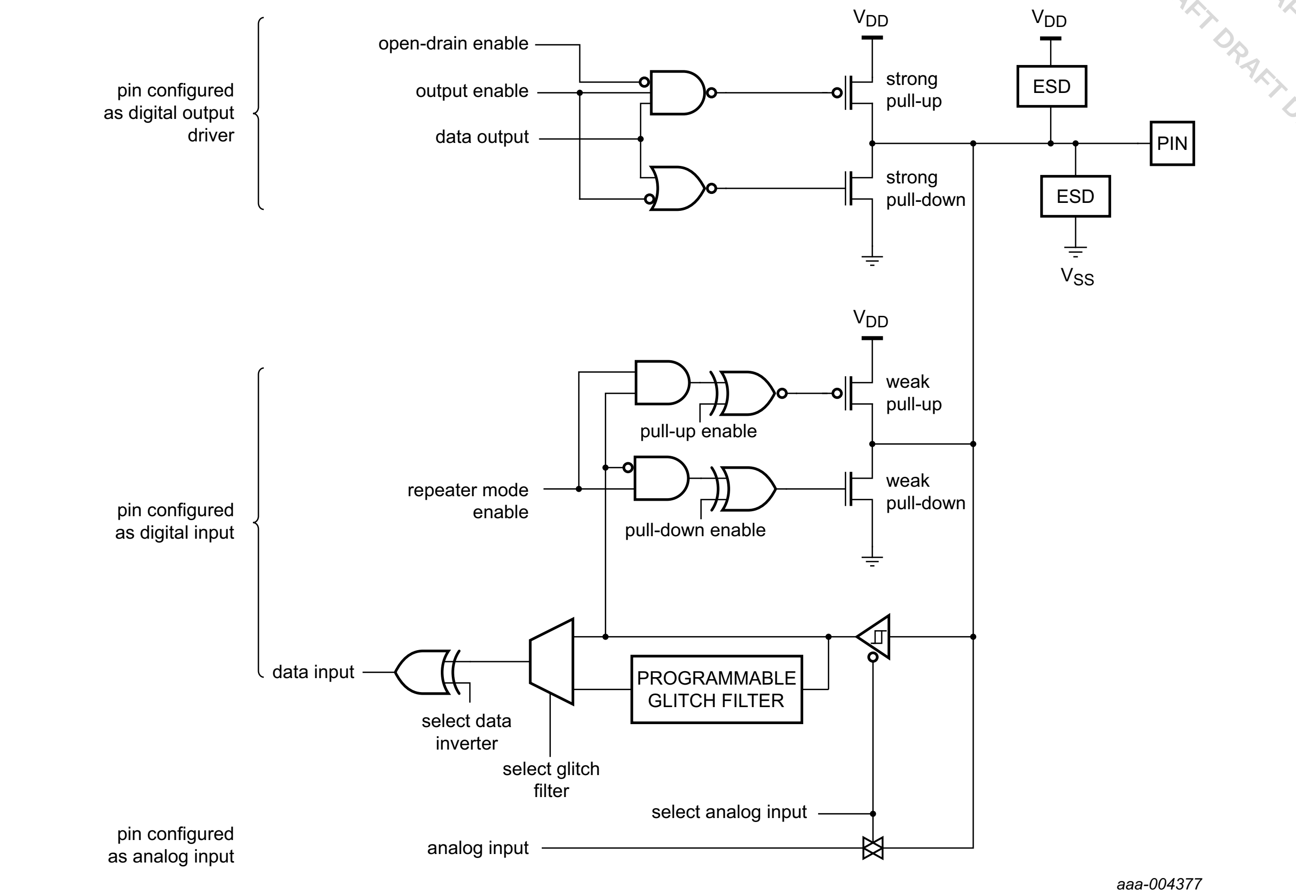

Fig 7. Standard I/O pad configuration

7.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

7.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing.

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- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

7.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 7).
- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

7.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and deep power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minters (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.

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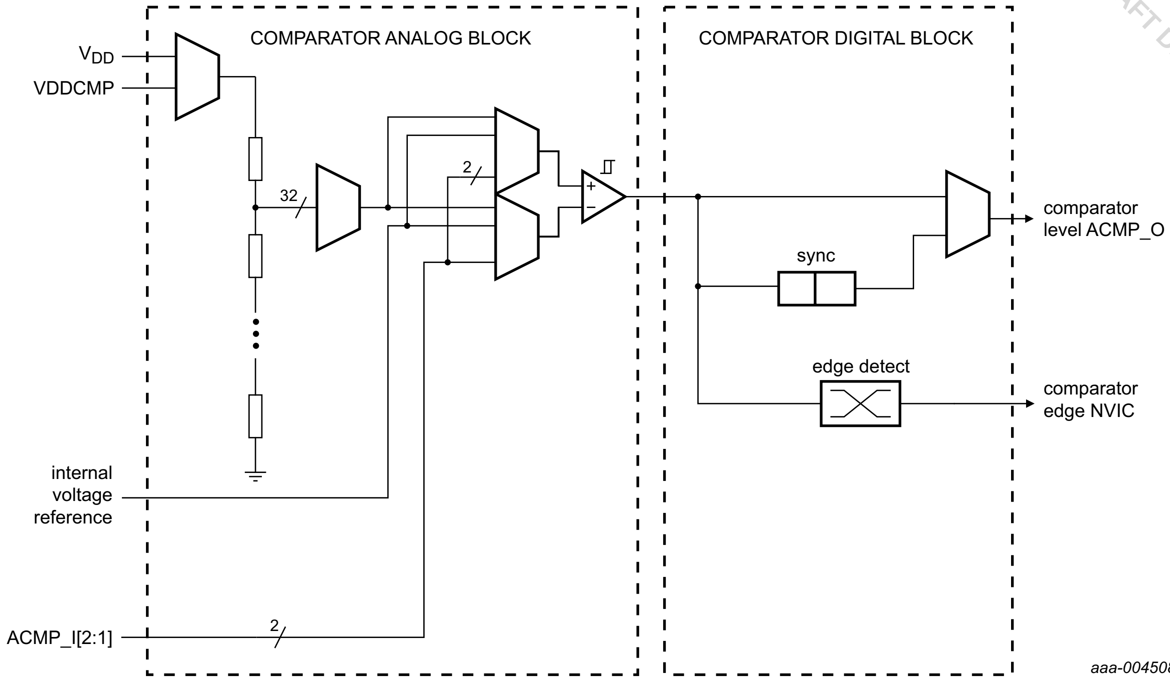

Fig 8. Comparator block diagram

7.19.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap and temperature sensor selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- The comparator output can be routed internally to the SCT input through the switch matrix.

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7.20 Clocking and power control

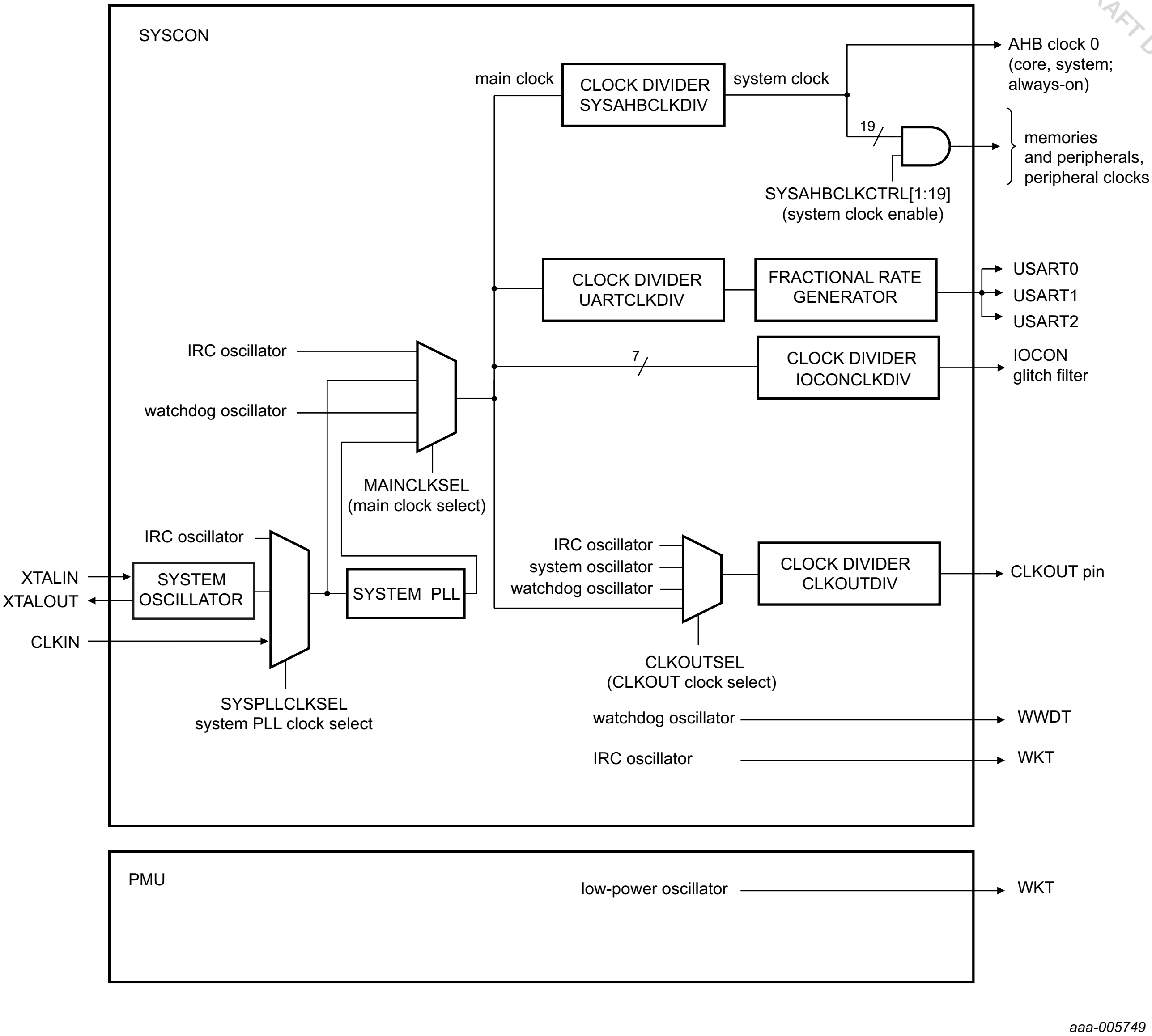

Fig 9. LPC81xM clock generation

7.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

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7.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The RESET pin selects between the JTAG boundary scan (RESET = LOW) and the ARM SWD debug (RESET = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the RESET pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the RESET pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the TRST pin to enable the SWD debug mode, and release the RESET pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[3]	−0.5	+5.5	V
		5 V open-drain pins PIO0_10 and PIO0_11	[4]	−0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[5]	−0.5	+3.6	V
V_{IA}	analog input voltage		[6] [7]	−0.5 V	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[8]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	<tbd>	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[9]	-	<tbd>	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] V_{DD} present or not present.

[6] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

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10. Static characteristics

Table 9. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.4	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	<tbd>	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][6][7][8]	-	5.5	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][6][7][8]	-	<tbd>	-	mA
		Sleep mode; system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	0.8	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	<tbd>	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	2.6	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	<tbd>	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][9]	-	170	-	μA
		Power-down mode; V_{DD} = 3.3 V	[2][3][9]	-	2	-	μA
		Deep power-down mode; V_{DD} = 3.3 V; Low-power oscillator off	[2][10]	-	220	-	nA
		Low-power oscillator on/WKT wake-up enabled			<tbd>	-	nA
Standard port pins configured as digital pins, $\overline{RESET}$, see Figure 11							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	<tbd>	<tbd>	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	<tbd>	<tbd>	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	<tbd>	<tbd>	nA
V_I	input voltage	$V_{DD} \geq 1.8$ V; 5 V tolerant pins except PIO0_6	[12][14]	0	-	5	V
		$V_{DD} \geq 1.8$ V; on 3 V tolerant pin PIO0_6		0	-	3.6	
		V_{DD} = 0 V		0	-	3.6	V

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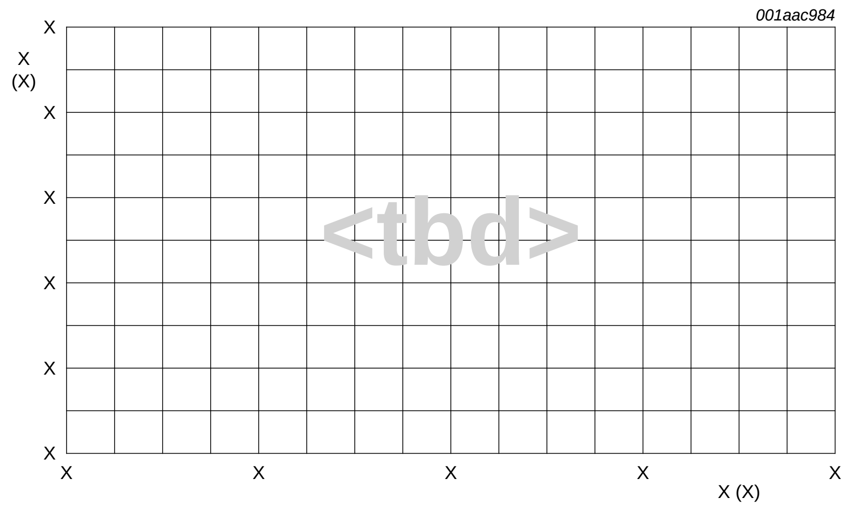
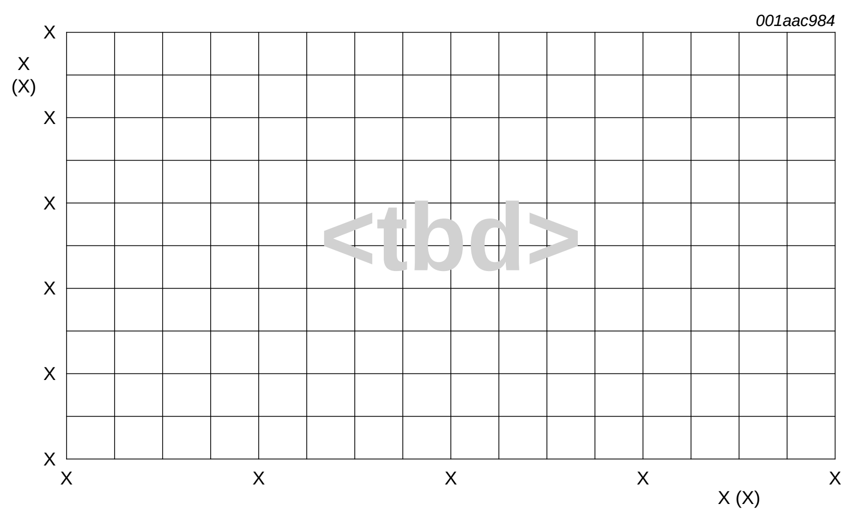


Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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10.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	30 MHz	
IRC	<tbd>	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	<tbd>	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	<tbd>	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	<tbd>	-	-	Independent of main clock frequency.
Main PLL	-	<tbd>	-	-
CLKOUT	-	<tbd>	<tbd>	Main clock divided by 4 in the CLKOUTDIV register.
SCT	-	<tbd>	<tbd>	-
MRT	-	<tbd>	<tbd>	-
WKT	-	<tbd>	<tbd>	-
GPIO	-	<tbd>	<tbd>	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
Pin interrupt/pattern match		<tbd>	<tbd>	-
IOCON	-	<tbd>	<tbd>	-
I2C	-	<tbd>	<tbd>	-
ROM	-	<tbd>	<tbd>	-
SPI0	-	<tbd>	<tbd>	-
SPI1	-	<tbd>	<tbd>	-
USART0	-	<tbd>	<tbd>	-
USART1	-	<tbd>	<tbd>	-
USART2	-	<tbd>	<tbd>	-
WWDT	-	<tbd>	<tbd>	Main clock selected as clock source for the WDT.
Comparator	-	<tbd>	<tbd>	-
CRC	-	<tbd>	<tbd>	-
SWM	-	<tbd>	<tbd>	-

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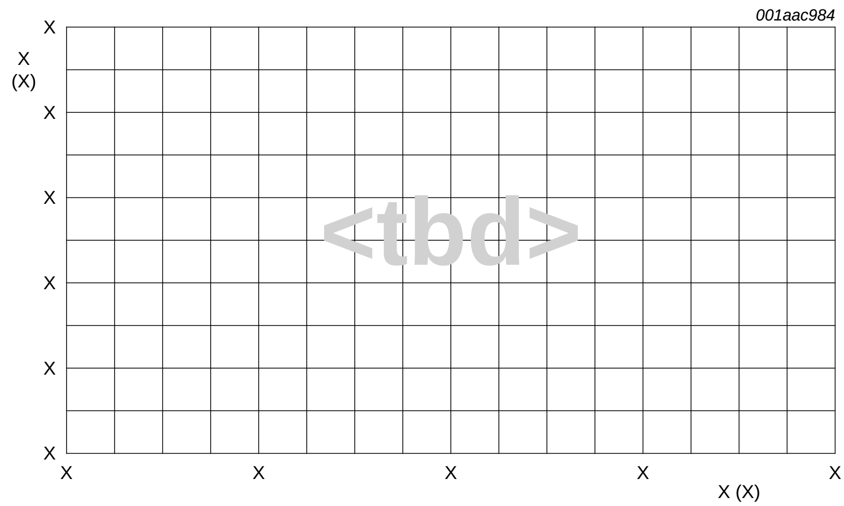
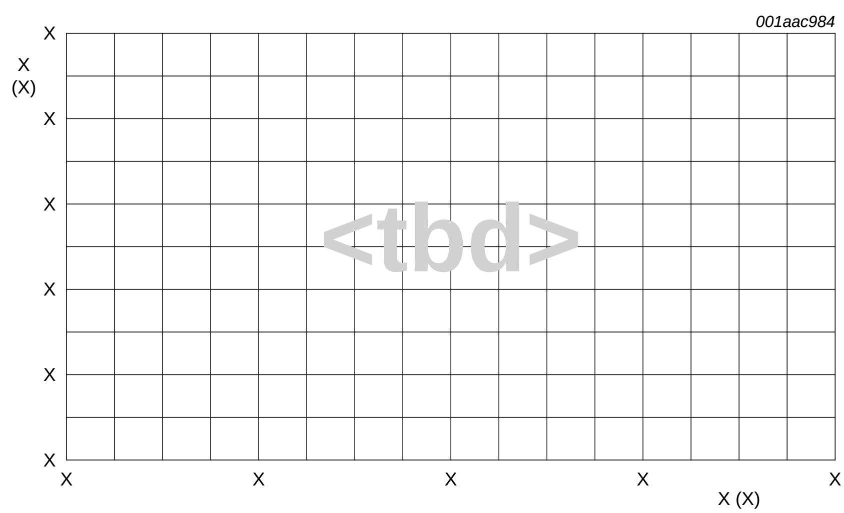


Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins and <tbd>.

Fig 21. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 22. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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11. Dynamic characteristics

11.1 Power-up ramp conditions

<tbd>

11.2 Flash memory

Table 11. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[2][1]	10000	100000	-	cycles
t_{ret}	retention time	powered	[2]	10	20	-	years
		unpowered	[2]	20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors	[2]	95	100	105	ms
t_{prog}	programming time		[2][3]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Min and max values are valid for T_{amb} = −40 °C to +85 °C only.

[3] Programming times are given for writing <tbd> bytes to the flash. T_{amb} < +85 °C. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC800 user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

11.3 External clock for the oscillator in slave mode and CLKIN

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 9). For connecting the oscillator to the XTAL pins, also see Section 13.1.

Table 12. Dynamic characteristic: external clock (XTALIN or CLKIN inputs)

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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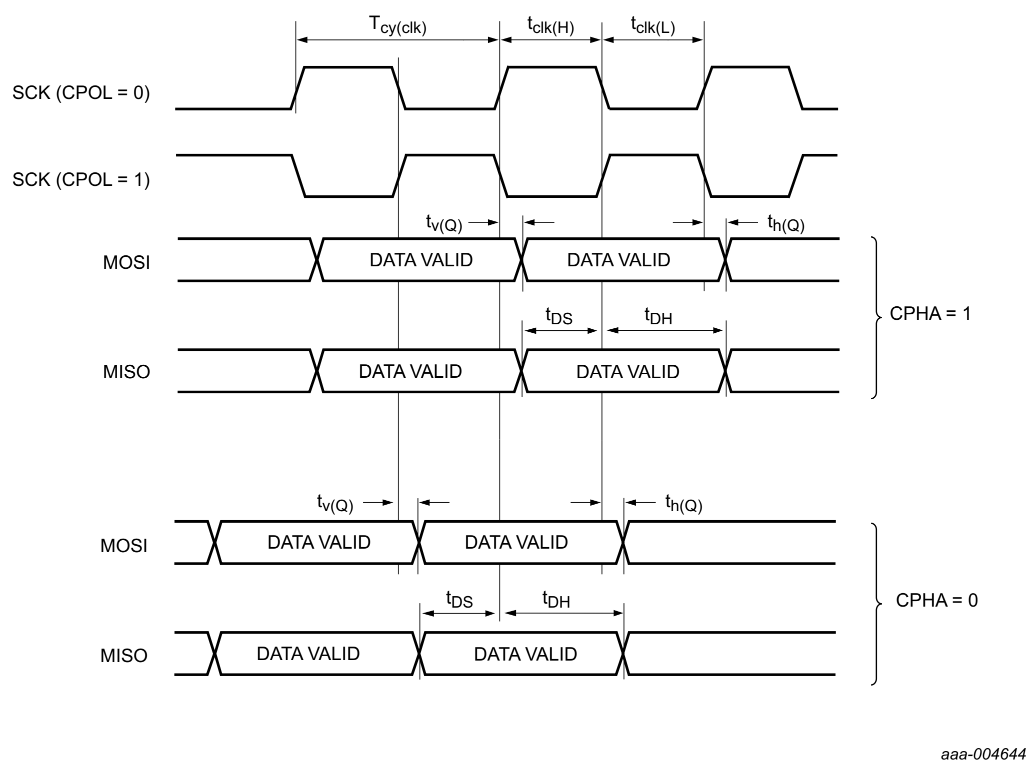
Table 18. Dynamic characteristics of SPI pins

T_{amb} = −40 °C to 85 °C; C_L = <tbd>; 1.8 V <= V_{DD} <= 3.6 V. Simulated parameters; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			<tbd>	-	-	ns
t_{DS}	data set-up time	in SPI mode	[2]	<tbd>	-	-	ns
t_{DH}	data hold time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	[2]	<tbd>	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V		<tbd>			ns
		1.8 V ≤ V_{DD} < 2.0 V		<tbd>	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	<tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	-	-	<tbd>	ns

[1] $T_{cy(clk)}$ = <tbd>.

[2] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 28. SPI master timing in SPI mode

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[1] Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator channels<tbd>.

Table 24. Comparator voltage ladder reference static characteristics
$V_{DD(3V3)}$ = 3.3 V; T_{amb} = -40 °C to + 85°C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal $V_{DD(3V3)}$ supply			<tbd>	<tbd>	
		decimal code = 00	[2]	-			%
		decimal code = 08		-	<tbd>	<tbd>	%
		decimal code = 16		-	<tbd>	<tbd>	%
		decimal code = 24		-	<tbd>	<tbd>	%
		decimal code = 30		-	<tbd>	<tbd>	%
		decimal code = 31		-	<tbd>	<tbd>	%
$E_{V(O)}$	output voltage error	External VDDCMP supply			<tbd>	<tbd>	
		decimal code = 00		-			%
		decimal code = 08		-	<tbd>	<tbd>	%
		decimal code = 16		-	<tbd>	<tbd>	%
		decimal code = 24		-	<tbd>	<tbd>	%
		decimal code = 30		-	<tbd>	<tbd>	%
		decimal code = 31		-	<tbd>	<tbd>	%

[1] Measured <tbd> with a 2 kHz input signal and overdrive < 100 μV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.

13. Application information

13.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

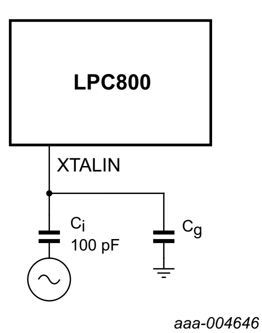

Fig 30. Slave mode operation of the on-chip oscillator

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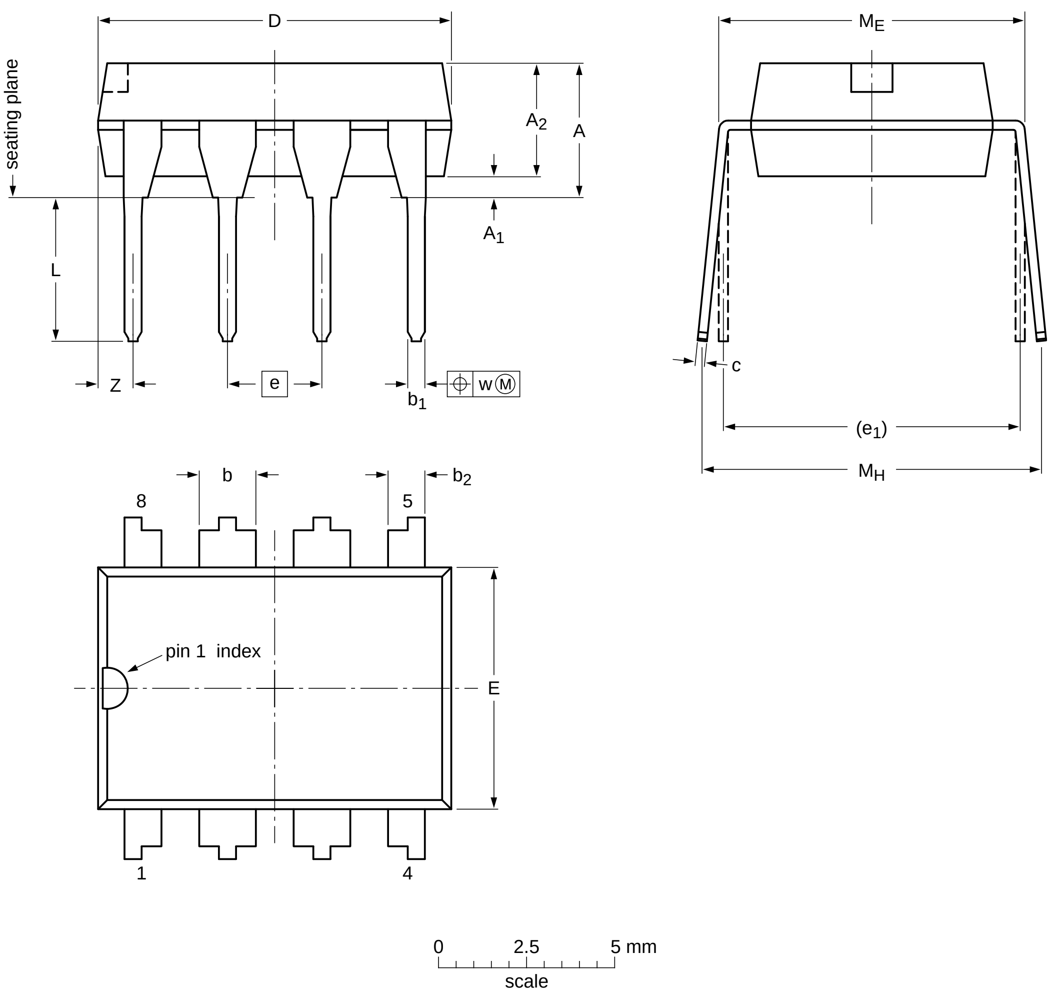
14. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit(1)		A	A_1	A_2	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1)
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

sot097-2_po

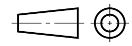
Outline version	References IEC	References JEDEC	References JEITA		European projection	Issue date
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 32. Package outline SOT097-2 (DIP8)

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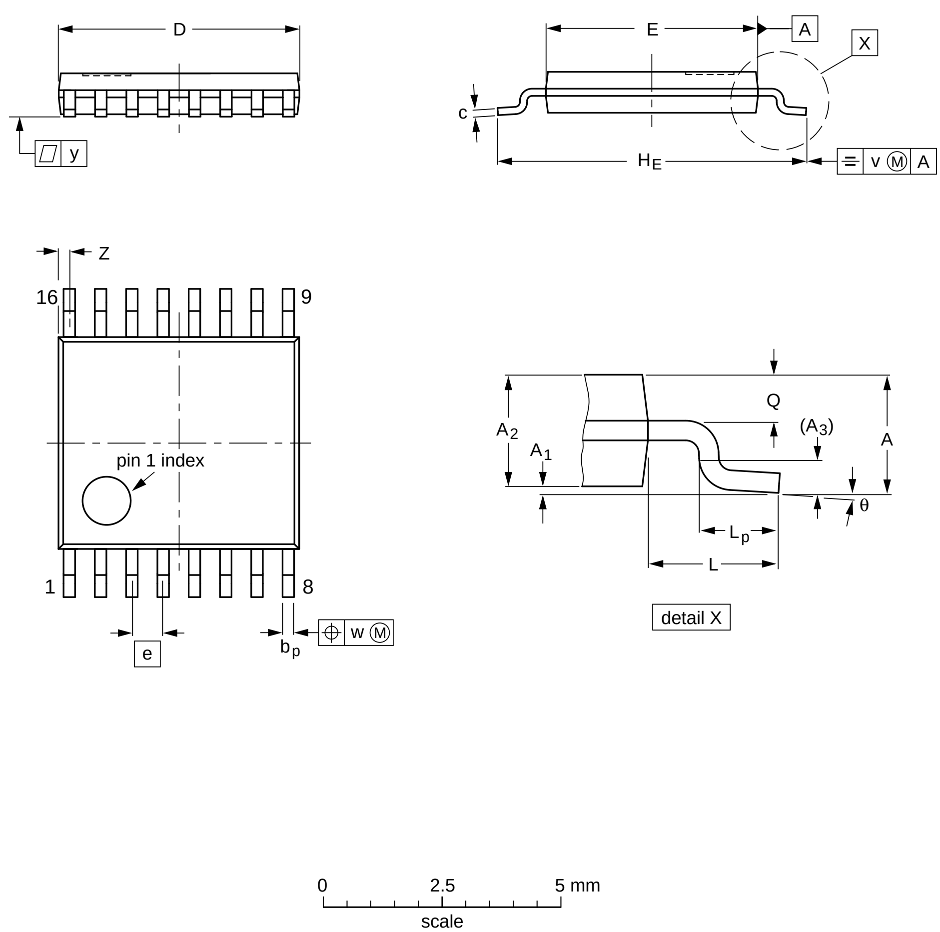
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 33. Package outline SOT403-1 (TSSOP16)

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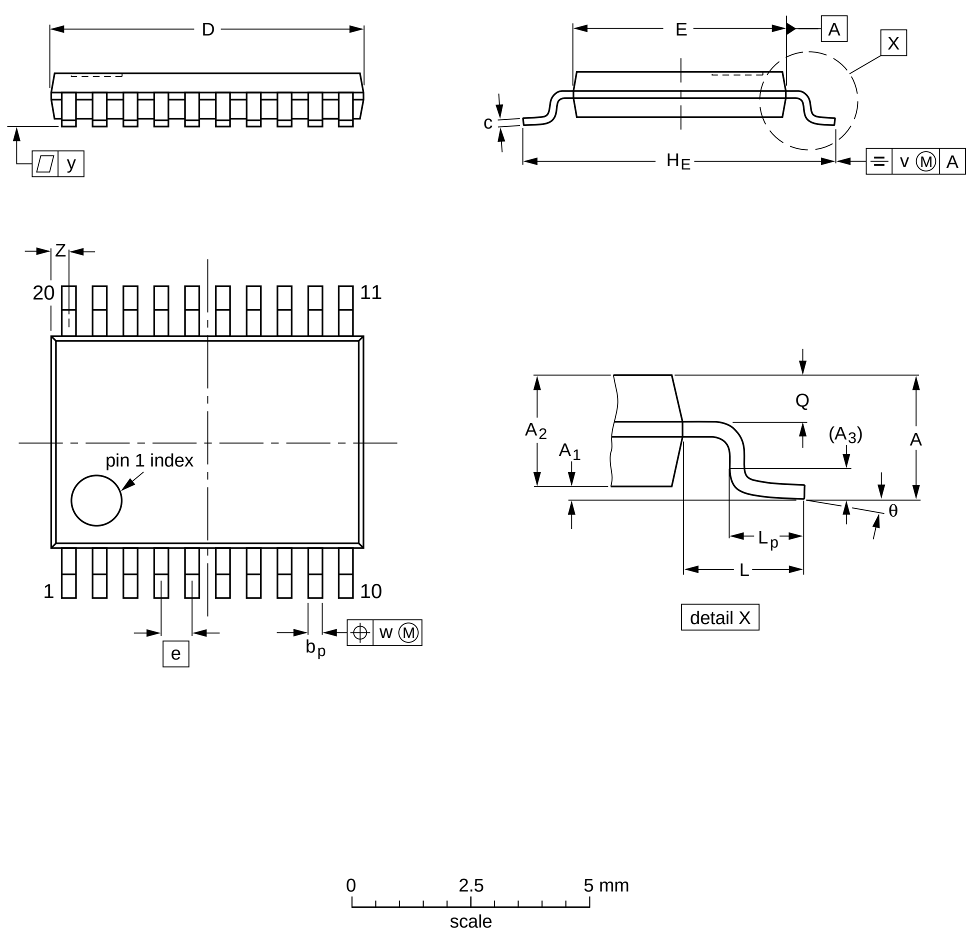
TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 35. Package outline SOT360-1 (TSSOP20)

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For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 November 2012

Document identifier: LPC81xM