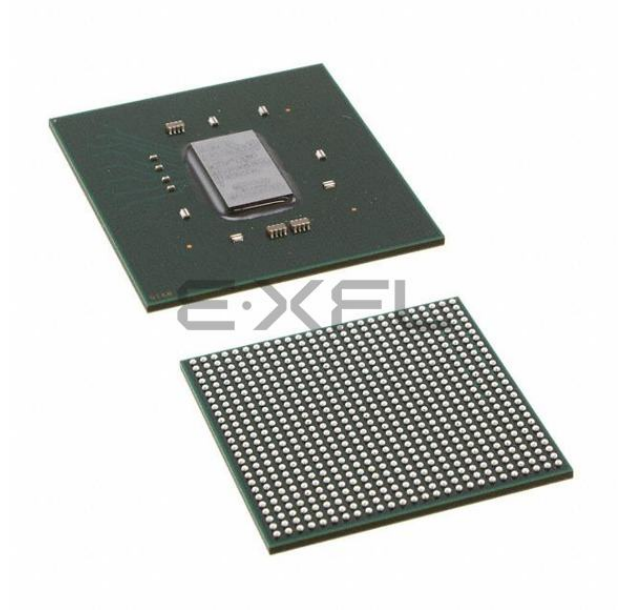
AMD Xilinx - XCKU040-1FBVA676I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	30300
Number of Logic Elements/Cells	530250
Total RAM Bits	21606000
Number of I/O	312
Number of Gates	-
Voltage - Supply	0.922V ~ 0.979V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcku040-1fbva676i

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R(7)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HR I/O banks (measured per JEDEC specification)					
R(7)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	–50%	60	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100)	–	100	–	Ω
n	Temperature diode ideality factor	–	1.002	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
6. VRP resistor tolerance is (240Ω ±1%)
7. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT}/V_{CCINT_IO} and V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCINT}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. When the current minimums are met, the device powers on after the V_{CCINT}/V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 17. In each table, the I/O bank type is either high performance (HP) or high range (HR).

Table 23: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages								Units
		1.0V		0.95V				0.90V		
		-3		-2		-1/-1L		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
	HR	0	1250	0	1250	0	1000	0	1000	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	Mb/s
	HR	0	625	0	625	0	500	0	500	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
	HR	0	1250	0	1250	0	1000	0	1000	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	Mb/s
	HR	0	625	0	625	0	500	0	500	Mb/s

Notes:
1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 24: **LVDS Native Mode Performance(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages								Units
		1.0V		0.95V				0.90V		
		-3		-2		-1/-1L		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE 4:1, 8:1)	HP	300	1600	300	1600	300	1400	300	1400	Mb/s
	HR	300	1250	300	1250	300	1250	300	1250	Mb/s
LVDS TX SDR (TX_BITSLICE 2:1, 4:1)	HP	150	800	150	800	150	700	150	700	Mb/s
	HR	150	625	150	625	150	625	150	625	Mb/s
LVDS RX DDR (RX_BITSLICE 1:4, 1:8)(2)	HP	300	1600	300	1600	300	1400	300	1400	Mb/s
	HR	300	1250	300	1250	300	1250	300	1250	Mb/s
LVDS RX SDR (RX_BITSLICE 1:2, 1:4)(2)	HP	150	800	150	800	150	700	150	700	Mb/s
	HR	150	625	150	625	150	625	150	625	Mb/s

Notes:
1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

Table 25: **LVDS Native-Mode 1000BASE-X Support(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages			
		1.0V	0.95V		0.90V
		-3	-2	-1/-1L	-1L
1000BASE-X	HP	Yes	Yes	Yes	Yes

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 26 provides the maximum data rates for applicable memory standards using the Kintex UltraScale FPGAs memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 26: **Maximum Physical Interface (PHY) Rate for Memory Interfaces by I/O and Package**

Memory Standard	I/O Bank Type	Package	DRAM Type	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages					Units
				1.0V	0.95V			0.90V	
				-3E	-2E	-2I	-1C/I -1M -1LI	-1LI	
DDR4	HP	All FF/RF packages All FL packages FBVA900	Single rank component	2400	2400	2400	2133	2133	Mb/s
			1 rank DIMM(1)(2)	2133	2133	2133	1866	1866	
			2 rank DIMM(1)(3)	1866	1866	1866	1600	1600	
			4 rank DIMM(1)(4)	1333	1333	1333	N/A	N/A	
		FBVA676 RBA676 SFVA784	Single rank component	2133	2133	2133	1866	1866	
			1 rank DIMM(1)(2)	1866	1866	1866	1600	1600	
			2 rank DIMM(1)(3)	1600	1600	1600	1333	1333	
DDR3	HP	All FF/RF packages All FL packages FBVA676 RBA676 FBVA900	Single rank component	2133	2133	2133	1866	1866	Mb/s
			1 rank DIMM(1)(2)	1866	1866	1866	1600	1600	
			2 rank DIMM(1)(3)	1600	1600	1600	1333	1333	
			4 rank DIMM(1)(4)	1066	1066	1066	800	800	
		SFVA784	Single rank component	1866	1866	1866	1600	1600	
			1 rank DIMM(1)(2)	1600	1600	1600	1333	1333	
			2 rank DIMM(1)(3)	1333	1333	1333	1066	1066	
			4 rank DIMM(1)(4)	800	800	800	606	606	
	HR	All	Single rank component	1333(5)			1066	1066	

Table 27: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	
	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	
HSTL_I_18_F	0.52	0.55	0.59	0.59	0.59	0.73	0.73	0.93	0.93	0.93	0.84	0.84	1.08	1.08	1.08	ns
HSTL_I_18_S	0.52	0.55	0.59	0.59	0.59	0.85	0.85	1.05	1.05	1.05	0.95	0.96	1.18	1.18	1.18	ns
HSTL_I_F	0.52	0.55	0.59	0.59	0.59	0.75	0.75	0.94	0.94	0.95	0.92	0.92	1.16	1.16	1.17	ns
HSTL_I_S	0.52	0.55	0.59	0.59	0.59	0.79	0.79	0.98	0.98	0.99	0.97	1.00	1.25	1.25	1.25	ns
HSTL_II_18_F	0.52	0.55	0.59	0.59	0.59	0.82	0.82	1.01	1.01	1.02	0.97	1.00	1.25	1.25	1.25	ns
HSTL_II_18_S	0.52	0.55	0.59	0.59	0.59	0.85	0.85	1.05	1.05	1.05	1.03	1.05	1.30	1.30	1.30	ns
HSTL_II_F	0.52	0.55	0.59	0.59	0.59	0.73	0.73	0.93	0.93	0.93	0.89	0.90	1.13	1.13	1.13	ns
HSTL_II_S	0.52	0.55	0.59	0.59	0.59	0.82	0.82	1.01	1.01	1.02	0.98	0.98	1.22	1.22	1.22	ns
HSUL_12_F	0.52	0.55	0.59	0.59	0.59	0.75	0.75	0.94	0.94	0.95	0.75	0.75	0.94	0.94	0.95	ns
HSUL_12_S	0.52	0.55	0.59	0.59	0.59	0.84	0.84	1.04	1.04	1.04	0.96	0.97	1.15	1.15	1.15	ns
LVCMOS12_F_12	0.76	0.95	0.95	0.95	0.95	0.95	0.95	1.16	1.16	1.16	0.95	0.95	1.16	1.16	1.16	ns
LVCMOS12_F_4	0.76	0.95	0.95	0.95	0.95	1.13	1.16	1.39	1.39	1.39	1.13	1.16	1.39	1.39	1.39	ns
LVCMOS12_F_8	0.76	0.95	0.95	0.95	0.95	0.97	0.97	1.19	1.19	1.19	0.97	0.97	1.19	1.19	1.19	ns
LVCMOS12_S_12	0.76	0.95	0.95	0.95	0.95	1.06	1.06	1.28	1.28	1.28	1.06	1.06	1.28	1.28	1.28	ns
LVCMOS12_S_4	0.76	0.95	0.95	0.95	0.95	1.27	1.36	1.60	1.60	1.60	1.27	1.36	1.60	1.60	1.60	ns
LVCMOS12_S_8	0.76	0.95	0.95	0.95	0.95	1.10	1.10	1.32	1.32	1.32	1.10	1.10	1.32	1.32	1.32	ns
LVCMOS15_F_12	0.68	0.82	0.87	0.87	0.88	0.96	0.96	1.18	1.18	1.18	0.96	0.96	1.18	1.18	1.18	ns
LVCMOS15_F_16	0.68	0.82	0.87	0.87	0.88	0.94	0.94	1.15	1.15	1.15	0.94	0.94	1.17	1.17	1.17	ns
LVCMOS15_F_4	0.68	0.82	0.87	0.87	0.88	1.15	1.15	1.38	1.38	1.39	1.15	1.15	1.38	1.38	1.39	ns
LVCMOS15_F_8	0.68	0.82	0.87	0.87	0.88	1.02	1.02	1.24	1.24	1.24	1.02	1.02	1.24	1.24	1.24	ns
LVCMOS15_S_12	0.68	0.82	0.87	0.87	0.88	1.07	1.07	1.29	1.29	1.30	1.07	1.07	1.29	1.29	1.30	ns
LVCMOS15_S_16	0.68	0.82	0.87	0.87	0.88	1.04	1.04	1.26	1.26	1.27	1.04	1.04	1.26	1.26	1.27	ns
LVCMOS15_S_4	0.68	0.82	0.87	0.87	0.88	1.28	1.29	1.53	1.53	1.54	1.28	1.29	1.53	1.53	1.54	ns
LVCMOS15_S_8	0.68	0.82	0.87	0.87	0.88	1.11	1.11	1.34	1.34	1.34	1.11	1.11	1.34	1.34	1.34	ns
LVCMOS18_F_12	0.64	0.76	0.79	0.79	0.80	1.04	1.04	1.25	1.25	1.26	1.04	1.04	1.25	1.25	1.26	ns
LVCMOS18_F_16	0.64	0.76	0.79	0.79	0.80	1.00	1.00	1.21	1.21	1.22	1.00	1.00	1.21	1.21	1.22	ns
LVCMOS18_F_4	0.64	0.76	0.79	0.79	0.80	1.17	1.17	1.41	1.41	1.41	1.17	1.17	1.41	1.41	1.41	ns
LVCMOS18_F_8	0.64	0.76	0.79	0.79	0.80	1.10	1.10	1.33	1.33	1.33	1.10	1.10	1.33	1.33	1.33	ns
LVCMOS18_S_12	0.64	0.76	0.79	0.79	0.80	1.11	1.11	1.34	1.34	1.35	1.11	1.11	1.34	1.34	1.35	ns
LVCMOS18_S_16	0.64	0.76	0.79	0.79	0.80	1.11	1.11	1.34	1.34	1.34	1.11	1.11	1.34	1.34	1.34	ns
LVCMOS18_S_4	0.64	0.76	0.79	0.79	0.80	1.32	1.32	1.58	1.58	1.58	1.32	1.32	1.58	1.58	1.58	ns
LVCMOS18_S_8	0.64	0.76	0.79	0.79	0.80	1.18	1.18	1.38	1.38	1.38	1.18	1.18	1.38	1.38	1.38	ns
LVCMOS25_F_12	0.83	0.85	0.90	0.90	0.91	1.54	1.54	1.81	1.81	1.81	1.54	1.54	1.81	1.81	1.81	ns
LVCMOS25_F_16	0.83	0.85	0.90	0.90	0.91	1.56	1.59	1.88	1.88	1.88	1.56	1.59	1.88	1.88	1.88	ns
LVCMOS25_F_4	0.83	0.85	0.90	0.90	0.91	2.24	2.24	2.56	2.56	2.56	2.24	2.24	2.56	2.56	2.56	ns
LVCMOS25_F_8	0.83	0.85	0.90	0.90	0.91	1.67	1.67	1.95	1.95	1.95	1.67	1.67	1.95	1.95	1.95	ns
LVCMOS25_S_12	0.83	0.85	0.90	0.90	0.91	2.05	2.14	2.47	2.47	2.47	2.05	2.14	2.47	2.47	2.47	ns
LVCMOS25_S_16	0.83	0.85	0.90	0.90	0.91	1.84	1.89	2.19	2.19	2.19	1.84	1.89	2.19	2.19	2.19	ns
LVCMOS25_S_4	0.83	0.85	0.90	0.90	0.91	3.23	3.27	3.68	3.68	3.68	3.23	3.27	3.68	3.68	3.68	ns
LVCMOS25_S_8	0.83	0.85	0.90	0.90	0.91	2.11	2.15	2.47	2.47	2.47	2.11	2.15	2.47	2.47	2.47	ns

Table 27: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	
	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	
LVCMOS33_F_12	0.96	0.97	1.03	1.03	1.03	1.98	1.98	2.24	2.24	2.24	1.98	1.98	2.24	2.24	2.24	ns
LVCMOS33_F_16	0.96	0.97	1.03	1.03	1.03	1.79	1.79	2.09	2.09	2.09	1.79	1.79	2.09	2.09	2.09	ns
LVCMOS33_F_4	0.96	0.97	1.03	1.03	1.03	2.34	2.34	2.63	2.63	2.63	2.34	2.34	2.63	2.63	2.63	ns
LVCMOS33_F_8	0.96	0.97	1.03	1.03	1.03	2.05	2.05	2.32	2.32	2.33	2.05	2.05	2.32	2.32	2.33	ns
LVCMOS33_S_12	0.96	0.97	1.03	1.03	1.03	2.13	2.13	2.48	2.48	2.48	2.13	2.13	2.48	2.48	2.48	ns
LVCMOS33_S_16	0.96	0.97	1.03	1.03	1.03	2.11	2.11	2.43	2.43	2.43	2.11	2.11	2.43	2.43	2.43	ns
LVCMOS33_S_4	0.96	0.97	1.03	1.03	1.03	3.23	3.23	3.67	3.67	3.67	3.23	3.23	3.67	3.67	3.67	ns
LVCMOS33_S_8	0.96	0.97	1.03	1.03	1.03	2.28	2.28	2.55	2.55	2.55	2.66	2.67	2.78	2.78	2.78	ns
LVDS_25	0.45	0.58	0.62	0.62	0.63	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns
LVPECL	0.43	0.57	0.62	0.62	0.63	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.04	1.04	1.05	1.05	1.06	1.83	1.83	2.10	2.10	2.10	1.83	1.83	2.10	2.10	2.10	ns
LVTTL_F_16	1.04	1.04	1.05	1.05	1.06	1.79	1.79	2.06	2.06	2.06	1.79	1.79	2.06	2.06	2.06	ns
LVTTL_F_4	1.04	1.04	1.05	1.05	1.06	2.34	2.34	2.63	2.63	2.63	2.34	2.34	2.63	2.63	2.63	ns
LVTTL_F_8	1.04	1.04	1.05	1.05	1.06	1.97	1.97	2.22	2.22	2.23	1.97	1.97	2.22	2.22	2.23	ns
LVTTL_S_12	1.04	1.04	1.05	1.05	1.06	1.90	1.90	2.19	2.19	2.19	1.96	1.97	2.19	2.19	2.19	ns
LVTTL_S_16	1.04	1.04	1.05	1.05	1.06	2.07	2.07	2.40	2.40	2.40	2.07	2.07	2.40	2.40	2.40	ns
LVTTL_S_4	1.04	1.04	1.05	1.05	1.06	3.23	3.23	3.67	3.67	3.67	3.23	3.23	3.67	3.67	3.67	ns
LVTTL_S_8	1.04	1.04	1.05	1.05	1.06	2.22	2.22	2.47	2.47	2.47	2.22	2.37	2.50	2.50	2.51	ns
MINI_LVDS_25	0.45	0.58	0.62	0.62	0.63	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns
PPDS_25	0.45	0.58	0.62	0.62	0.63	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns
RSDS_25	0.45	0.58	0.62	0.62	0.63	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns
SLVS_400_25	0.45	0.58	0.62	0.62	0.63	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.52	0.55	0.59	0.59	0.59	0.72	0.72	0.91	0.91	0.91	0.83	0.83	1.04	1.04	1.04	ns
SSTL12_S	0.52	0.55	0.59	0.59	0.59	0.78	0.78	0.97	0.97	0.98	0.88	0.88	1.11	1.11	1.11	ns
SSTL135_F	0.52	0.55	0.59	0.59	0.59	0.72	0.72	0.90	0.90	0.91	0.88	0.89	1.11	1.11	1.11	ns
SSTL135_S	0.52	0.55	0.59	0.59	0.59	0.77	0.77	0.97	0.97	0.97	0.94	0.94	1.18	1.18	1.18	ns
SSTL135_R_F	0.52	0.55	0.59	0.59	0.59	0.74	0.74	0.93	0.93	0.93	0.85	0.86	1.08	1.08	1.08	ns
SSTL135_R_S	0.52	0.55	0.59	0.59	0.59	0.82	0.82	1.02	1.02	1.03	0.95	0.96	1.19	1.19	1.19	ns
SSTL15_F	0.52	0.55	0.59	0.59	0.59	0.68	0.68	0.87	0.87	0.87	0.83	0.84	1.07	1.07	1.07	ns
SSTL15_S	0.52	0.55	0.59	0.59	0.59	0.80	0.80	1.00	1.00	1.01	0.98	0.99	1.23	1.23	1.23	ns
SSTL15_R_F	0.52	0.55	0.59	0.59	0.59	0.75	0.75	0.94	0.94	0.94	0.88	0.89	1.11	1.11	1.11	ns
SSTL15_R_S	0.52	0.55	0.59	0.59	0.59	0.83	0.83	1.04	1.04	1.04	0.95	0.96	1.20	1.20	1.21	ns
SSTL18_I_F	0.52	0.55	0.59	0.59	0.59	0.76	0.76	0.96	0.96	0.96	0.94	0.95	1.21	1.21	1.21	ns
SSTL18_I_S	0.52	0.55	0.59	0.59	0.59	0.88	0.88	1.08	1.08	1.08	0.88	0.88	1.08	1.08	1.08	ns
SSTL18_II_F	0.52	0.55	0.59	0.59	0.59	0.73	0.73	0.92	0.92	0.92	0.89	0.90	1.14	1.14	1.14	ns
SSTL18_II_S	0.52	0.55	0.59	0.59	0.59	0.85	0.85	1.05	1.05	1.05	1.01	1.06	1.32	1.32	1.32	ns
SUB_LVDS	0.45	0.58	0.62	0.62	0.63	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns
TMDS_33	0.57	0.65	0.73	0.73	0.74	0.80	0.83	0.95	0.96	0.95	105.74	105.74	105.85	105.85	105.85	ns

Table 28: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	
	-3	-2	-1/-1L	-1M	-1L	-3	-2	-1/-1L	-1M	-1L	-3	-2	-1/-1L	-1M	-1L	
DIFF_HSTL_I_12_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSTL_I_12_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_12_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_HSTL_I_18_F	0.43	0.48	0.55	0.55	0.55	0.45	0.49	0.53	0.53	0.53	0.53	0.61	0.68	0.68	0.68	ns
DIFF_HSTL_I_18_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.59	0.59	0.59	0.59	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_18_S	0.43	0.48	0.55	0.55	0.55	0.56	0.62	0.67	0.67	0.67	0.67	0.77	0.86	0.86	0.86	ns
DIFF_HSTL_I_DCI_12_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSTL_I_DCI_12_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_DCI_12_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_HSTL_I_DCI_18_F	0.43	0.48	0.55	0.55	0.55	0.45	0.49	0.53	0.53	0.53	0.53	0.61	0.68	0.68	0.68	ns
DIFF_HSTL_I_DCI_18_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.59	0.59	0.59	0.59	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_DCI_18_S	0.43	0.48	0.55	0.55	0.55	0.56	0.62	0.67	0.67	0.67	0.67	0.77	0.86	0.86	0.86	ns
DIFF_HSTL_I_DCI_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSTL_I_DCI_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_DCI_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_HSTL_I_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSTL_I_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSTL_I_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_HSUL_12_DCI_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSUL_12_DCI_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSUL_12_DCI_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_HSUL_12_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_HSUL_12_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_HSUL_12_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_POD10_DCI_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.55	0.55	0.55	0.58	0.65	0.73	0.73	0.73	ns
DIFF_POD10_DCI_M	0.43	0.48	0.55	0.55	0.55	0.52	0.58	0.63	0.63	0.63	0.62	0.71	0.79	0.79	0.79	ns
DIFF_POD10_DCI_S	0.43	0.48	0.55	0.55	0.55	0.61	0.68	0.74	0.74	0.74	0.69	0.79	0.88	0.88	0.88	ns
DIFF_POD10_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.55	0.55	0.55	0.58	0.65	0.73	0.73	0.73	ns
DIFF_POD10_M	0.43	0.48	0.55	0.55	0.55	0.52	0.58	0.63	0.63	0.63	0.62	0.71	0.79	0.79	0.79	ns
DIFF_POD10_S	0.43	0.48	0.55	0.55	0.55	0.61	0.68	0.74	0.74	0.74	0.69	0.79	0.88	0.88	0.88	ns
DIFF_POD12_DCI_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.55	0.55	0.55	0.58	0.65	0.73	0.73	0.73	ns
DIFF_POD12_DCI_M	0.43	0.48	0.55	0.55	0.55	0.52	0.58	0.63	0.63	0.63	0.62	0.71	0.79	0.79	0.79	ns
DIFF_POD12_DCI_S	0.43	0.48	0.55	0.55	0.55	0.61	0.68	0.74	0.74	0.74	0.69	0.79	0.88	0.88	0.88	ns
DIFF_POD12_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.55	0.55	0.55	0.58	0.65	0.73	0.73	0.73	ns
DIFF_POD12_M	0.43	0.48	0.55	0.55	0.55	0.52	0.58	0.63	0.63	0.63	0.62	0.71	0.79	0.79	0.79	ns
DIFF_POD12_S	0.43	0.48	0.55	0.55	0.55	0.61	0.68	0.74	0.74	0.74	0.69	0.79	0.88	0.88	0.88	ns
DIFF_SSTL12_DCI_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns
DIFF_SSTL12_DCI_M	0.43	0.48	0.55	0.55	0.55	0.50	0.55	0.60	0.60	0.60	0.60	0.68	0.76	0.76	0.76	ns
DIFF_SSTL12_DCI_S	0.43	0.48	0.55	0.55	0.55	0.56	0.61	0.67	0.67	0.67	0.67	0.76	0.85	0.85	0.85	ns
DIFF_SSTL12_F	0.43	0.48	0.55	0.55	0.55	0.46	0.50	0.54	0.54	0.54	0.54	0.62	0.68	0.68	0.68	ns

Table 28: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	1.0V	0.95V			0.9V	
	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	-3	-2	-1 / -1L	-1M	-1L	
SSTL135_DCI_S	0.43	0.46	0.52	0.52	0.52	0.57	0.63	0.68	0.68	0.68	0.69	0.78	0.87	0.87	0.87	ns
SSTL135_F	0.43	0.46	0.52	0.52	0.52	0.48	0.52	0.56	0.56	0.56	0.56	0.64	0.70	0.70	0.70	ns
SSTL135_M	0.43	0.46	0.52	0.52	0.52	0.52	0.57	0.61	0.61	0.61	0.61	0.70	0.78	0.78	0.78	ns
SSTL135_S	0.43	0.46	0.52	0.52	0.52	0.57	0.63	0.68	0.68	0.68	0.69	0.78	0.87	0.87	0.87	ns
SSTL15_DCI_F	0.43	0.46	0.52	0.52	0.52	0.47	0.52	0.56	0.56	0.56	0.56	0.63	0.70	0.70	0.70	ns
SSTL15_DCI_M	0.43	0.46	0.52	0.52	0.52	0.52	0.57	0.61	0.61	0.61	0.61	0.70	0.78	0.78	0.78	ns
SSTL15_DCI_S	0.43	0.46	0.52	0.52	0.52	0.57	0.63	0.68	0.68	0.68	0.69	0.78	0.87	0.87	0.87	ns
SSTL15_F	0.43	0.46	0.52	0.52	0.52	0.47	0.52	0.56	0.56	0.56	0.56	0.63	0.70	0.70	0.70	ns
SSTL15_M	0.43	0.46	0.52	0.52	0.52	0.52	0.57	0.61	0.61	0.61	0.61	0.70	0.78	0.78	0.78	ns
SSTL15_S	0.43	0.46	0.52	0.52	0.52	0.57	0.63	0.68	0.68	0.68	0.69	0.78	0.87	0.87	0.87	ns
SSTL18_I_DCI_F	0.43	0.46	0.52	0.52	0.52	0.47	0.51	0.55	0.55	0.55	0.55	0.63	0.70	0.70	0.70	ns
SSTL18_I_DCI_M	0.43	0.46	0.52	0.52	0.52	0.52	0.57	0.61	0.61	0.61	0.61	0.70	0.78	0.78	0.78	ns
SSTL18_I_DCI_S	0.43	0.46	0.52	0.52	0.52	0.58	0.63	0.69	0.69	0.69	0.69	0.78	0.88	0.88	0.88	ns
SSTL18_I_F	0.43	0.46	0.52	0.52	0.52	0.47	0.51	0.55	0.55	0.55	0.55	0.63	0.70	0.70	0.70	ns
SSTL18_I_M	0.43	0.46	0.52	0.52	0.52	0.52	0.57	0.61	0.61	0.61	0.61	0.70	0.78	0.78	0.78	ns
SSTL18_I_S	0.43	0.46	0.52	0.52	0.52	0.58	0.63	0.69	0.69	0.69	0.69	0.78	0.88	0.88	0.88	ns
SUB_LVDS	0.42	0.46	0.51	0.51	0.51	0.57	0.67	0.72	0.72	0.72	890.24	890.26	890.28	890.28	890.28	ns

Table 29 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 29: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1 / -1L	-1L	
$T_{OUTBUF\_DELAY\_TE\_PAD}$ (1)	T input to pad high-impedance for HR I/O banks	1.37	1.52	1.69	1.69	ns
	T input to pad high-impedance for HP I/O banks	0.62	0.71	0.78	0.78	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	0.47	0.65	0.68	0.68	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.06	1.21	1.49	1.49	ns

Notes:

1. The $T_{OUTBUF\_DELAY\_TE\_PAD}$ values are applicable to single-ended I/O standards. For true differential standards, the values are larger. Use the Vivado timing report for the most accurate timing values for your configuration.

Table 31: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub series terminated logic), Class I and Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I and II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I and II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0

Table 39: **Global Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			1.0V	0.95V			0.90V	
			-3	-2	-1	-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.								
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM/PLL (far clock region)	XCKU025	N/A	6.40	7.37	N/A	N/A	ns
		XCKU035	5.84	6.73	7.64	7.64	8.09	ns
		XCKU040	5.84	6.73	7.64	7.64	8.09	ns
		XCKU060	5.94	6.84	7.91	7.91	8.22	ns
		XCKU085	5.95	6.98	8.12	8.12	8.21	ns
		XCKU095	N/A	6.67	7.69	N/A	N/A	ns
		XCKU115	5.95	6.98	8.12	8.12	8.21	ns
		XQKU040	N/A	6.73	7.75	N/A	N/A	ns
		XQKU060	N/A	6.84	7.91	N/A	N/A	ns
		XQKU095	N/A	6.67	7.69	N/A	N/A	ns
		XQKU115	N/A	6.98	8.12	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 40: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			1.0V	0.95V			0.90V	
			-3	-2	-1	-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	XCKU025	N/A	1.80	1.88	N/A	N/A	ns
		XCKU035	2.13	2.45	2.78	2.78	3.72	ns
		XCKU040	2.13	2.45	2.78	2.78	3.72	ns
		XCKU060	1.58	1.92	2.05	2.05	2.41	ns
		XCKU085	1.58	1.95	2.12	2.12	2.41	ns
		XCKU095	N/A	1.59	1.85	N/A	N/A	ns
		XCKU115	1.58	1.95	2.12	2.12	2.41	ns
		XQKU040	N/A	1.81	1.91	N/A	N/A	ns
		XQKU060	N/A	1.92	2.05	N/A	N/A	ns
		XQKU095	N/A	1.59	1.85	N/A	N/A	ns
		XQKU115	N/A	1.95	2.12	N/A	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 42 through Table 43 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 42: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade, V_{CCINT} Operating Voltage, and Temperature Range						Units
				1.0V	0.95V				0.90V	
				-3E	-2E/I	-1C/I	-1M	-1LI	-1LI	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)										
$T_{PSMMCMCC\_KU025}$	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCKU025	N/A	2.16	2.51	N/A	N/A	N/A	ns
$T_{PHMMCMCC\_KU025}$		Hold		N/A	–0.48	–0.48	N/A	N/A	N/A	ns
$T_{PSMMCMCC\_KU035}$		Setup	XCKU035	1.70	1.72	1.74	N/A	1.74	2.07	ns
$T_{PHMMCMCC\_KU035}$		Hold		–0.23	–0.23	–0.23	N/A	–0.23	–0.13	ns
$T_{PSMMCMCC\_KU040}$		Setup	XCKU040	1.70	1.72	1.74	N/A	1.74	2.07	ns
$T_{PHMMCMCC\_KU040}$		Hold		–0.23	–0.23	–0.23	N/A	–0.23	–0.13	ns
$T_{PSMMCMCC\_KU060}$		Setup	XCKU060	2.21	2.23	2.51	N/A	2.51	2.55	ns
$T_{PHMMCMCC\_KU060}$		Hold		–0.47	–0.47	–0.47	N/A	–0.47	–0.15	ns
$T_{PSMMCMCC\_KU085}$		Setup	XCKU085	2.21	2.23	2.51	N/A	2.51	2.55	ns
$T_{PHMMCMCC\_KU085}$		Hold		–0.37	–0.37	–0.37	N/A	–0.37	–0.15	ns
$T_{PSMMCMCC\_KU095}$		Setup	XCKU095	N/A	2.25	2.55	N/A	N/A	N/A	ns
$T_{PHMMCMCC\_KU095}$		Hold		N/A	–0.47	–0.47	N/A	N/A	N/A	ns
$T_{PSMMCMCC\_KU115}$		Setup	XCKU115	2.21	2.23	2.51	N/A	2.51	2.55	ns
$T_{PHMMCMCC\_KU115}$		Hold		–0.37	–0.37	–0.37	N/A	–0.37	–0.15	ns
$T_{PSMMCMCC\_KU040}$		Setup	XQKU040	N/A	2.23	2.58	2.60	N/A	N/A	ns
$T_{PHMMCMCC\_KU040}$		Hold		N/A	–0.45	–0.45	–0.45	N/A	N/A	ns
$T_{PSMMCMCC\_KU060}$		Setup	XQKU060	N/A	2.23	2.51	2.52	N/A	N/A	ns
$T_{PHMMCMCC\_KU060}$		Hold		N/A	–0.47	–0.47	–0.47	N/A	N/A	ns
$T_{PSMMCMCC\_KU095}$		Setup	XQKU095	N/A	2.25	2.55	2.56	N/A	N/A	ns
$T_{PHMMCMCC\_KU095}$		Hold		N/A	–0.47	–0.47	–0.47	N/A	N/A	ns
$T_{PSMMCMCC\_KU115}$		Setup	XQKU115	N/A	2.23	2.51	N/A	N/A	N/A	ns
$T_{PHMMCMCC\_KU115}$		Hold		N/A	–0.37	–0.37	N/A	N/A	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: **Global Clock Input Setup and Hold With PLL**

Symbol	Description		Device	Speed Grade, V_{CCINT} Operating Voltage, and Temperature Range						Units
				1.0V	0.95V				0.90V	
				-3	-2	-1	-1M	-1L	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)										
$T_{PSPLLCC\_KU025}$	Global clock input and input flip-flop (or latch) with PLL	Setup	XCKU025	N/A	–0.48	–0.48	N/A	N/A	N/A	ns
$T_{PHPLLCC\_KU025}$		Hold		N/A	2.42	2.70	N/A	N/A	N/A	ns
$T_{PSPLLCC\_KU035}$		Setup	XCKU035	0.00	0.00	0.00	N/A	0.00	0.00	ns
$T_{PHPLLCC\_KU035}$		Hold		1.36	1.59	1.79	N/A	1.79	1.79	ns
$T_{PSPLLCC\_KU040}$		Setup	XCKU040	0.00	0.00	0.00	N/A	0.00	0.00	ns
$T_{PHPLLCC\_KU040}$		Hold		1.36	1.59	1.79	N/A	1.79	1.79	ns
$T_{PSPLLCC\_KU060}$		Setup	XCKU060	–0.70	–0.70	–0.70	N/A	–0.70	–0.78	ns
$T_{PHPLLCC\_KU060}$		Hold		2.18	2.41	2.75	N/A	2.75	2.98	ns
$T_{PSPLLCC\_KU085}$		Setup	XCKU085	–0.66	–0.66	–0.66	N/A	–0.66	–0.78	ns
$T_{PHPLLCC\_KU085}$		Hold		2.18	2.46	2.83	N/A	2.83	2.98	ns
$T_{PSPLLCC\_KU095}$		Setup	XCKU095	N/A	–0.94	–0.94	N/A	N/A	N/A	ns
$T_{PHPLLCC\_KU095}$		Hold		N/A	2.36	2.71	N/A	N/A	N/A	ns
$T_{PSPLLCC\_KU115}$		Setup	XCKU115	–0.66	–0.66	–0.66	N/A	–0.66	–0.78	ns
$T_{PHPLLCC\_KU115}$		Hold		2.18	2.46	2.83	N/A	2.83	2.98	ns
$T_{PSPLLCC\_KU040}$		Setup	XQKU040	N/A	–0.67	–0.67	–0.67	N/A	N/A	ns
$T_{PHPLLCC\_KU040}$		Hold		N/A	2.48	2.83	2.84	N/A	N/A	ns
$T_{PSPLLCC\_KU060}$		Setup	XQKU060	N/A	–0.70	–0.70	–0.70	N/A	N/A	ns
$T_{PHPLLCC\_KU060}$		Hold		N/A	2.41	2.75	2.75	N/A	N/A	ns
$T_{PSPLLCC\_KU095}$		Setup	XQKU095	N/A	–0.94	–0.94	–0.94	N/A	N/A	ns
$T_{PHPLLCC\_KU095}$		Hold		N/A	2.36	2.71	2.71	N/A	N/A	ns
$T_{PSPLLCC\_KU115}$		Setup	XQKU115	N/A	–0.66	–0.66	N/A	N/A	N/A	ns
$T_{PHPLLCC\_KU115}$		Hold		N/A	2.46	2.83	N/A	N/A	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 45: **Package Skew *(Cont'd)***

Symbol	Description	Device	Package	Value	Units
PKGSKEW (*cont'd*)	Package Skew	XCKU115	FLVA1517	217	ps
			FLVD1517	143	ps
			FLVB1760	177	ps
			FLVD1924	172	ps
			FLVF1924	143	ps
			FLVA2104	184	ps
			FLVB2104	198	ps
		XQKU040	RBA676	178	ps
			RFA1156	164	ps
		XQKU060	RFA1156	170	ps
		XQKU095	RFA1156	163	ps
		XQKU115	RLD1517	147	ps
			RLF1924	146	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 49: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages								Units
			1.0V		0.95V				0.90V		
			-3E		-2E, -2I		-1C, -1I, -1M, -1LI		-1LI		
	Package Type		FF/FL	FB/SF	FF/FL RF	FB/SF RB	All Packages		All Packages		
F_{GTHMAX}	GTH maximum line rate		16.375	12.5	16.375	12.5	12.5		12.5(1)		Gb/s
F_{GTHMIN}	GTH minimum line rate		0.5	0.5	0.5	0.5	0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range(2)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range(3)	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range(4)	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. Designs must use Vivado Design Suite v2015.4.1 or later to achieve 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 50: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Devices	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	250	MHz

Table 56: **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.0L}$	Sinusoidal jitter (CPLL)(3)	4.0 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.50	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.50	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.40	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 2.0 GHz and RXOUT_DIV = 1
5. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Protocol Jitter Characteristics

For Table 58 through Table 63, the *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended settings for optimal usage of protocol specific characteristics.

Table 58: **Gigabit Ethernet Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 59: **XAUI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 60: **PCI Express Protocol Characteristics (GTH Transceivers)(1)**

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 61: **CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 62: **SFP+ Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 73: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$T_{J16.375\_QPLL}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0\_QPLL}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1\_QPLL}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.025\_QPLL}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.025\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1\_QPLL}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.8\_QPLL}$	Total jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$D_{J9.8\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J8.0\_QPLL}$	Total jitter(2)(4)	8.0 Gb/s	–	–	0.28	UI
$D_{J8.0\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Table 73: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J4.00L}$	Total jitter(3)(4)	4.00 Gb/s	–	–	0.32	UI
$D_{J4.00L}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$T_{J3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–	0.20	UI
$D_{J3.75}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.05	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four fully-populated GTY Quads at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 74: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ16.375}$	Sinusoidal jitter (CPLL)(3)	16.375 Gb/s	–	–	0.30	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (CPLL)(3)	15.0 Gb/s	–	–	0.30	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (CPLL)(3)	14.1 Gb/s	–	–	0.30	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (CPLL)(3)	13.1 Gb/s	–	–	0.30	UI
$J_{T\_SJ12.5\_QPLL}$	Sinusoidal jitter (CPLL)(3)	12.5 Gb/s	–	–	0.30	UI
$J_{T\_SJ12.5\_CPLL}$	Sinusoidal jitter (CPLL)(3)	12.5 Gb/s	–	–	0.30	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (CPLL)(3)	11.3 Gb/s	–	–	0.30	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	–	–	0.30	UI

Date	Version	Description of Revisions
05/12/2015	1.6	The minimum software requirements changed for KU040 requiring Vivado Design Suite 2015.1 v1.15 per the design advisory answer record AR64347: *Design Advisory for UltraScale Speed Specification - 2015.1 Production Speed Specification Changes*. This includes revisions to Table 20, Table 21, Table 22, Table 27, Table 28, and Table 38 to Table 43. Also, in Table 29, revised the HR I/O values for $T_{OUTBUF\_DELAY\_TE\_PAD}$ and added Note 1. Updated Table 21 and Table 22 to production release of the XCKU035 devices in the FBVA676 and FFVA1156 packages. Added Note 2 to Table 3. Clarifying edits to Table 30 and Table 31. Added Note 1 to Table 81. Updated the On-Chip Sensor Accuracy in Table 84. In Table 87, added more specifications to the STARTUPE3 Ports section.
02/24/2015	1.5	In Table 1, added I_{DC} and I_{RMS} and updates to the GTH and GTY Transceivers $I_{DCIN/OUT}$ section including adding Note 9. Added many specifications and recommended values to Table 3. Updated specifications in Table 4, Table 5, and Table 6. Added Table 7. Revised the V_{OCM} maximum for MINI_LVDS_25 and RSDS_25 in Table 12. Revised the V_{ICM} specifications in Table 14. Removed rows from Table 16 and Table 17. Removed V_{OH} and V_{OL} rows, revised the V_{OCM} maximum, and revised V_{ICM} in Table 18. Removed V_{OH} and V_{OL} rows and revised V_{ICM} in Table 19. Updated the following tables specifically addressing FBVA900 design specifications; Table 21, Table 22, Table 45, and Table 49. Removed Table 27. Updated Table 20, Table 21, Table 22, Table 27, and Table 28 with speed specifications for Vivado Design Suite 2014.4.1. Completely revised the Performance Characteristics section including adding Table 23, Table 24, and Table 25, updating Table 26 (including Note 7), and removing Table 27: *Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBV Packages)*. Added the section: I/O Standard Adjustment Measurement Methodology. Revised F_{REFCLK} in Table 33. Revised MMCM_$T_{LOCKMAX}$ in Table 36. Revised the F_{INMAX} in Table 36 and Table 37. Updated Table 44. Updated devices listed, packages listed, and package skew in Table 45. Updated $V_{CMOUTDC}$ and D_{VPPOUT} in Table 46. Added Table 48. Table 49. Added new values and descriptions to both Table 55 and Table 56. Updated the F_{DRP_CLK} in Table 81, Table 82, and Table 83. Added to F_{CORE_CLK} and $F_{USERCLK}$ Table 81. Updated On-chip reference and Note 5 in Table 84. Updated the F_{EMCCK}, F_{SCCK}, F_{MCCK}, T_{POR}, and $T_{USRCCLKO}$ specifications in Table 87.
11/14/2014	1.4	Updated Note 2 and Note 3 in Table 1 and Note 3, Note 4, and Note 6 in Table 2. Updated Note 3 in Table 6. Revised the Power-On/Off Power Supply Sequencing section. Updated the descriptions in Table 8. Removed Note 1 from both Table 26 and Table 27. Revised DDR3 specification for FBVA900 package -2I speed grade in Table 27. Updated Table 20, Table 27, and Table 28 with speed specifications for Vivado Design Suite 2014.3. Updated the descriptions in Table 37. Added a discussion on the data in the device pin-to-pin parameter tables on page 40 and page 43. Revised the values for F_{LBUS_CLK} in Table 81. Updated Note 5 in Table 84. In Table 87, added more speed specifications, updated T_{PL}, $F_{MCCKTOL}$, and F_{RBCCK}, added the *STARTUPE3 Ports* section, and added Note 1.
07/10/2014	1.3	Updated LVDCI_15 information in Table 10. Revised the SLVS_400 values in Table 12. Updated Table 20 and all the tables relevant to the latest speed specification Vivado 2014.2 v1.08. Removed RLDRAM II from Table 26 and Table 27. Also added FBV Package to Table 27. Removed $T_{DELAY\_RST\_RDY}$ from Table 33. Revised MMCM_F_{INDUTY} in Table 36 and PLL_F_{INDUTY} in Table 37. Updated the V_{IN} description in Table 46. Updated Figure 3 and Figure 4. Updated Note 1 in Table 55. Added two new sections for the Integrated Interface Block for Interlaken for the XCKU095 and XQKU095 and the Integrated Interface Block for 100G Ethernet MAC and PCS for the XCKU095 and XQKU095.