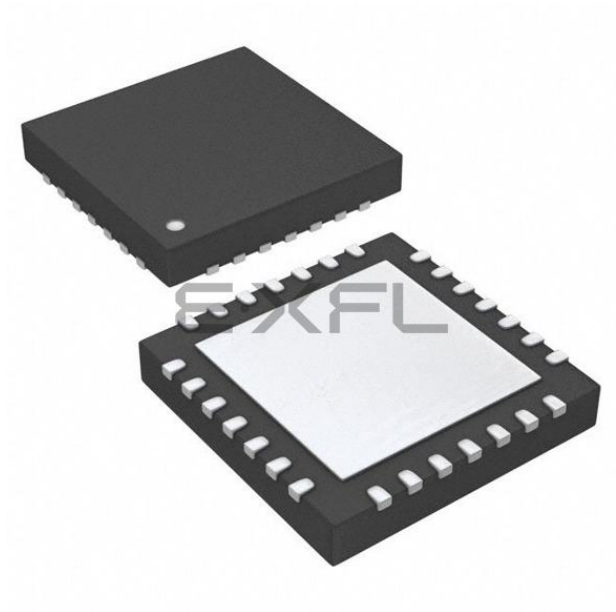
Microchip Technology - PIC32MM0064GPM028-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm028-i-ml

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RP21	—	—	—	—	14	1	I/O	ST/DIG	Remappable peripherals (input or output)
RP22	—	—	—	—	13	64	I/O	ST/DIG	
RP23	—	—	—	—	2	50	I/O	ST/DIG	
RP24	—	—	11	11	37	30	I/O	ST/DIG	
RTCC	25	22	28	31	8	58	O	DIG	Real-Time Clock/Calendar alarm/seconds output
SCK1	17	14	18	18	48	47	I/O	ST/DIG	SPI1 clock (input or output)
SCK3	24	21	27	30	13	64	I/O	ST/DIG	SPI3 clock (input or output)
SCL1	17	14	18	18	48	48	I/O	I2C	I2C1 synchronous serial clock input/output
ASCL1	19	16	21	22	5	55	I/O	I2C	Alternate I2C1 synchronous serial clock input/ output
SCL2	7	4	2	2	26	16	I/O	I2C	I2C2 synchronous serial clock input/output
SCL3	24	21	27	30	12	63	I/O	I2C	I2C3 synchronous serial clock input/output
SCLKI	12	9	10	10	36	29	I	ST	Secondary Oscillator digital clock input
SDA1	18	15	19	20	1	49	I/O	I2C	I2C1 data input/output
ASDA1	14	11	15	15	45	43	I/O	I2C	Alternate I2C1 data input/output
SDA2	6	3	1	1	25	15	I/O	I2C	I2C2 data input/output
SDA3	16	13	17	17	47	46	I/O	I2C	I2C3 data input/output
SDI1	25	22	28	31	15	31	I	ST	SPI1 data input
SDI3	16	13	17	17	14	1	I	ST	SPI3 data input
SDO1	18	15	19	20	38	34	O	DIG	SPI1 data output
SDO3	19	16	21	22	34	27	O	DIG	SPI3 data output
SOSCI	11	8	9	9	35	28	—	—	Secondary Oscillator crystal
SOSCO	12	9	10	10	36	29	—	—	Secondary Oscillator crystal
$\overline{SS1}$	26	23	29	32	16	32	I	ST	SPI1 slave select input
$\overline{SS3}$	14	11	15	15	45	22	I	ST	SPI3 slave select input
T1CK	18	15	19	20	38	34	I	ST	Timer1 external clock input
T2CK	18	15	3	3	27	19	I	ST	Timer2 external clock input
T3CK	19	16	4	4	28	20	I	ST	Timer3 external clock input
T1G	18	15	19	20	38	34	I	ST	Timer1 clock gate input
T2G	18	15	3	3	27	19	I	ST	Timer2 clock gate input
T3G	19	16	4	4	28	20	I	ST	Timer3 clock gate input
TCK	17	14	18	18	48	48	I	ST	JTAG clock input
TDI	7	4	2	2	26	16	I	ST	JTAG data input
TDO	19	16	21	22	5	55	O	DIG	JTAG data output
TMS	18	15	19	20	1	49	I	ST	JTAG mode select input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{\text{MCLR}}$.	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-Maskable Interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	_general_exception_handler
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	_general_exception_handler
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	_general_exception_handler

7.2 Interrupts

The PIC32MM0256GPM064 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS61108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_EXTERNAL_0_VECTOR	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_EXTERNAL_3_VECTOR	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
PORTD Change Notification	_CHANGE_NOTICE_D_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
RESERVED		12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
RESERVED		13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
RESERVED		14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
RESERVED		15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
RESERVED		16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	No
Timer1	_TIMER_1_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
Timer2	_TIMER_2_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer3	_TIMER_3_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
RESERVED		20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	No
RESERVED		21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	No
RESERVED		22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No
Comparator 1	_COMPARATOR_1_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Comparator 2	_COMPARATOR_2_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Comparator 3	_COMPARATOR_3_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	No

TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART2 Reception	_UART2_RX_VECTOR	56	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	57	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	58	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
UART3 Reception	_UART3_RX_VECTOR	59	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
UART3 Transmission	_UART3_TX_VECTOR	60	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
UART3 Error	_UART3_ERR_VECTOR	61	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
RESERVED		62	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	No
RESERVED		63	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	No
RESERVED		64	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	No
I2C1 Slave	_I2C1_SLAVE_VECTOR	65	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
I2C1 Master	_I2C1_MASTER_VECTOR	66	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
I2C1 Bus Collision	_I2C1_BUS_VECTOR	67	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
I2C2 Slave	_I2C2_SLAVE_VECTOR	68	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
I2C2 Master	_I2C2_MASTER_VECTOR	69	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
I2C2 Bus Collision	_I2C2_BUS_VECTOR	70	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
I2C3 Slave	_I2C3_SLAVE_VECTOR	71	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
I2C3 Master	_I2C3_MASTER_VECTOR	72	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
I2C3 Bus Collision	_I2C3_BUS_VECTOR	73	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	74	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	No
CCP1 Timer	_CCT1_VECTOR	75	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	76	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	No
CCP2 Timer	_CCT2_VECTOR	77	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	78	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	No
CCP3 Timer	_CCT3_VECTOR	79	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	No
CCP4 Input Capture or Output Compare	_CCP4_VECTOR	80	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	No
CCP4 Timer	_CCT4_VECTOR	81	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	No
CCP5 Input Capture or Output Compare	_CCP5_VECTOR	82	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	No
CCP5 Timer	_CCT5_VECTOR	83	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	No
CCP6 Input Capture or Output Compare	_CCP6_VECTOR	84	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	No
CCP6 Timer	_CCT6_VECTOR	85	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	No
CCP7 Input Capture or Output Compare	_CCP7_VECTOR	86	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	No
CCP7 Timer	_CCT7_VECTOR	87	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	No

REGISTER 8-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTRx = CHSSIZx)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTRx = CHSSIZx/2)
0 = No interrupt is pending

REGISTER 9-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>:** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 9-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Reference Oscillator Output Enable bit(1)
1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on the REFO1 pin
0 = Reference clock is not driven out on the REFO1 pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 9-6: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SRC	LOCK	POL	ORNG	ORPOL
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Self-Tune Enable bit
- 1 = FRC self-tuning is enabled; the TUNx bits are controlled by hardware
- 0 = FRC self-tuning is disabled; the TUNx bits are readable and writable

bit 14 **Reserved:** Used by debugger

bit 13 **SIDL:** FRC Self-Tune Stop in Idle bit
- 1 = Self-tuning stops during Idle mode
- 0 = Self-tuning continues during Idle mode

bit 12 **SRC:** FRC Self-Tune Reference Clock Source bit
- 1 = The USB host clock is used to tune the FRC
- 0 = The 32.768 kHz SOSC clock is used to tune the FRC

bit 11 **LOCK:** FRC Self-Tune Lock Status bit
- 1 = FRC accuracy is currently within ±0.2% of the SRC reference accuracy
- 0 = FRC accuracy may not be within ±0.2% of the SRC reference accuracy

bit 10 **POL:** FRC Self-Tune Lock Interrupt Polarity bit
- 1 = A self-tune lock interrupt is generated when LOCK is '0'
- 0 = A self-tune lock interrupt is generated when LOCK is '1'

bit 9 **ORNG:** FRC Self-Tune Out of Range Status bit
- 1 = SRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
- 0 = SRC reference clock is within the tunable range; tuning is performed

bit 8 **ORPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit
- 1 = A self-tune out of range interrupt is generated when STOR is '0'
- 0 = A self-tune out of range interrupt is generated when STOR is '1'

bit 7-6 **Unimplemented:** Read as '0'

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

10.10 I/O Ports Control Registers

TABLE 10-5: PORTA REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2BB0	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSA<13:11>(2)			—	—	—	—	ANSA6(2)	—	—	ANSA<3:0>				000F
2BC0	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA<15:0>(3)																021F
2BD0	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA<15:0>(3)																xxxx
2BE0	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA<15:0>(3)																0000
2BF0	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA<15:0>(3)																0000
2C00	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA<15:0>(3)																0000
2C10	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA<15:0>(4)																0000
2C20	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2C30	CNEN0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE0A<15:0>(3)																0000
2C40	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATA<15:0>(3)																0000
2C50	CNEN1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1A<15:0>(3)																0000
2C60	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA<15:0>(3)																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 48, 36 or 28-pin devices.

3: Bits<14:11> are not available on 48-pin devices; bits<15:10> and bits<8:5> are not available on 36-pin devices.

4: Bits<15:5> are not available on 28-pin devices.

REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer1 On bit
1 = Timer1 is enabled
0 = Timer1 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)

bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
1 = Asynchronous write to TMR1 register is in progress
0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK Pin
00 = External clock comes from the Secondary Oscillator (SOSC)

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from T2CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: The user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only available on even numbered timers (Timer2).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
	TGATE	TCKPS<2:0>			—	—	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer3 On bit
1 = Timer3 is enabled
0 = Timer3 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer3 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer3 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer3 Input Clock Prescale Select bits
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer3 Clock Source Select bit
1 = External clock is from the T3CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

REGISTER 17-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(1)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **SLPEN:** UARTx Run During Sleep Enable bit
- 1 = UARTx clock runs during Sleep
- 0 = UARTx clock is turned off during Sleep

bit 22 **ACTIVE:** UARTx Running Status bit
- 1 = UARTx is active (UxMODE register shouldn't be updated)
- 0 = UARTx is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-17 **CLKSEL:** UARTx Clock Selection bits
- 11 = The UARTx clock is the Reference Output (REFO1) clock
- 10 = The UARTx clock is the FRC oscillator clock
- 01 = The UARTx clock is the SYSCLK
- 00 = The UARTx clock is the PBCLK

bit 16 **OVFDIS:** Run During Overflow Condition Mode bit
- 1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized
- 0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx is enabled; UARTx pins are controlled by UARTx, as defined by the UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled; all UARTx pins are controlled by the corresponding bits in the PORTx, TRISx and LATx registers, UARTx power consumption is minimal

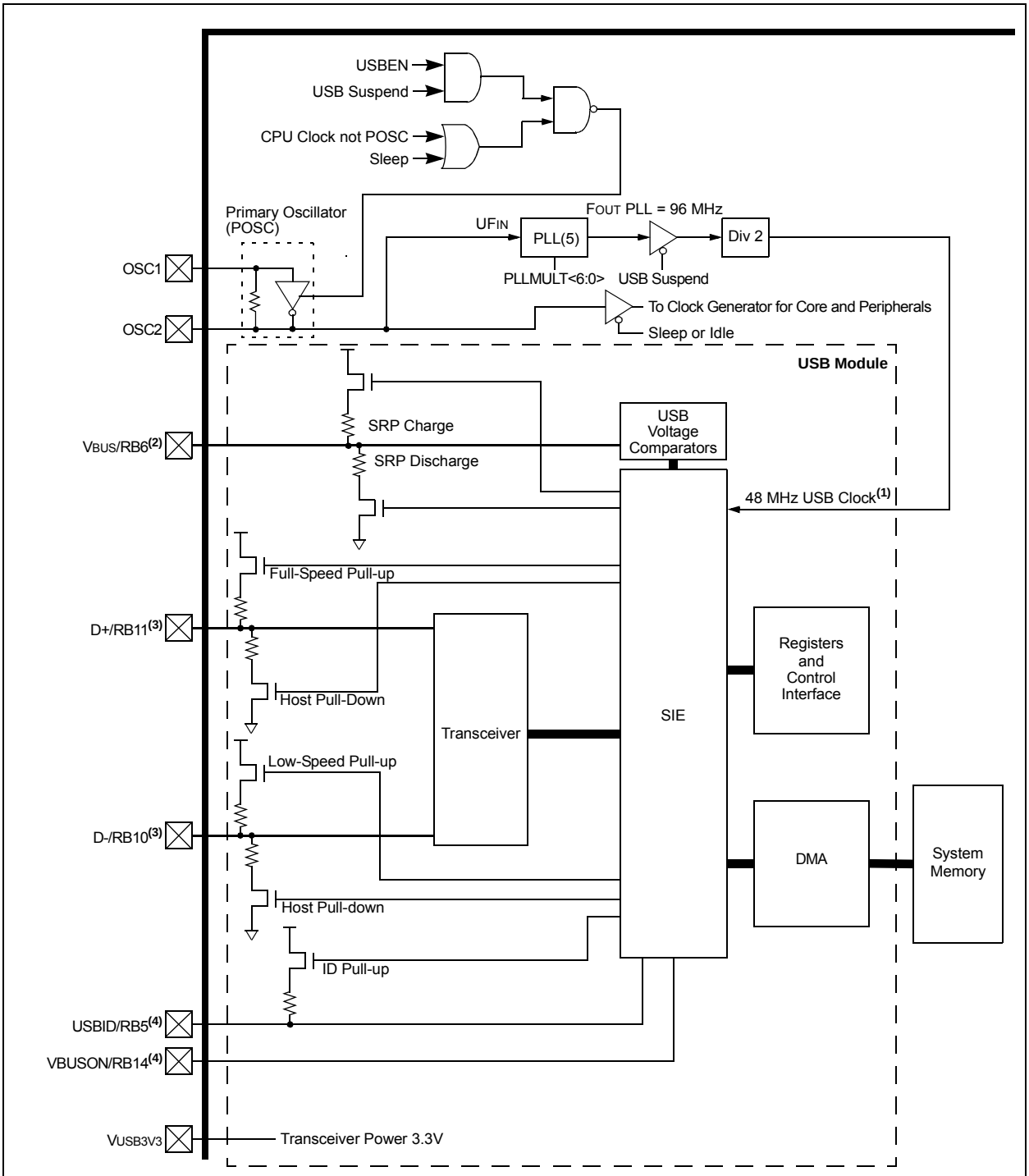
bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues operation when device enters Idle mode
- 0 = Continues operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

Note 1: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

FIGURE 18-1: PIC32MM0256GPM064 FAMILY USB INTERFACE DIAGRAM



Note 1: A 48 MHz clock is required for proper USB operation.

2: This pin can be used as a GPIO when the USB module is disabled.

3: This pin can be used as a GPIO if the USB module is disabled and powered by an external source.

4: This pin is controlled by the USB module when the module is enabled in Host or OTG mode. If the module is disabled or enabled in a mode that does not require it, this pin can be reclaimed via a device Configuration bit (refer to Register 26-1).

REGISTER 19-5: RTCDATE/ALMDATE: RTCC DATE/ALARM REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

REGISTER 23-1: DAC1CON: VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** Voltage Reference Selection bits

11111 = (DACDAT<4:0> * CVREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** Voltage Reference Output Enable bit

1 = Voltage level is output on the CVREF pin
0 = Voltage level is disconnected from the CVREF pin

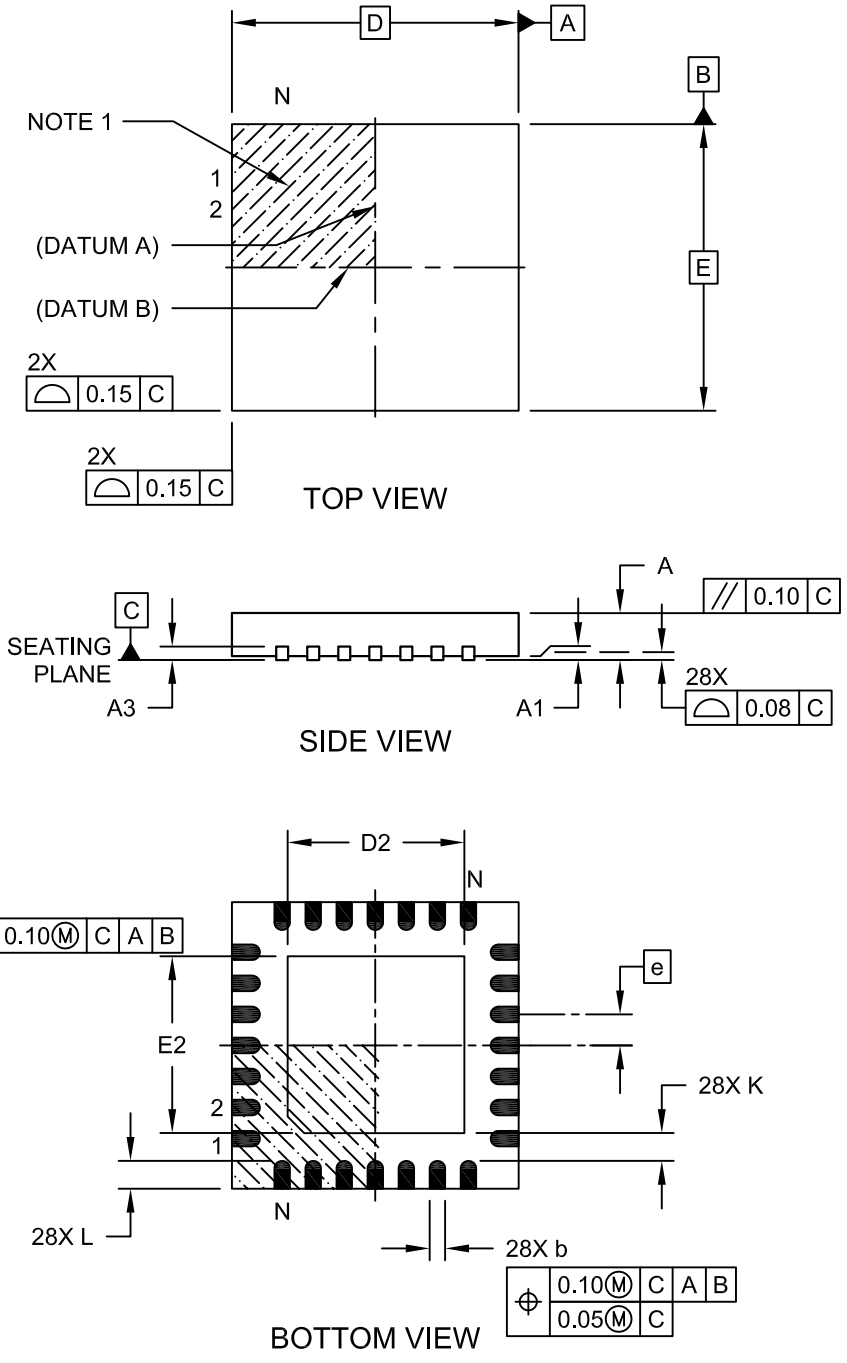
bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the CVREF+ input pin voltage
00 = No reference is selected – output is AVSS

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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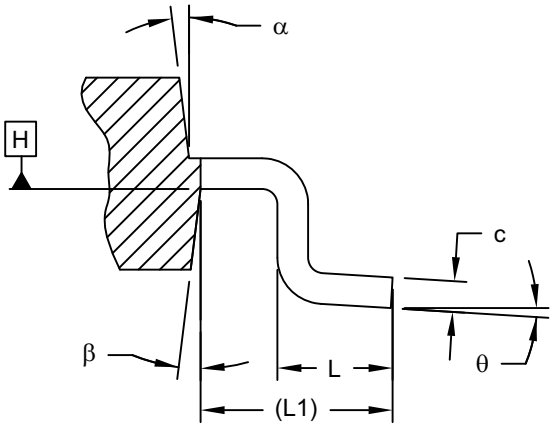
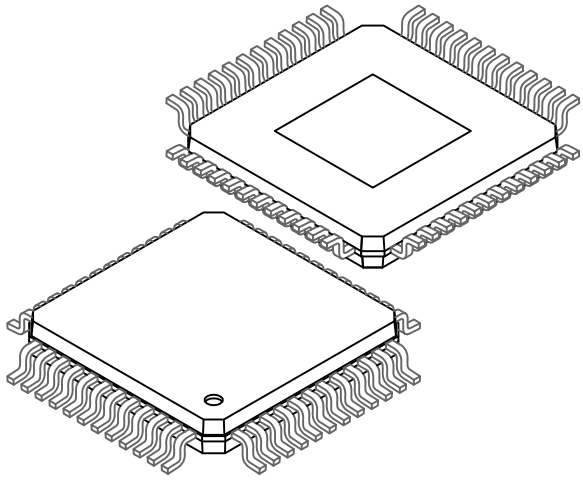
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Exposed Pad Width	E2		3.50 BSC	
Exposed Pad Length	D2		3.50 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-183A Sheet 2 of 2

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