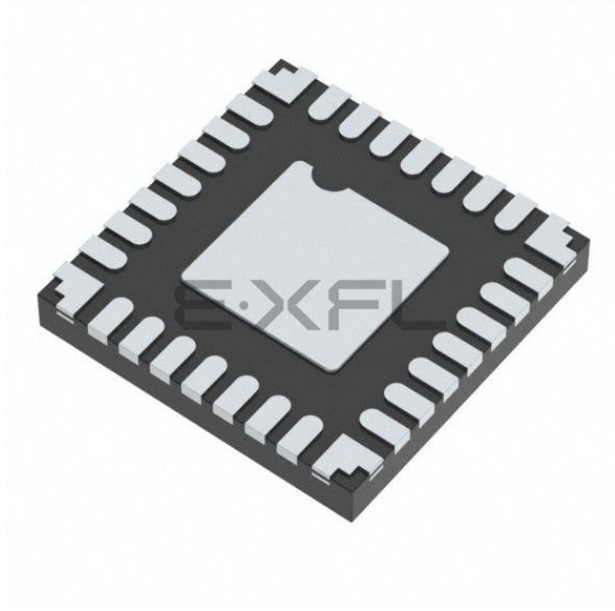
Microchip Technology - PIC32MM0064GPM028T-I/M6 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm028t-i-m6

Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I^2C	USB	Packages
							Dedicated 16-Bit Timers	UART(1)/LIN/J2602	MCCP(4)	SCCP(3)	CLC	SPI(2)/I^2S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.

2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.

3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
U1BCLK	18	15	19	20	38	34	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{\text{U1CTS}}$	17	14	18	18	48	6	I	ST	UART1 Clear-to-Send
$\overline{\text{U1RTS}}$	18	15	19	20	38	34	O	DIG	UART1 Ready-to-Send
U1RX	26	23	29	32	20	10	I	ST	UART1 receive data input
U1TX	25	22	28	31	44	40	O	DIG	UART1 transmit data output
USBID	14	11	15	15	45	43	I	ST	USB OTG ID (OTG mode only)
USBOEN	19	16	21	22	5	55	O	—	USB transceiver output enable flag
VBUSON	25	22	28	31	15	2	O	—	USB host and On-The-Go (OTG) bus power control output
VBUS	15	12	16	16	46	44	P	—	USB VBUS connection (5V nominal)
VUSB3V3	23	20	26	29	11	62	P	—	USB transceiver power input (3.3V nominal)
VCAP	20	17	22	24	7	56	P	—	Core voltage regulator filter capacitor connection
VDD	13,28	10,25	13,23,31	13,26, 34	18,30, 43	17,23, 39,57	P	—	Digital modules power supply
VREF-	3	28	34	37	22	12	I	ANA	Analog-to-Digital Converter negative reference
VREF+	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter positive reference
VSS	8,27	5,24	6,12,30	6,12,33	6,17,31, 42	18,24, 38	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

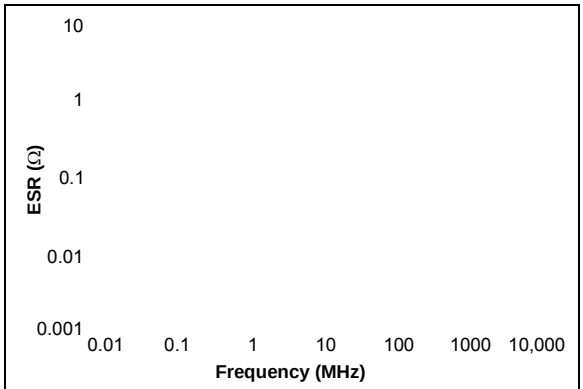
2.4 Voltage Regulator Pin (VCAP)

A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM319R61C106KE15D	10 µF	±10%	16V	-55 to +85ºC

REGISTER 8-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** DMA Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

REGISTER 8-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

REGISTER 8-14: DCHxSPTR: DMA CHANNEL x SOURCE POINTER REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to Byte 65,535 of the source

•

•

•

0000000000000001 = Points to Byte 1 of the source

0000000000000000 = Points to Byte 0 of the source

Note 1: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 8-15: DCHxDPTR: DMA CHANNEL x DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to Byte 65,535 of the destination

•

•

•

0000000000000001 = Points to Byte 1 of the destination

0000000000000000 = Points to Byte 0 of the destination

9.3 FRC Active Clock Tuning

PIC32MM0256GPM064 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"* regarding full-speed USB devices.

Note:	The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the ON bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the SRC bit (OSCTUN<12>). When SRC = 1, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When SRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	To use the USB as a reference clock tuning source (SRC = 1), the microcontroller must be configured for USB device operation and connected to a non-suspended USB host or hub port. If the SOSC is to be used as the reference clock tuning source (SRC = 0), the SOSC must also be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference, by greater than 0.2% in either direction, or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The LOCK and ORNG status bits (OSCTUN<11,9>) are used to indicate these conditions.

The POL and ORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the LOCK and ORNG bits to determine the exact cause of the interrupt.

Note:	The POL and ORPOL bits should be ignored when the self-tune system is disabled (ON = 0).

Note:	After exiting out of self-tune, 6 writes may be required to update the TUN<5:0> bits.

REGISTER 9-6: OSCTUN: FRC TUNING REGISTER (CONTINUED)

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency – 1.50%
100001 =
•
•
•
111111 =
000000 = Center frequency; oscillator runs at a nominal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency + 1.453%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note:	Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

TABLE 10-6: PORTB REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2CB0	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSB<13:11>(2)			—	—	—	—	ANSB6(2)	—	ANSB<4:0>					E01F
2CC0	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB<15:0>																FFFF
2CD0	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB<15:0>																0000
2CE0	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB<15:0>																0000
2CF0	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB<15:0>																0000
2D00	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB<15:0>																0000
2D10	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB<15:0>																0000
2D20	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2D30	CNEN0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE0B<15:0>																0000
2D40	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATB<15:0>																0000
2D50	CNEN1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1B<15:0>																0000
2D60	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: The ANSB<13:11> and ANSB6 bits are not available on 48, 36 or 28-pin devices.

REGISTER 13-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to the upper 16 bits of this register address using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
On Reset, this bit is set to the inverse of the value of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

REGISTER 14-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1
Auto-shutdown is controlled by CLC2 for MCCP2
Auto-shutdown is controlled by CLC3 for MCCP3
Auto-shutdown is controlled by CLC1 for SCCP4
Auto-shutdown is controlled by CLC2 for SCCP5
Auto-shutdown is controlled by CLC3 for SCCP6
Auto-shutdown is controlled by CLC4 for SCCP7
Auto-shutdown is controlled by CLC1 for SCCP8
Auto-shutdown is controlled by CLC2 for SCCP9
xxx1 xxxx = Auto-shutdown is controlled by the SCCP4 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP1 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx 1xxx = Auto-shutdown is controlled by the SCCP5 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP2 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx x1xx = Auto-shutdown is controlled by Comparator 3
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.
2: This pin is remappable from SCCP modules.

REGISTER 18-11: U1CON: USB CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	JSTATE	SE0	PKTDIS(4) / TOKBUSY(1,5)	USBRST	HOSTEN(2)	RESUME(3)	PPBRST	USBEN(4) / SOFEN(5)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE Flag bit
- 1 = JSTATE was detected on the USB
- 0 = JSTATE was not detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
- 1 = Single-ended zero was detected on the USB
- 0 = Single-ended zero was not detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
- 1 = Token and packet processing are disabled (set upon SETUP token received)
- 0 = Token and packet processing are enabled

TOKBUSY: Token Busy Indicator bit(1,5)
- 1 = Token is being executed by the USB module
- 0 = No token is being executed

bit 4 **USBRST:** Module Reset bit
- 1 = USB Reset is generated
- 0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
- 1 = USB host capability is enabled
- 0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit(3)
- 1 = Resume signaling is activated
- 0 = Resume signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 18-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the Resume signaling when this bit is cleared.

4: Device mode.

5: Host mode.

REGISTER 18-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
- 1 = Eye pattern test is enabled
- 0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
- 1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
- 0 = $\overline{OE}$ signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** USB Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 3 **LSDEV:** USB Low-Speed Device Enable bit
- 1 = USB macro operates in Low-Speed Device Only mode
- 0 = USB macro operates in OTG, Host or Fast Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
- 1 = USB module automatically suspends upon entry to Sleep mode; see the USUSPEND bit (U1PWRC<1>) in Register 18-5
- 0 = USB module does not automatically suspend upon entry to Sleep mode; software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

REGISTER 20-6: AD1CSS: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	—	CSS<30:27>				—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CSS<19:16>(1,2,3)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-27 **CSS<30:27>:** ADC Input Pin Scan Selection bits
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

bit 26-20 **Unimplemented:** Read as '0'

bit 19-0 **CSS<19:0>:** ADC Input Pin Scan Selection bits(1,2,3)
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

Note 1: The CSS<19:12> bits are not implemented in 28-pin devices
2: The CSS<19:15> bits are not implemented in 36-pin and 40-pin devices
3: The CSS<17:14> bits are not implemented in 48-pin devices

REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER (CONTINUED)

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin and compared with 1.2V band gap)
1110 = VDD trip point is between 2.00V and 2.22V
1101 = VDD trip point is between 2.08V and 2.33V
1100 = VDD trip point is between 2.15V and 2.44V
1011 = VDD trip point is between 2.25V and 2.55V
1010 = VDD trip point is between 2.35V and 2.69V
1001 = VDD trip point is between 2.45V and 2.80V
1000 = VDD trip point is between 2.65V and 2.98V
0111 = VDD trip point is between 2.75V and 3.09V
0110 = VDD trip point is between 2.95V and 3.30V
0101 = VDD trip point is between 3.25V and 3.63V
0100-0000 = Reserved; do not use.

25.6 On-Chip Voltage Regulator Low-Power Modes

The main on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode on its own whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (PWRCON<0>). Clearing the VREGS bit enables Standby mode.

Note 1: The SYSKEY register is used to unlock the PWRCON register.

When in Sleep mode, PIC32MM0256GPM064 family devices may use a separate low-power, low-voltage/ retention regulator to power critical circuits. This regulator, which operates at 1.2V nominal, maintains power to data RAM, WDT, Timer1 and the RTCC, while all other core digital logic is powered down. The low-voltage/ retention regulator is only available when Sleep mode is invoked. It is controlled by the RETVR Configuration bit (FPOR<2>) and in firmware by the RETEN bit (PWRCON<1>). RETVR must be programmed to zero (= 0) and the RETEN bit must be set (= 1) for the regulator to be enabled. When the retention regulator is enabled, the main regulator is off and does not consume power.

Note 1: When using the low-voltage/retention regulator, VREGS (PWRCON<0>) must be set to '1'.

The main voltage regulator takes approximately 10 µS to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after standby (VREGS bit = 0) or retention (RETEN bit = 1, RETVR bit = 0) modes. The TVREG specification is listed in Table 29-12.

25.7 Low-Power Brown-out Reset

The PIC32MM0256GPM064 family devices have a second low-power Brown-out Reset circuit with a reduced trip point precision. This low-power BOR circuit can be activated when the main BOR is disabled. It can be done by programming the LPBOREN Configuration bit (FPOR<3>) to one.

REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

bit 6-5 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Watchdog Timer window size is 25%
10 = Watchdog Timer window size is 37.5%
01 = Watchdog Timer window size is 50%
00 = Watchdog Timer window size is 75%

bit 4-0 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

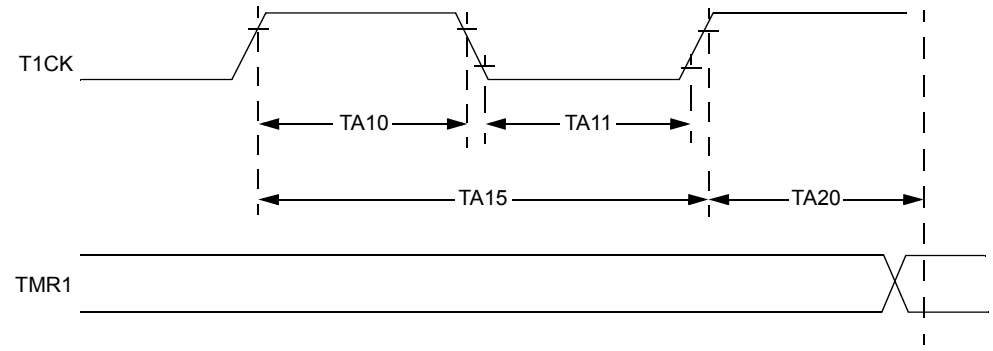
TABLE 29-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	VBG	Internal Band Gap Reference	—	1.2	—	V	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Series Resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, RETVR (FPOR<2>) = 0

TABLE 29-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0101	3.25	—	3.63	V	
			HLVDL<3:0> = 0110	2.95	—	3.30	V	
			HLVDL<3:0> = 0111	2.75	—	3.09	V	
			HLVDL<3:0> = 1000	2.65	—	2.98	V	
			HLVDL<3:0> = 1001	2.45	—	2.80	V	
			HLVDL<3:0> = 1010	2.35	—	2.69	V	
			HLVDL<3:0> = 1011	2.25	—	2.55	V	
			HLVDL<3:0> = 1100	2.15	—	2.44	V	
			HLVDL<3:0> = 1101	2.08	—	2.33	V	
			HLVDL<3:0> = 1110	2.00	—	2.22	V	
DC101	VTHL	HLVD Voltage on LVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.2	—	V	

FIGURE 29-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTxH	T1CK High Time	Synchronous, with Prescaler	[(12.5 ns or 1 TPBCLK)/N] + 20 ns	—	—	ns	Must also meet Parameter TA15(2)
			Asynchronous, with Prescaler	10	—	—	ns	
TA11	TTxL	T1CK Low Time	Synchronous, with Prescaler	[(12.5 ns or 1 TPBCLK)/N] + 20 ns	—	—	ns	Must also meet Parameter TA15(2)
			Asynchronous, with Prescaler	10	—	—	ns	
TA15	TTxP	T1CK Input Period	Synchronous, with Prescaler	[(Greater of 20 ns or 2 TPBCLK)/N] + 30 ns	—	—	ns	VDD > 2.0V(2)
				[(Greater of 20 ns or 2 TPBCLK)/N] + 50 ns	—	—	ns	VDD < 2.0V(2)
			Asynchronous, with Prescaler	20	—	—	ns	VDD > 2.0V
				50	—	—	ns	VDD < 2.0V
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		—		1	TPBCLK	

Note 1: This parameter is characterized but not tested in manufacturing.

2: N = Prescale Value (1, 8, 64, 256).