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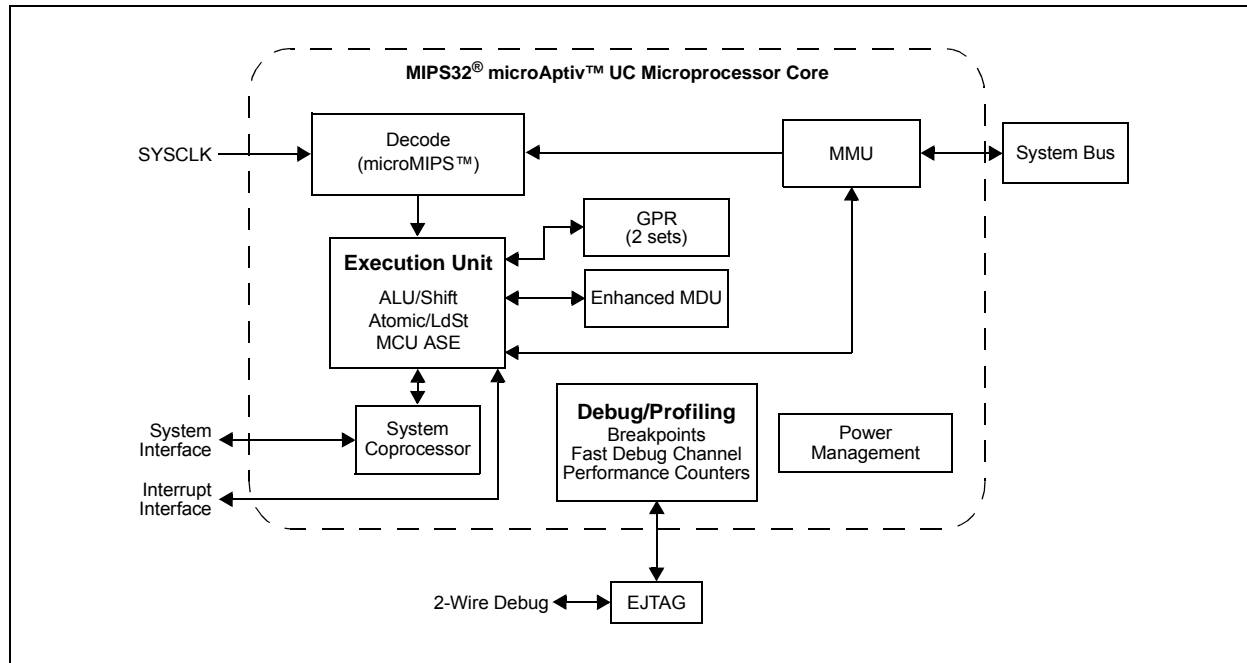
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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm028t-i-ml

PIC32MM0256GPM064 FAMILY

FIGURE 3-1: PIC32MM0256GPM064 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



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TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-3	Reserved	Reserved in the microAptiv™ UC.
4	UserLocal	User information that can be written by privileged software and read via RDHWR Register 29.
5-6	Reserved	Reserved in the microAptiv UC.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-Privileged mode.
8	BadVAddr ⁽¹⁾	Reports the address for the most recent address related exception.
9	Count ⁽¹⁾	Processor cycle count.
10	Reserved	Reserved in the microAptiv UC.
11	Compare ⁽¹⁾	Timer interrupt control.
12	Status/ IntCtl/ SRSCtl/ SRSTMap1/ View_IPL/ SRSTMAP2	Processor status and control; interrupt control and shadow set control.
13	Cause ⁽¹⁾ / View_RIPL	Cause of last exception.
14	EPC ⁽¹⁾	Program Counter at last exception.
15	PRId/ EBase/ CDMMBase	Processor identification and revision; exception base address; Common Device Memory Map Base register.
16	CONFIG/ CONFIG1/ CONFIG2/ CONFIG3/ CONFIG7	Configuration registers.
7-22	Reserved	Reserved in the microAptiv UC.
23	Debug/ Debug2/ TraceControl/ TraceControl2/ UserTraceData1/ TraceBPC ⁽²⁾	EJTAG Debug register. EJTAG Debug Register 2. EJTAG Trace Control register. EJTAG Trace Control Register 2. EJTAG User Trace Data 1 register. EJTAG Trace Breakpoint register.
24	DEPC ⁽²⁾ / UserTraceData2	Program Counter at last debug exception. EJTAG User Trace Data 2 register.
25	PerfCtl0/ PerfCnt0/ PerfCtl1/ PerfCnt1	Performance Counter 0 control. Performance Counter 0. Performance Counter 1 control. Performance Counter 1.
26	ErrCtl	Software parity check enable.
27	CacheErr	Records information about SRAM parity errors.
28-29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC ⁽¹⁾	Program Counter at last error.
31	DeSAVE ⁽²⁾	Debug Handler Scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used in debug.

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REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	r-0
	—	K23<2:0>			KU<2:0> ⁽¹⁾			—
23:16	r-0	R-0	R-1	R-0	r-0	r-0	r-0	R-1
	—	UDI	SB	MDU	—	—	—	DS
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-1
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	r-0	r-0	r-0	r-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit
R = Readable bit	W = Writable bit
-n = Value at POR	U = Unimplemented bit, read as '0'
	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the CONFIG1 register

bit 30-28 **K23<2:0>:** Cacheability of the kseg2 and kseg3 Segments bits

010 = Cache is not implemented

bit 27-25 **KU<2:0>:** Cacheability of the kuseg and useg Segments bits⁽¹⁾

010 = Cache is not implemented

bit 24-23 **Reserved:** Must be written as zeros; returns zeros on reads

bit 22 **UDI:** User-Defined bit

0 = CorExtend user-defined instructions are not implemented

bit 21 **SB:** SimpleBE bit

1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit

0 = Fast, high-performance MDU

bit 19-17 **Reserved:** Must be written as zeros; returns zeros on reads

bit 16 **DS:** Dual SRAM Interface bit

1 = Dual instruction/data SRAM interface

bit 15 **BE:** Endian Mode bit

0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits

00 = MIPS32®

bit 12-10 **AR<2:0>:** Architecture Revision Level bits

001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits

011 = Fixed mapping

bit 6-3 **Reserved:** Must be written as zeros; returns zeros on reads

bit 2-0 **K0<2:0>:** kseg0 Coherency Algorithm bits

010 = Cache is not implemented

Note 1: The KU<2:0> bits are not usable as this device does not support User mode.

8.1 DMA Control Registers

TABLE 8-1: DMA CONTROLLER REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8900	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
8910	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>			0000
8920	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000
8930	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
8940	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
8950	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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REGISTER 8-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHP DAT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHP DAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:

Data to be matched must be stored in this register to allow terminate on match.

All Other modes:

Unused.

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REGISTER 9-2: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-y	r-0	U-0	U-0	U-0	U-0	U-0	U-0
	PLLICK	—	—	—	—	—	—	—

Legend:	r = Reserved bit	y = Values set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = PLL divide-by-256
110 = PLL divide-by-64
101 = PLL divide-by-32
100 = PLL divide-by-16
011 = PLL divide-by-8
010 = PLL divide-by-4
001 = PLL divide-by-2
000 = PLL divide-by-1 (default setting)

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

111111-0000111 = Reserved
0000110 = 24x
0000101 = 12x
0000100 = 8x
0000011 = 6x
0000010 = 4x
0000001 = 3x (default setting)
0000000 = 2x

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PLLICK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the system PLL (not divided)
0 = POSC is selected as the input to the system PLL; the POR default value is specified by the PLLSRC bit
The POR default value is specified by the PLLSRC Configuration bit in the FOSCSEL register. Refer to Register 26-9 in **Section 26.0 “Special Features”** for more information.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 26.4 “System Registers Write Protection”** for details.

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REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER (CONTINUED)

- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Selection bit
 When TCS = 1:
 1 = External clock input is synchronized
 0 = External clock input is not synchronized
 When TCS = 0:
 This bit is ignored.
- bit 1 **TCS:** Timer1 Clock Source Select bit
 1 = External clock is defined by the TECS<1:0> bits
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

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REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER (CONTINUED)

- bit 3 **T32:** 32-Bit Timer Mode Select bit⁽²⁾
 1 = Odd numbered and even numbered timers form a 32-bit timer
 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽³⁾
 1 = External clock from T2CK pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

- Note 1:** The user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit is only available on even numbered timers (Timer2).
- 3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1). All timer functions are set through the even numbered timers.
- 4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

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REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
15:8	U-0	U-0	U-0	U-0	U-0	R/C-0	U-0	U-0
	—	—	—	—	—	ICGARM ⁽¹⁾	—	—
7:0	R-0	W1-0	W1-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE

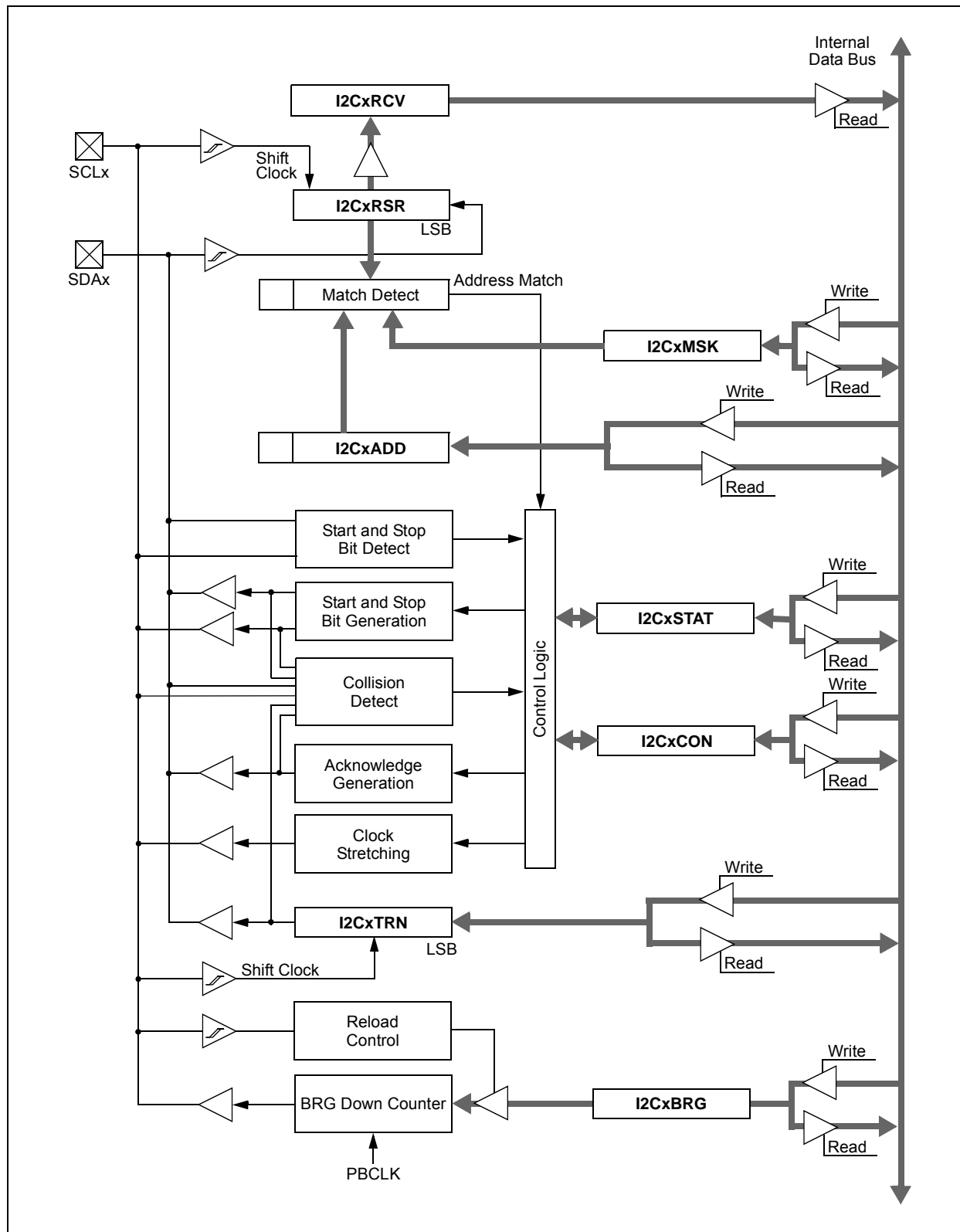
Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

- bit 31-21 **Unimplemented:** Read as '0'
- bit 20 **PRLWIP:** CCPxPRL Write in Progress Status bit
 1 = An update to the CCPxPRL register with the buffered contents is in progress
 0 = An update to the CCPxPRL register is not in progress
- bit 19 **TMRHWIP:** CCPxTMRH Write in Progress Status bit
 1 = An update to the CCPxTMRH register with the buffered contents is in progress
 0 = An update to the CCPxTMRH register is not in progress
- bit 18 **TMRLWIP:** CCPxTMRL Write in Progress Status bit
 1 = An update to the CCPxTMRL register with the buffered contents is in progress
 0 = An update to the CCPxTMRL register is not in progress
- bit 17 **RBWIP:** CCPxRB Write in Progress Status bit
 1 = An update to the CCPxRB register with the buffered contents is in progress
 0 = An update to the CCPxRB register is not in progress
- bit 16 **RAWIP:** CCPxRA Write in Progress Status bit
 1 = An update to the CCPxRA register with the buffered contents is in progress
 0 = An update to the CCPxRA register is not in progress
- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **ICGARM:** Input Capture Gate Arm bit⁽¹⁾
 A write of '1' to this location will arm the input capture gating logic for a one-shot gate event when ICGSM<1:0> = 01 or 10. The bit location reads as '0'.
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **CCPTRIG:** CCPx Trigger Status bit
 1 = Timer has been triggered and is running (set by hardware or writing to TRSET)
 0 = Timer has not been triggered and is held in Reset (cleared by writing to TRCLR)
- bit 6 **TRSET:** CCPx Trigger Set Request bit
 Write '1' to this location to trigger the timer when TRIGEN = 1 (location always reads '0').
- bit 5 **TRCLR:** CCPx Trigger Clear Request bit
 Write '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads '0').
- bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit
 1 = A shutdown event is in progress; CCPx outputs are in the shutdown state
 0 = CCPx outputs operate normally

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

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FIGURE 16-1: I2Cx BLOCK DIAGRAM



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18.5 Control Registers

REGISTER 18-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to Clear bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit

- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit

- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit

- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit

- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit

- 1 = Change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit

- 1 = Change on the session valid input was detected
- 0 = No change on the session valid input was detected

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REGISTER 18-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-Bit Frame Number Lower bits

These register bits are updated with the current frame number whenever a SOF token is received.

REGISTER 18-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 Bits of the Frame Numbers bits

These register bits are updated with the current frame number whenever a SOF token is received.

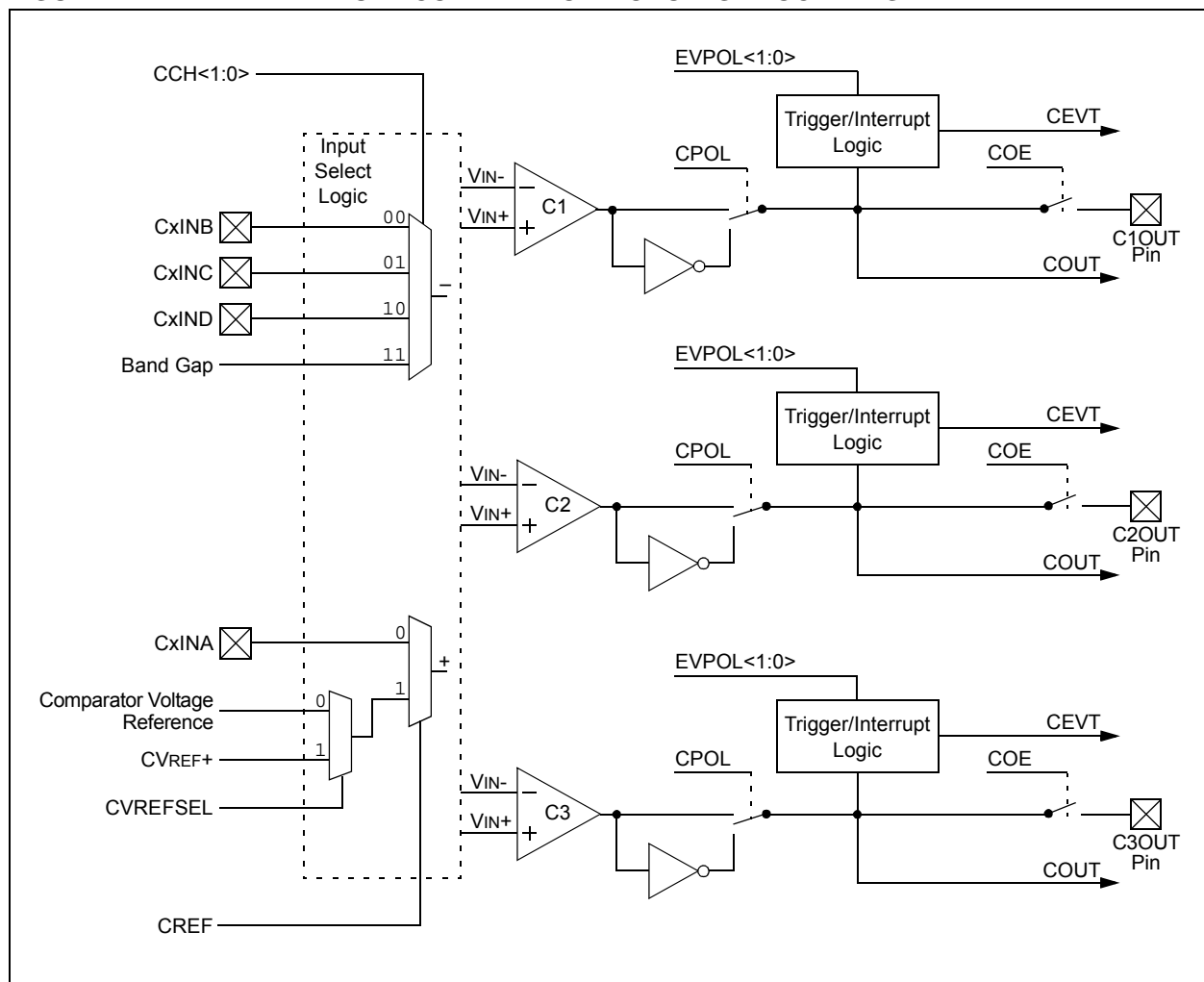
22.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and CVREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals ‘1’, the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module is shown in Figure 22-1. Each comparator has its own control register, CMxCON (Register 22-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 22-1).

FIGURE 22-1: THREE DUAL COMPARATOR MODULES BLOCK DIAGRAM



26.9 Configuration Word Registers

TABLE 26-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30\14	29\13	28\12	27\11	26\10	25\9	24\8	23\7	22\6	21\5	20\4	19\3	18\2	17\1	16\0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	FVBUSIO	FUSBIDIO	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ALT2C	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>			SWDTPS<4:0>			
17D4	FOSCSSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>			SOSCSSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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NOTES:

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FIGURE 29-4: CLKO AND I/O TIMING CHARACTERISTICS

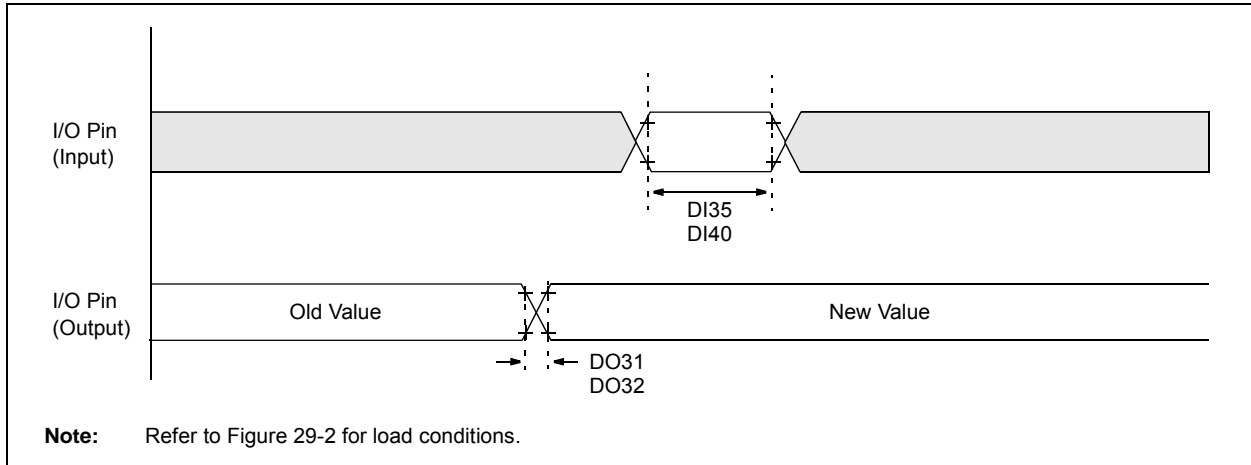


TABLE 29-22: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	
DO32	TioF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	Tcy	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	Tcy	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

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FIGURE 29-15: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

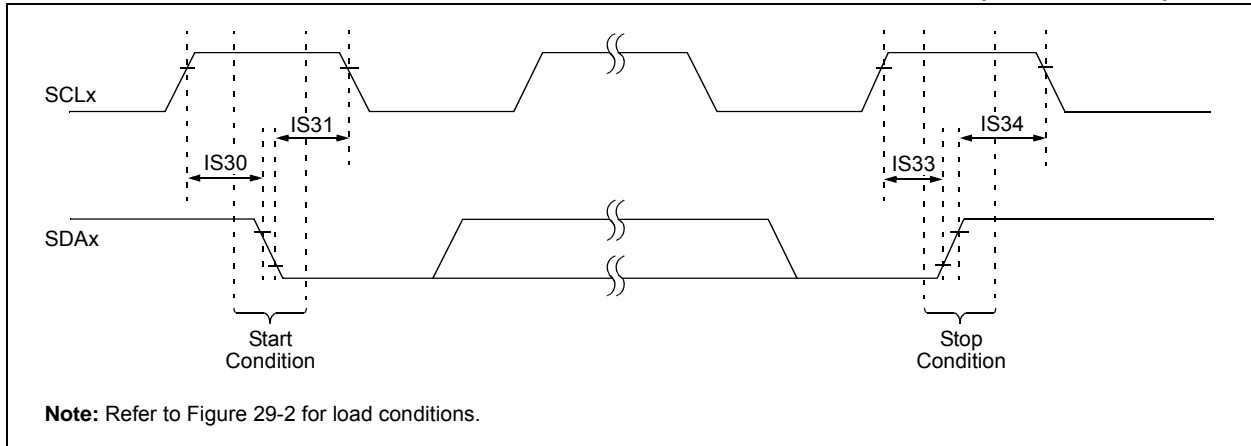


FIGURE 29-16: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

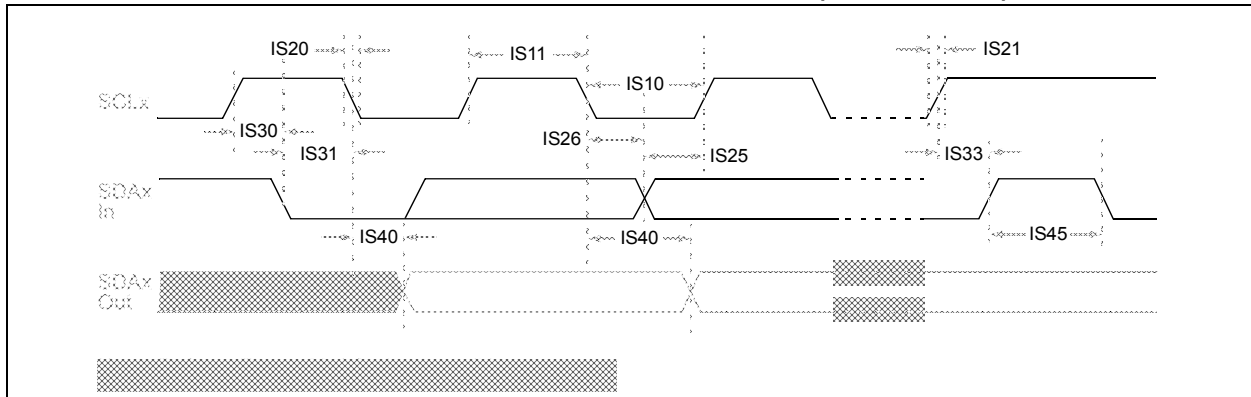


TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)			
				Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	

Note 1: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

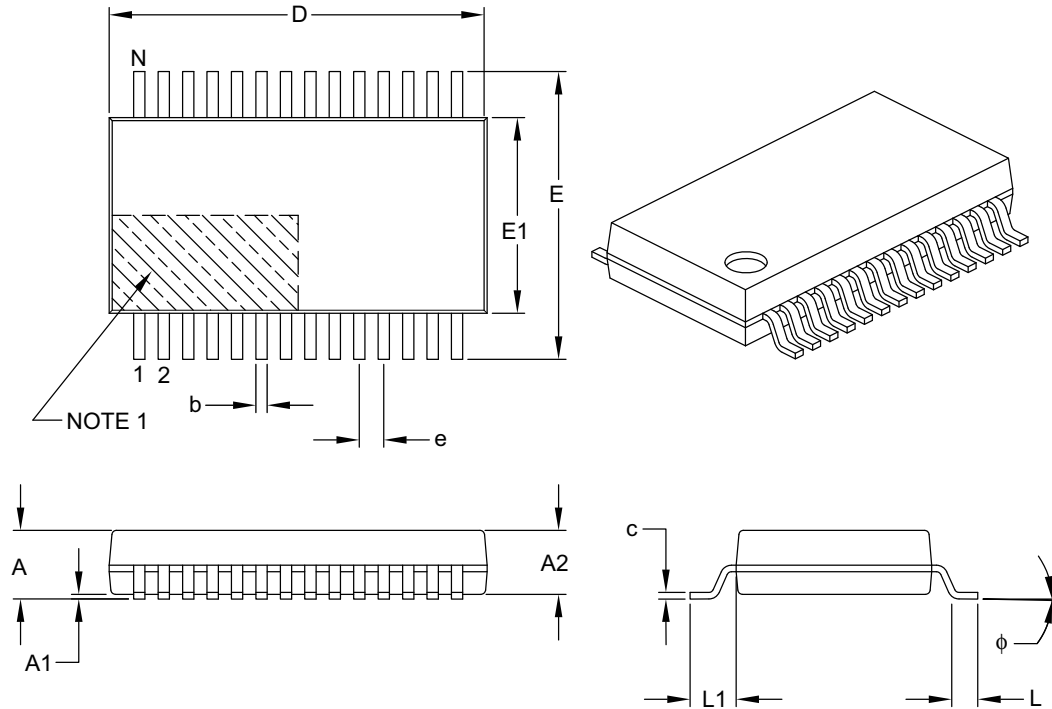
PIC32MM0256GPM064 FAMILY

30.2 Package Details

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

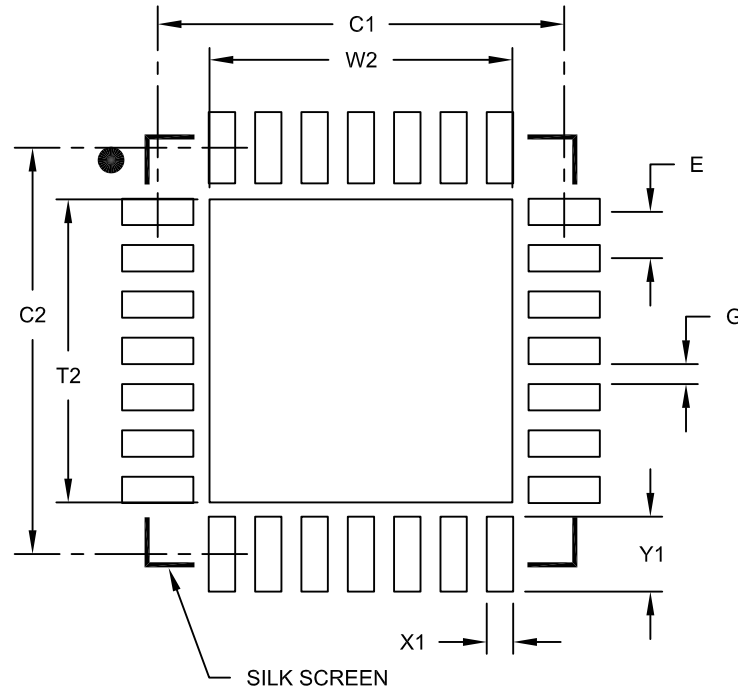
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC32MM0256GPM064 FAMILY

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

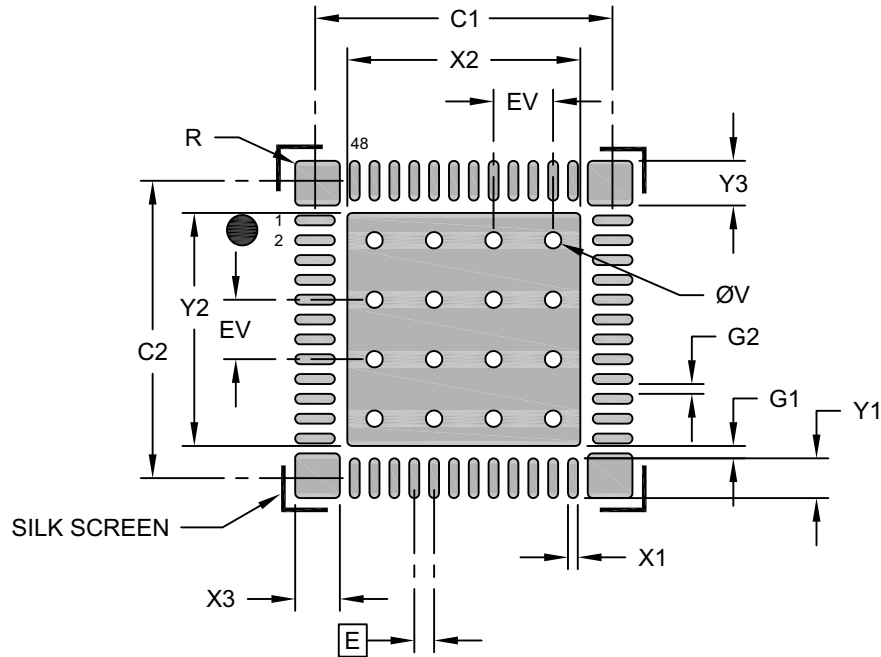
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC32MM0256GPM064 FAMILY

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Center Pad Width	X2			4.70
Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.80
Corner Anchor Pad Width (X4)	X3			0.90
Corner Anchor Pad Length (X4)	Y3			0.90
Pad Corner Radius (X 20)	R			0.10
Contact Pad to Center Pad (X48)	G1	0.25		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2442A-M4