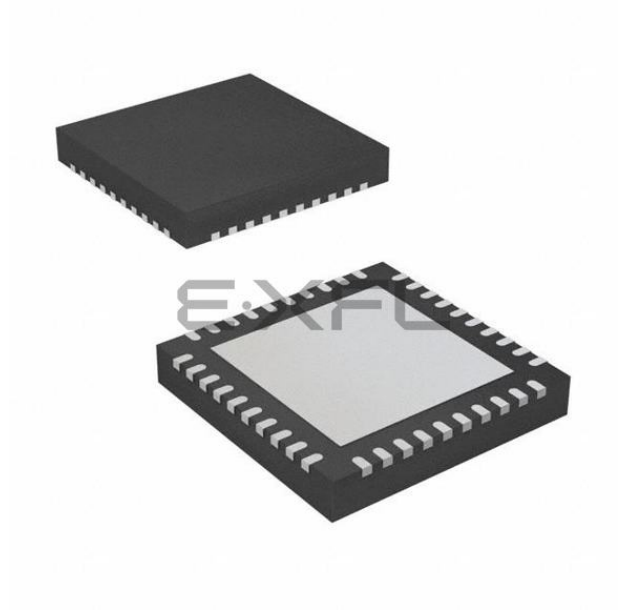
# Microchip Technology - PIC32MM0064GPM036-I/MV Datasheet



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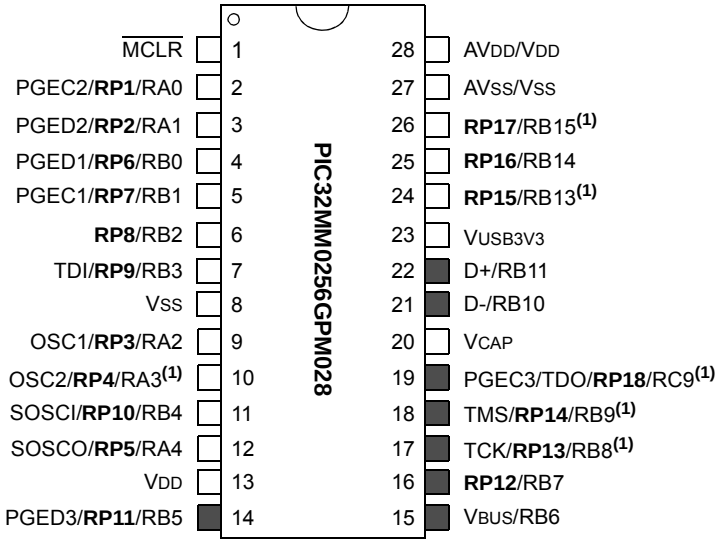
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 15x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-UFQFN Exposed Pad |
| Supplier Device Package | 40-UQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm036-i-mv |

## Pin Diagrams

### 28-Pin SSOP




**Legend:** Shaded pins are up to 5V tolerant.
**Note 1:** High drive strength pin.

**TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SSOP DEVICES**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | MCLR | 15 | VBUS/RB6 |
| 2 | PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0 | 16 | **RP12**/SDA3/SDI3/OCM3F/RB7 |
| 3 | PGED2/VREF-/AN1/**RP2**/OCM1F/RA1 | 17 | TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1) |
| 4 | PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0 | 18 | TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1) |
| 5 | PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1 | 19 | PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1) |
| 6 | AN4/C1INB/**RP8**/SDA2/OCM2E/RB2 | 20 | VCAP |
| 7 | TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3 | 21 | D-/RB10 |
| 8 | VSS | 22 | D+/RB11 |
| 9 | OSC1/CLKI/AN5/**RP3**/OCM1C/RA2 | 23 | VUSB3V3 |
| 10 | OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1) | 24 | AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1) |
| 11 | SOSCI/AN7/**RP10**/OCM3C/RB4 | 25 | CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14 |
| 12 | SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4 | 26 | AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1) |
| 13 | VDD | 27 | AVSS/VSS |
| 14 | PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5 | 28 | AVDD/VDD |

**Note 1:** High drive strength pin.
**2:** Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

## 7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS61108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0256GPM064 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The PIC32MM0256GPM064 family device interrupt module includes the following features:

- Single Vector or Multivector Mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for Each Vector
- Four User-Selectable Subpriority Levels within Each Priority
- One Shadow Register Set that can be Used for Any Priority Level, Eliminating Software Context Switch and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors' Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

**FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM**

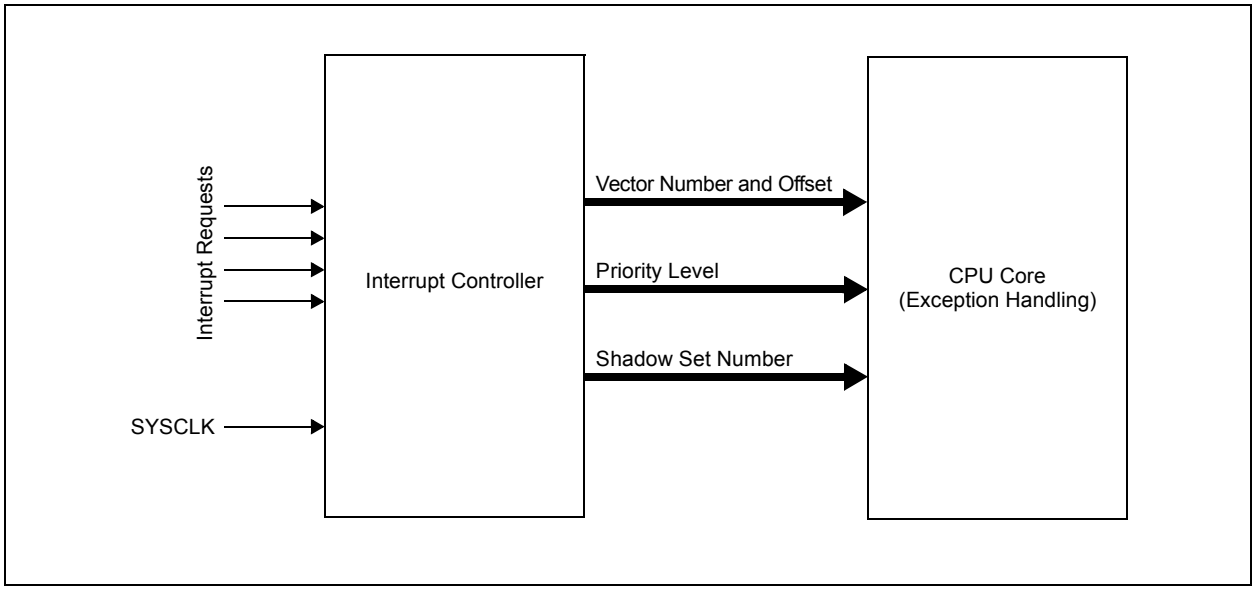


**TABLE 7-3: INTERRUPT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | VS<6:0> | | | | | | | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| F010 | PRISS | 31:16 | PRI7SS<3:0> | | | | PRI6SS<3:0> | | | | PRI5SS<3:0> | | | | PRI4SS<3:0> | | | | 0000 |
| | | 15:0 | PRI3SS<3:0> | | | | PRI2SS<3:0> | | | | PRI1SS<3:0> | | | | — | — | — | SS0 | 0000 |
| F020 | INTSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | SIRQ<7:0> | | | | | | | | 0000 |
| F030 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F040 | IFS0 | 31:16 | — | USBIF | — | — | — | — | CMP3IF | CMP2IF | CMP1IF | — | — | — | T3IF | T2IF | T1IF | — | 0000 |
| | | 15:0 | — | — | — | — | CNDIF | CNCIF | CNBIF | CNAIF | INT4IF | INT3IF | INT2IF | INT1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| F050 | IFS1 | 31:16 | — | — | U3EIF | U3TXIF | U3RXIF | U2EIF | U2TXIF | U2RXIF | U1EIF | U1TXIF | U1RXIF | — | — | — | SPI3RXIF | SPI3TXIF | 0000 |
| | | 15:0 | SPI3EIF | SPI2RXIF | SPI2TXIF | SPI2EIF | SPI1RXIF | SPI1TXIF | SPI1EIF | CLC4IF | CLC3IF | CLC2IF | CLC1IF | LVDIF | — | — | AD1IF | RTCCIF | 0000 |
| F060 | IFS2 | 31:16 | CPCIF | NVMIF | — | FSTIF | CCT9IF | CCP9IF | CCT8IF | CCP8IF | CCT7IF | CCP7IF | CCT6IF | CCP6IF | CCT5IF | CCP5IF | CCT4IF | CCP4IF | 0000 |
| | | 15:0 | CCT3IF | CCP3IF | CCT2IF | CCP2IF | CCT1IF | CCP1IF | I2C3BCIF | I2C3MIF | I2C3SIF | I2C2BCIF | I2C2MIF | I2C2SIF | I2C1BCIF | I2C1MIF | I2C1SIF | — | 0000 |
| F070 | IFS3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | DMA3IF | DMA2IF | DMA1IF | DMA0IF | ECCBEIF | — | 0000 |
| F080 | IEC0 | 31:16 | — | USBIE | — | — | — | — | CMP3IE | CMP2IE | CMP1IE | — | — | — | T3IE | T2IE | T1IE | — | 0000 |
| | | 15:0 | — | — | — | — | CNDIE | CNCIE | CNBIE | CNAIE | INT4IE | INT3IE | INT2IE | INT1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| F090 | IEC1 | 31:16 | — | — | U3EIE | U3TXIE | U3RXIE | U2EIE | U2TXIE | U2RXIE | U1EIE | U1TXIE | U1RXIE | — | — | — | SPI3RXIE | SPI3TXIE | 0000 |
| | | 15:0 | SPI3EIE | SPI2RXIE | SPI2TXIE | SPI2EIE | SPI1RXIE | SPI1TXIE | SPI1EIE | CLC4IE | CLC3IE | CLC2IE | CLC1IE | LVDIE | — | — | AD1IE | RTCCIE | 0000 |
| F0A0 | IEC2 | 31:16 | CPCIE | NVMIE | — | FSTIE | CCT9IE | CCP9IE | CCT8IE | CCP8IE | CCT7IE | CCP7IE | CCT6IE | CCP6IE | CCT5IE | CCP5IE | CCT4IE | CCP4IE | 0000 |
| | | 15:0 | CCT3IE | CCP3IE | CCT2IE | CCP2IE | CCT1IE | CCP1IE | I2C3BCIE | I2C3MIE | I2C3SIE | I2C2BCIE | I2C2MIE | I2C2SIE | I2C1BCIE | I2C1MIE | I2C1SIE | — | 0000 |
| F0B0 | IEC3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | DMA3IE | DMA2IE | DMA1IE | DMA0IE | ECCBEIE | — | 0000 |
| F0C0 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| F0D0 | IPC1 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | 0000 |
| F0E0 | IPC2 | 31:16 | — | — | — | CNDIP<2:0> | | | CNDIS<1:0> | | — | — | — | CNCIP<2:0> | | | CNCIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CNBIP<2:0> | | | CNBIS<1:0> | | — | — | — | CNAIP<2:0> | | | CNAIS<1:0> | | 0000 |
| F0F0 | IPC3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 8960 | DCH0CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 8970 | DCH0ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 8980 | DCH0INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 8990 | DCH0SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 89A0 | DCH0DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 89B0 | DCH0SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 89C0 | DCH0DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 89D0 | DCH0SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 89E0 | DCH0DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 89F0 | DCH0CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8A00 | DCH0CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8A10 | DCH0DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 8A20 | DCH1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 8A30 | DCH1ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 8A40 | DCH1INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

**REGISTER 8-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)**

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate an LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

**REGISTER 8-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPDAT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All Other modes:
Unused.

# 9.0 OSCILLATOR CONFIGURATION

**Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0256GPM064 family oscillator system has the following modules and features:

- A Total of Five External and Internal Oscillator Options as Clock Sources
- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- On-Chip User-Selectable Divisor Postscaler on Select Oscillator Sources
- Software-Controllable Switching between Various Clock Sources
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output

A block diagram of the oscillator system is provided in Figure 9-1.

## 9.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0256GPM064 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

## 9.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switching process.

**Note:** The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

### 9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in FOSC must be programmed to '0'. (Refer to **Section 26.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSC<2:0> control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

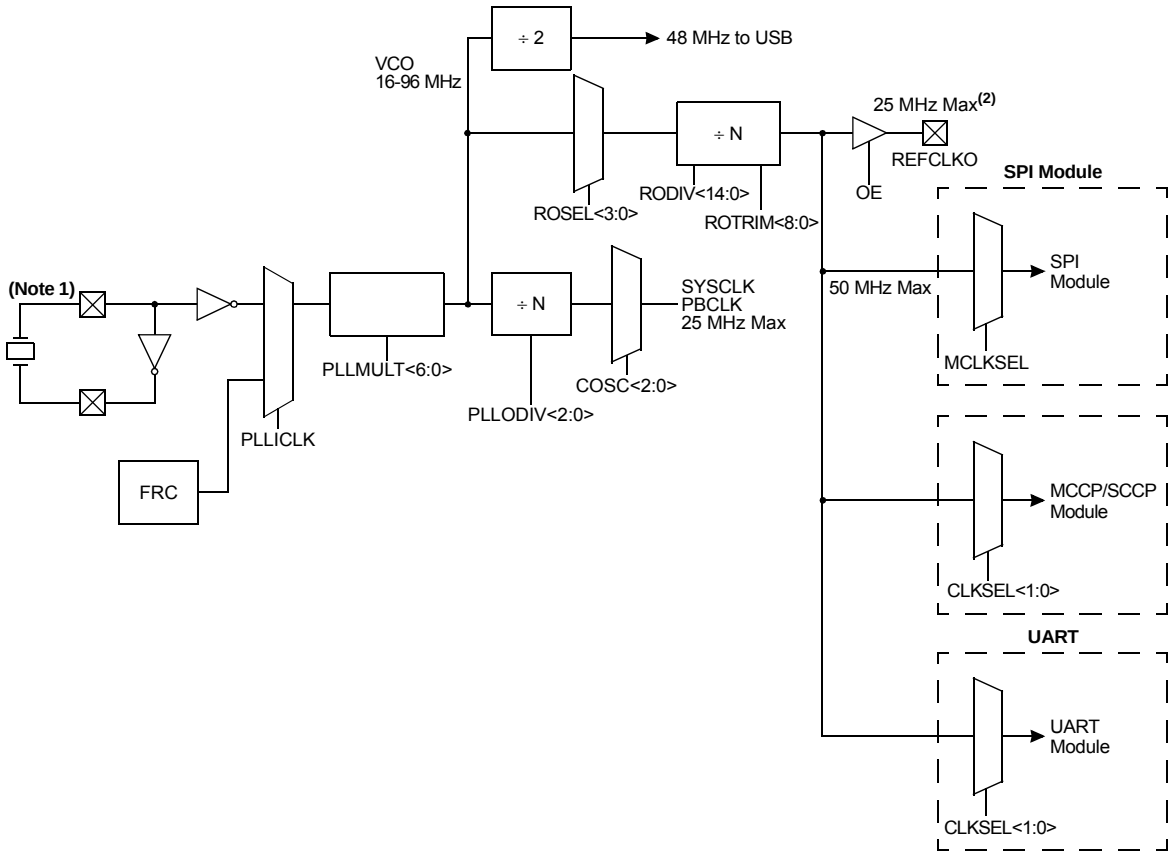
The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

### 9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register.
3. Write the appropriate value to the NOSC<2:0> bits (OSCCON<10:8>) for the new oscillator source.
4. Set the OSWEN bit to initiate the oscillator switch.

**FIGURE 9-2: REFERENCE OSCILLATOR**




**Note 1:** Support circuitry for crystal is not shown.
**2:** In Retention mode, the maximum peripheral output frequency to an I/O pin must be limited to 33 kHz or less.

**TABLE 10-3: REMAPPABLE INPUT SOURCES PIN ASSIGNMENTS(1)**

| Value | RPn Pins | Pin Assignment |
|---|---|---|
| 00001 | RP1 | RA0 Pin |
| 00010 | RP2 | RA1 Pin |
| 00011 | RP3 | RA2 Pin |
| 00100 | RP4 | RA3 Pin |
| 00101 | RP5 | RA4 Pin |
| 00110 | RP6 | RB0 Pin |
| 00111 | RP7 | RB1 Pin |
| 01000 | RP8 | RB2 Pin |
| 01001 | RP9 | RB3 Pin |
| 01010 | RP10 | RB4 Pin |
| 01011 | RP11 | RB5 Pin |
| 01100 | RP12 | RB7 Pin |
| 01101 | RP13 | RB8 Pin |
| 01110 | RP14 | RB9 Pin |
| 01111 | RP15 | RB13 Pin |
| 10000 | RP16 | RB14 Pin |
| 10001 | RP17 | RB15 Pin |
| 10010 | RP18 | RC9 Pin |
| 10011 | RP19 | RC2 Pin |
| 10100 | RP20 | RC7 Pin |
| 10101 | RP21 | RA7 Pin |
| 10110 | RP22 | RA10 Pin |
| 10111 | RP23 | RC6 Pin |
| 11000 | RP24 | RA9 Pin |
| 11001-11111 | Reserved | |

**Note 1:** All RPx pins are not available on all packages.

**REGISTER 14-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER (CONTINUED)**

bit 19-18 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

bit 17-16 **PSSBDF<1:0>:** PWMx Output Pins, OCxB, OCxD and OCxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT<5:0>:** PWM Dead-Time Select bits(1)
111111 = Insert 63 dead-time delay periods between complementary output signals
111110 = Insert 62 dead-time delay periods between complementary output signals
...
000010 = Insert 2 dead-time delay periods between complementary output signals
000001 = Insert 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

**Note 1:** These bits are implemented in MCCP modules only.

**REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/C-0 | U-0 | U-0 |
| | — | — | — | — | — | ICGARM(1) | — | — |
| 7:0 | R-0 | W1-0 | W1-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **PRLWIP:** CCPxPRL Write in Progress Status bit
- 1 = An update to the CCPxPRL register with the buffered contents is in progress
- 0 = An update to the CCPxPRL register is not in progress

bit 19 **TMRHWIP:** CCPxTMRH Write in Progress Status bit
- 1 = An update to the CCPxTMRH register with the buffered contents is in progress
- 0 = An update to the CCPxTMRH register is not in progress

bit 18 **TMRLWIP:** CCPxTMRL Write in Progress Status bit
- 1 = An update to the CCPxTMRL register with the buffered contents is in progress
- 0 = An update to the CCPxTMRL register is not in progress

bit 17 **RBWIP:** CCPxRB Write in Progress Status bit
- 1 = An update to the CCPxRB register with the buffered contents is in progress
- 0 = An update to the CCPxRB register is not in progress

bit 16 **RAWIP:** CCPxRA Write in Progress Status bit
- 1 = An update to the CCPxRA register with the buffered contents is in progress
- 0 = An update to the CCPxRA register is not in progress

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **ICGARM:** Input Capture Gate Arm bit(1)

A write of '1' to this location will arm the input capture gating logic for a one-shot gate event when ICGSM<1:0> = 01 or 10. The bit location reads as '0'.

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CCPTRIG:** CCPx Trigger Status bit
- 1 = Timer has been triggered and is running (set by hardware or writing to TRSET)
- 0 = Timer has not been triggered and is held in Reset (cleared by writing to TRCLR)

bit 6 **TRSET:** CCPx Trigger Set Request bit

Write '1' to this location to trigger the timer when TRIGEN = 1 (location always reads '0').

bit 5 **TRCLR:** CCPx Trigger Clear Request bit

Write '1' to this location to cancel the timer trigger when TRIGEN = 1 (location always reads '0').

bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit
- 1 = A shutdown event is in progress; CCPx outputs are in the shutdown state
- 0 = CCPx outputs operate normally

**Note 1:** This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

**REGISTER 18-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)**

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
1 = Token packet rejected due to CRC5 error
0 = Token packet accepted

**EOFEF:** EOF Error Flag bit(3,5)
1 = EOF error condition detected
0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**REGISTER 18-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE(1) / EOFEE(2) | PIDEE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

**EOFEE:** EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

**Note 1:** Device mode.
**2:** Host mode.

## 19.1 RTCC Control Registers

**TABLE 19-1: RTCC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | RTCCON1 | 31:16 | ALRMEN | CHIME | — | — | AMASK<3:0> | | | | ALMRPT<7:0> | | | | | | | | 0000 |
| | | 15:0 | ON | — | — | — | WRLOCK | — | — | — | RTCOE | OUTSEL<2:0> | | | — | — | — | — | 0000 |
| 0010 | RTCCON2 | 31:16 | DIV<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | FDIV<4:0> | | | | | — | — | — | — | — | PS<1:0> | | — | — | CLKSEL<1:0> | | 0000 |
| 0030 | RTCSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ALMEVT | — | — | SYNC | ALMSYNC | HALFSEC | 0000 |
| 0040 | RTCTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | | xxxx |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0050 | RTCDATE | 31:16 | YRTEN<3:0> | | | | YRONE<3:0> | | | | — | — | — | MTHTEN | MTHONE<3:0> | | | | 0000 |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | | — | — | — | — | — | WDAY<2:0> | | | 0000 |
| 0060 | ALMTIME | 31:16 | — | HRTEN<2:0> | | | HRONE<3:0> | | | | — | MINTEN<2:0> | | | MINONE<3:0> | | | | xxxx |
| | | 15:0 | SECTEN<3:0> | | | | SECONE<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0070 | ALMDATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | MTHTEN | MTHONE<3:0> | | | | 0000 |
| | | 15:0 | — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | | — | — | — | — | — | WDAY<2:0> | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**REGISTER 20-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)**

bit 7-4 **SSRC<3:0>:** Conversion Trigger Source Select bits
1111 = CLC2 module event ends sampling and starts conversion
1110 = CLC1 module event ends sampling and starts conversion
1101 = SCCP6 module event ends sampling and starts conversion
1100 = SCCP5 module event ends sampling and starts conversion
1011 = SCCP4 module event ends sampling and starts conversion
1010 = MCCP3 module event ends sampling and starts conversion
1001 = MCCP2 module event ends sampling and starts conversion
1000 = MCCP1 module event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
0100-0011 = Reserved
0010 = Timer3 period match ends sampling and starts conversion
0001 = Active transition on INT0 pin ends sampling and starts conversion
0000 = Clearing the SAMP bit ends sampling and starts conversion

bit 3 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit ADC operation
0 = 10-bit ADC operation

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
0 = The ADC SHA is holding
When ASAM = 0, writing '1' to this bit starts sampling. When SSRC<3:0 = 0000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** ADC Conversion Status bit(1)
1 = Analog-to-Digital conversion is done
0 = Analog-to-Digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

**Note 1:** The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.
**2:** The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).

**REGISTER 20-2: AD1CON2: ADC CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | VCFG<2:0> | | | OFFCAL | BUFREGEN | CSCNA | — | — |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BUFS | — | SMPI<3:0> | | | | BUFM | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

| | ADC $V_{R+}$ | ADC $V_{R-}$ |
|---|---|---|
| 000 | $AV_{DD}$ | $AV_{SS}$ |
| 001 | $AV_{DD}$ | External $V_{REF-}$ Pin |
| 010 | External $V_{REF+}$ Pin | $AV_{SS}$ |
| 011 | External $V_{REF+}$ Pin | External $V_{REF-}$ Pin |
| 1xx | Unimplemented; do not use | |

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ SHA Input for Input Multiplexer Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1 (ADC buffers split into 2 x 11-word buffers).
1 = ADC is currently filling Buffers 11-21, user should access data in 0-10
0 = ADC is currently filling Buffers 0-10, user should access data in 11-21

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 11-word buffers, ADC1BUF(0...10), ADC1BUF(11...21)
0 = Buffer configured as one 22-word buffer, ADC1BUF(0...21)

bit 0 **Unimplemented:** Read as '0'

**TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)**

| Peripheral | PMDx Bit Name | Register Name and Bit Location |
|---|---|---|
| Universal Asynchronous Receiver Transmitter 2 (UART2) | U2MD | PMD5<1> |
| Universal Asynchronous Receiver Transmitter 3 (UART3) | U3MD | PMD5<2> |
| Serial Peripheral Interface 1 (SPI1) | SPI1MD | PMD5<8> |
| Serial Peripheral Interface 2 (SPI2) | SPI2MD | PMD5<9> |
| Serial Peripheral Interface 3 (SPI3) | SPI3MD | PMD5<10> |
| Inter-Integrated Circuit Interface 1 (I2C1) | I2C1MD | PMD5<16> |
| Inter-Integrated Circuit Interface 2 (I2C2) | I2C2MD | PMD5<17> |
| Inter-Integrated Circuit Interface 3 (I2C3) | I2C3MD | PMD5<18> |
| Universal Serial Bus (USB) | USBMD | PMD5<24> |
| Real-Time Clock and Calendar (RTCC) | RTCCMD | PMD6<0> |
| Reference Clock Output (REFO1) | REFOMD | PMD6<8> |
| Direct Memory Access (DMA) | DMAMD | PMD7<4> |

**TABLE 29-14: COMPARATOR DC SPECIFICATIONS**

| **Operating Conditions:** 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Comments** |
| D300 | VIOFF | Input Offset Voltage | -20 | — | +20 | mV | **(Note 1)** |
| D301 | VICM | Input Common-Mode Voltage | VSS – 0.3V | — | VDD + 0.3V | V | **(Note 1)** |
| D307 | TRESP | Response Time | — | 150 | — | ns | **(Note 2)** |

**Note 1:** Parameters are characterized but not tested.

**2:** Measured with one input at VDD/2 and the other transitioning from VSS to VDD, 40 mV step, 15 mV overdrive.

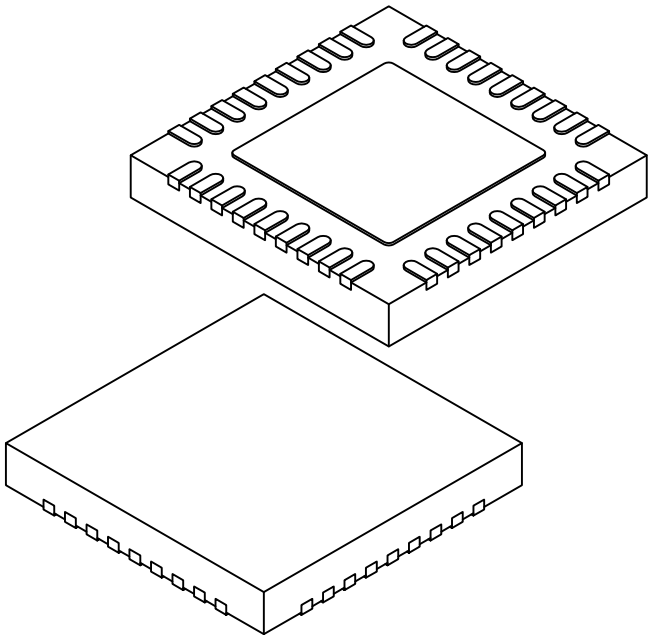
**TABLE 29-15: VOLTAGE REFERENCE DC SPECIFICATIONS**

| **Operating Conditions:** 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Comments** |
| VRD310 | TSET | Settling Time | — | — | 10 | µs | **(Note 1)** |
| VRD311 | VRAA | Absolute Accuracy | -1 | — | 1 | LSb | |
| VRD312 | VRUR | Unit Resistor Value (R) | — | 4.5 | — | kΩ | |

**Note 1:** Measures the interval while DACDAT<4:0> transitions from '11111' to '00000'.

**36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]**
**SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 36 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.70 | 3.80 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.70 | 3.80 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.50 | 0.60 | 0.75 |
| Terminal-to-Exposed-Pad | K | 0.45 | 0.55 | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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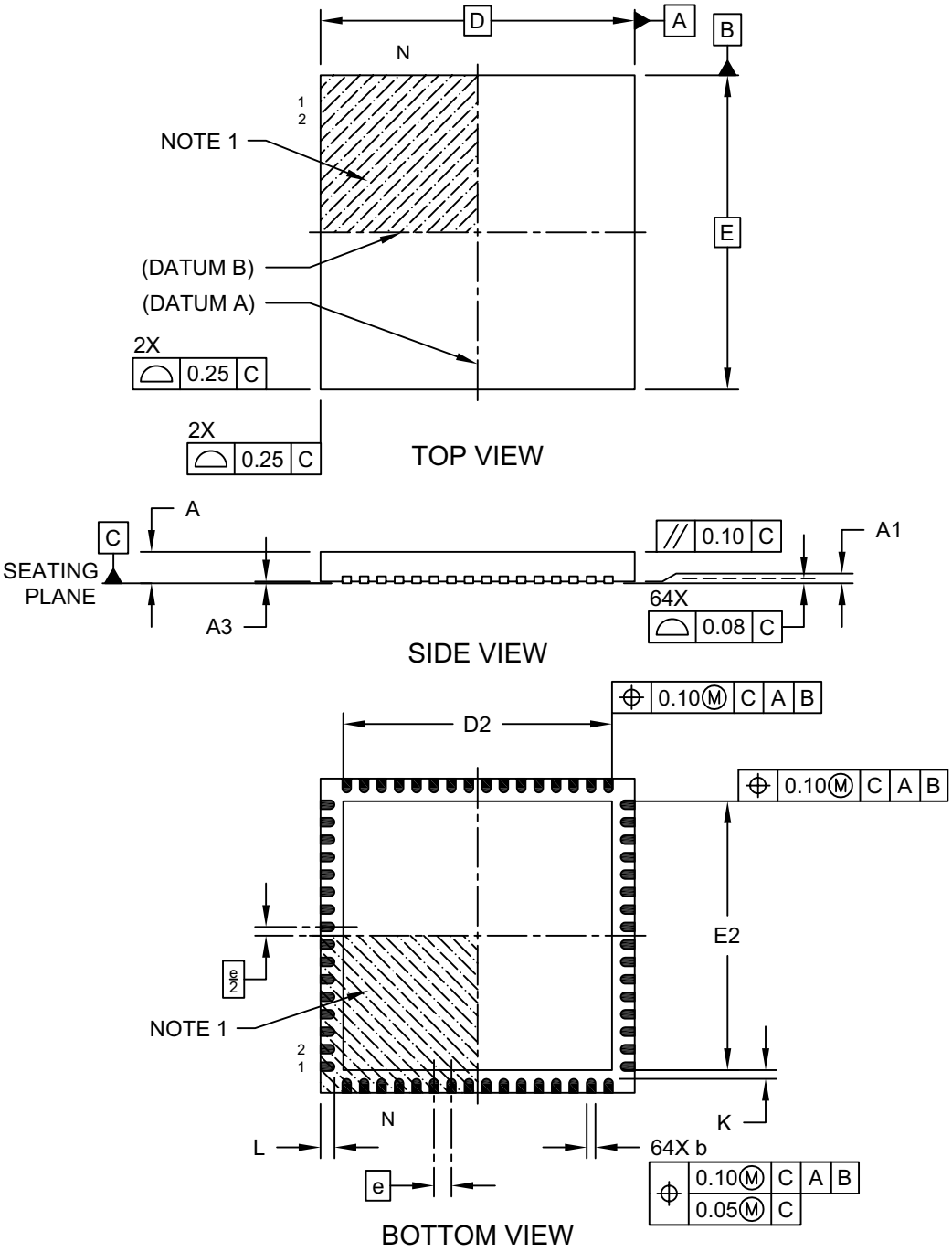
**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.70 x 7.70 Exposed Pad [QFN]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-213B Sheet 1 of 2