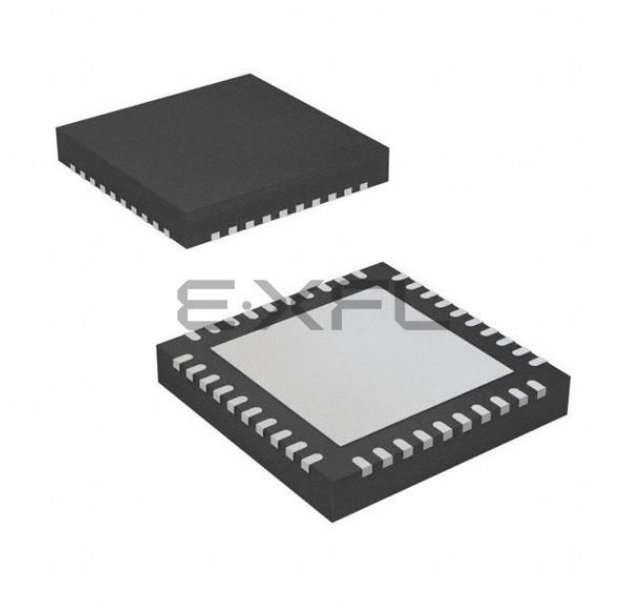
# Microchip Technology - PIC32MM0064GPM036T-I/MV Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 15x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-UFQFN Exposed Pad |
| Supplier Device Package | 40-UQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm036t-i-mv |

## Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

**TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES**

| Device | Pins | Program Memory (Kbytes) | Data Memory (Kbytes) | General Purpose I/O/PPS | 16-Bit Timers Maximum | PWM Outputs Maximum | Remappable Peripherals | | | | | | 10/12-Bit ADC (External Channels) | Comparators | CRC | RTCC | $I^2C$ | USB | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Dedicated 16-Bit Timers | UART(1)/LIN/J2602 | MCCP(4) | SCCP(3) | CLC | SPI(2)/$I^2S$ | | | | | | | |
| PIC32MM0064GPM028 | 28 | 64 | 16 | 21/18 | 21 | 18 | 3 | 3 | 3 | 6 | 4 | 3 | 12 | 3 | Yes | Yes | 3 | Yes | SSOP/QFN/ UQFN |
| PIC32MM0128GPM028 | 28 | 128 | 16 | 21/18 | 21 | 18 | 3 | 3 | 3 | 6 | 4 | 3 | 12 | 3 | Yes | Yes | 3 | Yes | SSOP/QFN/ UQFN |
| PIC32MM0256GPM028 | 28 | 256 | 32 | 21/18 | 21 | 18 | 3 | 3 | 3 | 6 | 4 | 3 | 12 | 3 | Yes | Yes | 3 | Yes | SSOP/QFN/ UQFN |
| PIC32MM0064GPM036 | 36/40 | 64 | 16 | 27/20 | 21 | 20 | 3 | 3 | 3 | 6 | 4 | 3 | 15 | 3 | Yes | Yes | 3 | Yes | VQFN/UQFN |
| PIC32MM0128GPM036 | 36/40 | 128 | 16 | 27/20 | 21 | 20 | 3 | 3 | 3 | 6 | 4 | 3 | 15 | 3 | Yes | Yes | 3 | Yes | VQFN/UQFN |
| PIC32MM0256GPM036 | 36/40 | 256 | 32 | 27/20 | 21 | 20 | 3 | 3 | 3 | 6 | 4 | 3 | 15 | 3 | Yes | Yes | 3 | Yes | VQFN/UQFN |
| PIC32MM0064GPM048 | 48 | 64 | 16 | 38/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 17 | 3 | Yes | Yes | 3 | Yes | UQFN/TQFP |
| PIC32MM0128GPM048 | 48 | 128 | 16 | 38/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 17 | 3 | Yes | Yes | 3 | Yes | UQFN/TQFP |
| PIC32MM0256GPM048 | 48 | 256 | 32 | 38/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 17 | 3 | Yes | Yes | 3 | Yes | UQFN/TQFP |
| PIC32MM0064GPM064 | 64 | 64 | 16 | 52/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 20 | 3 | Yes | Yes | 3 | Yes | QFN/TQFP |
| PIC32MM0128GPM064 | 64 | 128 | 16 | 52/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 20 | 3 | Yes | Yes | 3 | Yes | QFN/TQFP |
| PIC32MM0256GPM064 | 64 | 256 | 32 | 52/24 | 21 | 24 | 3 | 3 | 3 | 6 | 4 | 3 | 20 | 3 | Yes | Yes | 3 | Yes | QFN/TQFP |

**Note 1:** UART1 has assigned pins. UART2 and UART3 are remappable.

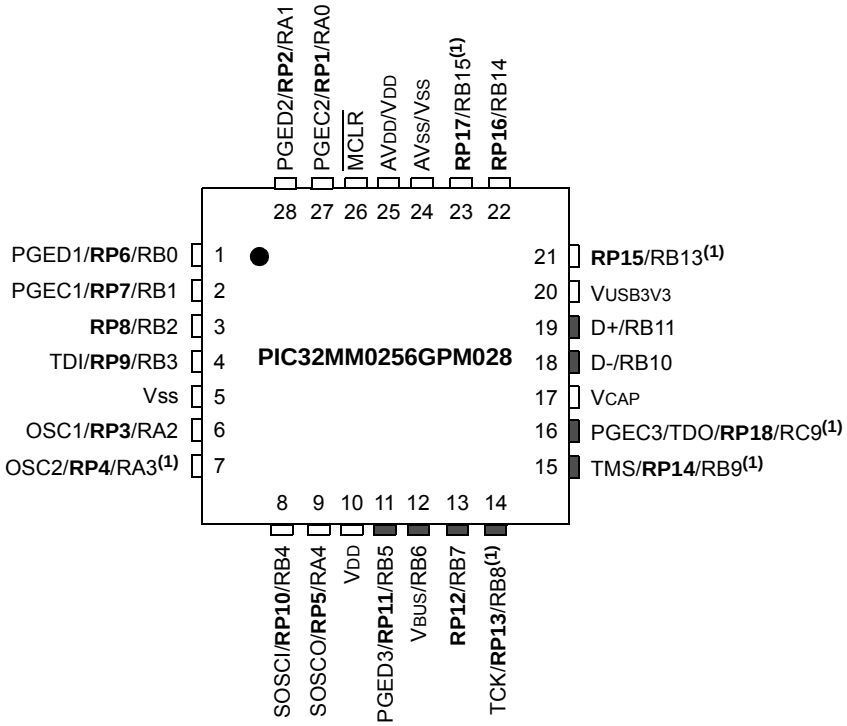
**2:** SPI1 and SPI3 have assigned pins. SPI2 is remappable.

**3:** SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

**4:** MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

## Pin Diagrams (Continued)

**28-Pin QFN/UQFN**




**Legend:** Shaded pins are up to 5V tolerant.
**Note 1:** High drive strength pin.

### TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0 | 15 | TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1) |
| 2 | PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1 | 16 | PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1) |
| 3 | AN4/C1INB/**RP8**/SDA2/OCM2E/RB2 | 17 | VCAP |
| 4 | TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3 | 18 | D-/RB10 |
| 5 | VSS | 19 | D+/RB11 |
| 6 | OSC1/CLKI/AN5/**RP3**/OCM1C/RA2 | 20 | VUSB3V3 |
| 7 | OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1) | 21 | AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1) |
| 8 | SOSCI/AN7/**RP10**/OCM3C/RB4 | 22 | CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14 |
| 9 | SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4 | 23 | AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1) |
| 10 | VDD | 24 | AVSS/VSS |
| 11 | PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5 | 25 | AVDD/VDD |
| 12 | VBUS/RB6 | 26 | MCLR |
| 13 | **RP12**/SDA3/SDI3/OCM3F/RB7 | 27 | PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0 |
| 14 | TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1) | 28 | PGED2/VREF-/AN1/**RP2**/OCM1F/RA1 |

**Note 1:** High drive strength pin.
**2:** Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

## Table of Contents

## 3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting of the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the WAIT instruction, used to initiate Sleep or Idle. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

## 3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

## 3.5 MIPS32® microAptiv™ UC Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv UC core, which is included on PIC32MM0256GPM064 family devices.

**REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0, HC | R/W-0 | R-0, HS, HC | R-0, HS, HC | r-0 | U-0 | U-0 | U-0 |
| | WR(1,3) | WREN(1) | WRERR(1,2) | LVDERR(1,2) | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> | | | |

| **Legend:** | HS = Hardware Settable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1,3)

This bit cannot be cleared and can be set only when WREN = 1, and the unlock sequence has been performed.
1 = Initiates a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enables writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disables writes to the WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage is detected (possible data corruption if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **Reserved:** Maintain as '0'

bit 10-4 **Unimplemented:** Read as '0'

**Note 1:** These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

**2:** These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).

**3:** This bit is only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

**TABLE 7-2: INTERRUPTS (CONTINUED)**

| Interrupt Source | MPLAB® XC32 Vector Name | Vector Number | Interrupt Related Bits Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Subpriority | |
| UART2 Reception | _UART2_RX_VECTOR | 56 | IFS1<24> | IEC1<24> | IPC14<4:2> | IPC14<1:0> | Yes |
| UART2 Transmission | _UART2_TX_VECTOR | 57 | IFS1<25> | IEC1<25> | IPC14<12:10> | IPC14<9:8> | Yes |
| UART2 Error | _UART2_ERR_VECTOR | 58 | IFS1<26> | IEC1<26> | IPC14<20:18> | IPC14<17:16> | Yes |
| UART3 Reception | _UART3_RX_VECTOR | 59 | IFS1<27> | IEC1<27> | IPC14<28:26> | IPC14<25:24> | Yes |
| UART3 Transmission | _UART3_TX_VECTOR | 60 | IFS1<28> | IEC1<28> | IPC15<4:2> | IPC15<1:0> | Yes |
| UART3 Error | _UART3_ERR_VECTOR | 61 | IFS1<29> | IEC1<29> | IPC15<12:10> | IPC15<9:8> | Yes |
| RESERVED | | 62 | IFS1<30> | IEC1<30> | IPC15<20:18> | IPC15<17:16> | No |
| RESERVED | | 63 | IFS1<31> | IEC1<31> | IPC15<28:26> | IPC15<25:24> | No |
| RESERVED | | 64 | IFS2<0> | IEC2<0> | IPC16<4:2> | IPC16<1:0> | No |
| I2C1 Slave | _I2C1_SLAVE_VECTOR | 65 | IFS2<1> | IEC2<1> | IPC16<12:10> | IPC16<9:8> | Yes |
| I2C1 Master | _I2C1_MASTER_VECTOR | 66 | IFS2<2> | IEC2<2> | IPC16<20:18> | IPC16<17:16> | Yes |
| I2C1 Bus Collision | _I2C1_BUS_VECTOR | 67 | IFS2<3> | IEC2<3> | IPC16<28:26> | IPC16<25:24> | Yes |
| I2C2 Slave | _I2C2_SLAVE_VECTOR | 68 | IFS2<4> | IEC2<4> | IPC17<4:2> | IPC17<1:0> | Yes |
| I2C2 Master | _I2C2_MASTER_VECTOR | 69 | IFS2<5> | IEC2<5> | IPC17<12:10> | IPC17<9:8> | Yes |
| I2C2 Bus Collision | _I2C2_BUS_VECTOR | 70 | IFS2<6> | IEC2<6> | IPC17<20:18> | IPC17<17:16> | Yes |
| I2C3 Slave | _I2C3_SLAVE_VECTOR | 71 | IFS2<7> | IEC2<7> | IPC17<28:26> | IPC17<25:24> | Yes |
| I2C3 Master | _I2C3_MASTER_VECTOR | 72 | IFS2<8> | IEC2<8> | IPC18<4:2> | IPC18<1:0> | Yes |
| I2C3 Bus Collision | _I2C3_BUS_VECTOR | 73 | IFS2<9> | IEC2<9> | IPC18<12:10> | IPC18<9:8> | Yes |
| CCP1 Input Capture or Output Compare | _CCP1_VECTOR | 74 | IFS2<10> | IEC2<10> | IPC18<20:18> | IPC18<17:16> | No |
| CCP1 Timer | _CCT1_VECTOR | 75 | IFS2<11> | IEC2<11> | IPC18<28:26> | IPC18<25:24> | No |
| CCP2 Input Capture or Output Compare | _CCP2_VECTOR | 76 | IFS2<12> | IEC2<12> | IPC19<4:2> | IPC19<1:0> | No |
| CCP2 Timer | _CCT2_VECTOR | 77 | IFS2<13> | IEC2<13> | IPC19<12:10> | IPC19<9:8> | No |
| CCP3 Input Capture or Output Compare | _CCP3_VECTOR | 78 | IFS2<14> | IEC2<14> | IPC19<20:18> | IPC19<17:16> | No |
| CCP3 Timer | _CCT3_VECTOR | 79 | IFS2<15> | IEC2<15> | IPC19<28:26> | IPC19<25:24> | No |
| CCP4 Input Capture or Output Compare | _CCP4_VECTOR | 80 | IFS2<16> | IEC2<16> | IPC20<4:2> | IPC20<1:0> | No |
| CCP4 Timer | _CCT4_VECTOR | 81 | IFS2<17> | IEC2<17> | IPC20<12:10> | IPC20<9:8> | No |
| CCP5 Input Capture or Output Compare | _CCP5_VECTOR | 82 | IFS2<18> | IEC2<18> | IPC20<20:18> | IPC20<17:16> | No |
| CCP5 Timer | _CCT5_VECTOR | 83 | IFS2<19> | IEC2<19> | IPC20<28:26> | IPC20<25:24> | No |
| CCP6 Input Capture or Output Compare | _CCP6_VECTOR | 84 | IFS2<20> | IEC2<20> | IPC21<4:2> | IPC21<1:0> | No |
| CCP6 Timer | _CCT6_VECTOR | 85 | IFS2<21> | IEC2<21> | IPC21<12:10> | IPC21<9:8> | No |
| CCP7 Input Capture or Output Compare | _CCP7_VECTOR | 86 | IFS2<22> | IEC2<22> | IPC21<20:18> | IPC21<17:16> | No |
| CCP7 Timer | _CCT7_VECTOR | 87 | IFS2<23> | IEC2<23> | IPC21<28:26> | IPC21<25:24> | No |

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F100 | IPC4 | 31:16 | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| F110 | IPC5 | 31:16 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| F120 | IPC6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | CMP3IP<2:0> | | | CMP3IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| F130 | IPC7 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| F140 | IPC8 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | 0000 |
| F150 | IPC9 | 31:16 | — | — | — | CLC3IP<2:0> | | | CLC3IS<1:0> | | — | — | — | CLC2IP<2:0> | | | CLC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CLC1IP<2:0> | | | CLC1IS<1:0> | | — | — | — | LVDIP<2:0> | | | LVDIS<1:0> | | 0000 |
| F160 | IPC10 | 31:16 | — | — | — | SPI1RXIP<2:0> | | | SPI1RXIS<1:0> | | — | — | — | SPI1TXIP<2:0> | | | SPI1TXIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | SPI1EIP<2:0> | | | SPI1EIS<1:0> | | — | — | — | CLC4IP<2:0> | | | CLC4IS<1:0> | | 0000 |
| F170 | IPC11 | 31:16 | — | — | — | SPI3EIP<2:0> | | | SPI3EIS<1:0> | | — | — | — | SPI2RXIP<2:0> | | | SPI2RXIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | SPI2TXIP<2:0> | | | SPI2TXIS<1:0> | | — | — | — | SPI2EIP<2:0> | | | SPI2EIS<1:0> | | 0000 |
| F180 | IPC12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | SPI3RXIP<2:0> | | | SPI3RXIS<1:0> | | — | — | — | SPI3TXIP<2:0> | | | SPI3TXIS<1:0> | | 0000 |
| F190 | IPC13 | 31:16 | — | — | — | U1EIP<2:0> | | | U1EIS<1:0> | | — | — | — | U1TXIP<2:0> | | | U1TXIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U1RXIP<2:0> | | | U1RXIS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| F1A0 | IPC14 | 31:16 | — | — | — | U3RXIP<2:0> | | | U3RXIS<1:0> | | — | — | — | U2EIP<2:0> | | | U2EIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U2TXIP<2:0> | | | U2TXIS<1:0> | | — | — | — | U2RXIP<2:0> | | | U2RXIS<1:0> | | 0000 |
| F1B0 | IPC15 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | U3EIP<2:0> | | | U3EIS<1:0> | | — | — | — | U3TXIP<2:0> | | | U3TXIS<1:0> | | 0000 |
| F1C0 | IPC16 | 31:16 | — | — | — | I2C1BCIP<2:0> | | | I2C1BCIS<1:0> | | — | — | — | I2C1MIP<2:0> | | | I2C1MIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1SIP<2:0> | | | I2C1SIS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| F1D0 | IPC17 | 31:16 | — | — | — | I2C3SIP<2:0> | | | I2C3SIS<1:0> | | — | — | — | I2C2BCIP<2:0> | | | I2C2BCIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2MIP<2:0> | | | I2C2MIS<1:0> | | — | — | — | I2C2SIP<2:0> | | | I2C2SIS<1:0> | | 0000 |
| F1E0 | IPC18 | 31:16 | — | — | — | CCT1IP<2:0> | | | CCT1IS<1:0> | | — | — | — | CCP1IP<2:0> | | | CCP1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C3BCIP<2:0> | | | I2C3BCIS<1:0> | | — | — | — | I2C3MIP<2:0> | | | I2C3MIS<1:0> | | 0000 |
| F1F0 | IPC19 | 31:16 | — | — | — | CCT3IP<2:0> | | | CCT3IS<1:0> | | — | — | — | CCP3IP<2:0> | | | CCP3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CCT2IP<2:0> | | | CCT2IS<1:0> | | — | — | — | CCP2IP<2:0> | | | CCP2IS<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F200 | IPC20 | 31:16 | — | — | — | CCT5IP<2:0> | | | CCT5IS<1:0> | | — | — | — | CCP5IP<2:0> | | | CCP5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CCT4IP<2:0> | | | CCT4IS<1:0> | | — | — | — | CCP4IP<2:0> | | | CCP4IS<1:0> | | 0000 |
| F210 | IPC21 | 31:16 | — | — | — | CCT7IP<2:0> | | | CCT7IS<1:0> | | — | — | — | CCP7IP<2:0> | | | CCP7IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CCT6IP<2:0> | | | CCT6IS<1:0> | | — | — | — | CCP6IP<2:0> | | | CCP6IS<1:0> | | 0000 |
| F220 | IPC22 | 31:16 | — | — | — | CCT9IP<2:0> | | | CCT9IS<1:0> | | — | — | — | CCP9IP<2:0> | | | CCP9IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CCT8IP<2:0> | | | CCT8IS<1:0> | | — | — | — | CCP8IP<2:0> | | | CCP8IS<1:0> | | 0000 |
| F230 | IPC23 | 31:16 | — | — | — | CPCIP<2:0> | | | CPCIS<1:0> | | — | — | — | NVMIP<2:0> | | | NVMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | FSTIP<2:0> | | | FSTIS<1:0> | | 0000 |
| F240 | IPC24 | 31:16 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | ECCBEIP<2:0> | | | ECCBEIS<1:0> | | — | — | — | — | — | — | — | — | 0000 |
| F250 | IPC25 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP3<2:0> | | | IS3<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP2<2:0> | | | IS2<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP1<2:0> | | | IS1<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP0<2:0> | | | IS0<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority 3 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority 3 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority 2 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority 2 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

**REGISTER 8-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPDAT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All Other modes:
Unused.

## 12.0 TIMER2 AND TIMER3

**Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-Bit Timer
- Synchronous Internal 16-Bit Gated Timer
- Synchronous External 16-Bit Timer

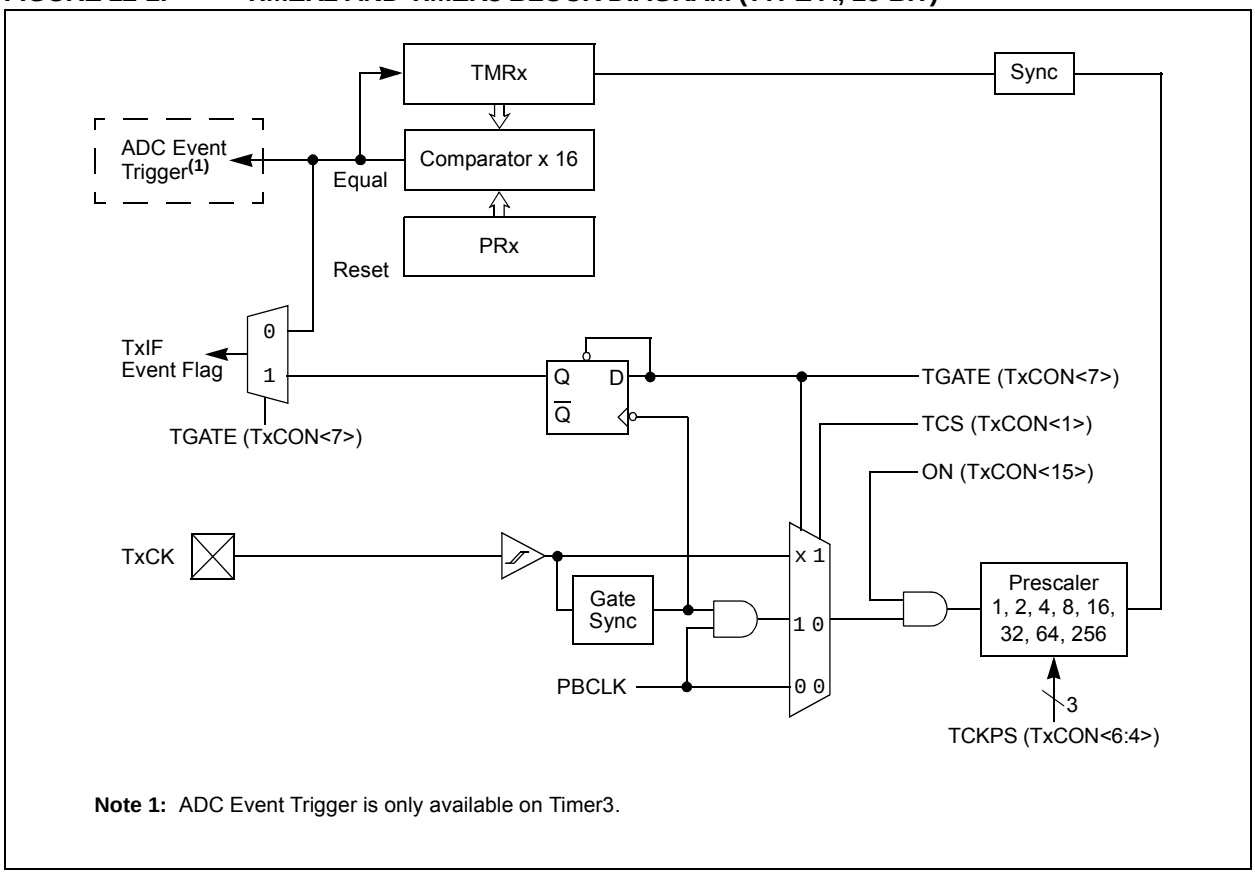
A single 32-bit synchronous timer is available by combining Timer2 with Timer3. The resulting 32-bit timer can operate in three modes:

- Synchronous Internal 32-Bit Timer
- Synchronous Internal 32-Bit Gated Timer
- Synchronous External 32-Bit

### 12.1 Additional Supported Features

- Selectable Clock Prescaler
- Timers Operational during CPU Idle
- ADC Event Trigger (only Timer3)
- Fast Bit Manipulation using CLR, SET and INV Registers

**FIGURE 12-1: TIMER2 AND TIMER3 BLOCK DIAGRAM (TYPE A, 16-BIT)**




**Note 1:** ADC Event Trigger is only available on Timer3.

**TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0260 | CCP2RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0270 | CCP2RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0280 | CCP2BUF | 31:16 | BUFH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | BUFL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0300 | CCP3CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | | 0000 |
| 0310 | CCP3CON2 | 31:16 | OENSYNC | — | OCFEN | OCEEN | OCDEN | OCCEN | OCBEN | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | | 0100 |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | | 0000 |
| 0320 | CCP3CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | OUTM<2:0> | | | — | — | POLACE | POLBDF | PSSACE<1:0> | | PSSBDF<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | DT<5:0> | | | | | | 0000 |
| 0330 | CCP3STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP | 0000 |
| | | 15:0 | — | — | — | — | — | ICGARM | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| 0340 | CCP3TMR | 31:16 | TMRH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | TMRL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0350 | CCP3PR | 31:16 | PRH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | PRL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0360 | CCP3RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0370 | CCP3RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0380 | CCP3BUF | 31:16 | BUFH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | BUFL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0400 | CCP4CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | | TRIGEN | ONESHOT | ALTSYNC | SYNC | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | | 0000 |
| 0410 | CCP4CON2 | 31:16 | OENSYNC | — | — | — | — | — | — | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | | 0100 |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | | 0000 |
| 0420 | CCP4CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | — | — | — | — | — | POLACE | — | PSSACE<1:0> | | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

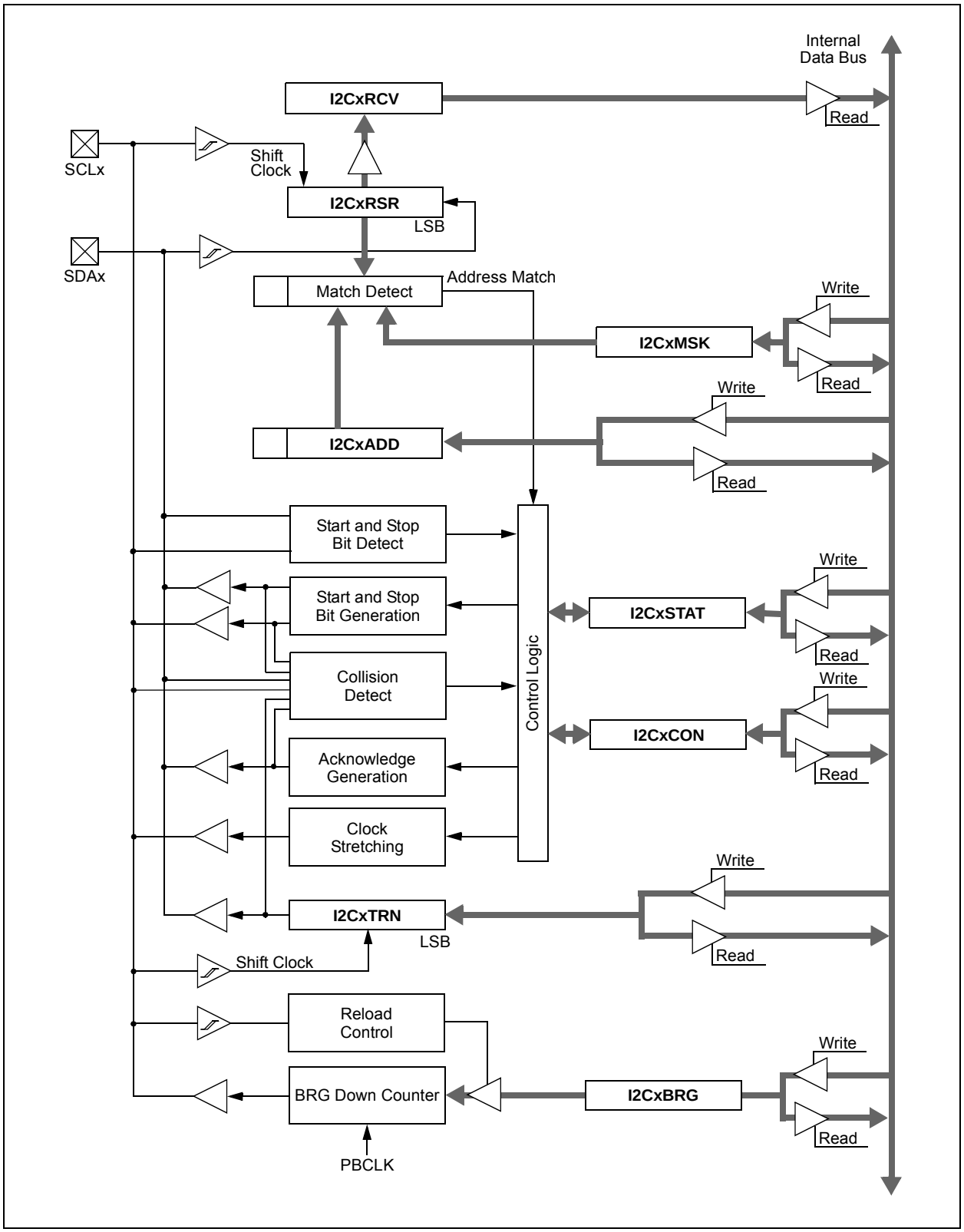
**TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0760 | CCP7RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0770 | CCP7RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0780 | CCP7BUF | 31:16 | BUFH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | BUFL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0800 | CCP8CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | | 0000 |
| 0810 | CCP8CON2 | 31:16 | OENSYNC | — | OCFEN | OCEEN | OCDEN | OCCEN | OCBEN | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | | 0100 |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | | 0000 |
| 0820 | CCP8CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | — | — | — | — | — | POLACE | — | PSSACE<1:0> | | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 0830 | CCP8STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | PRLWIP | TMRHWIP | TMRLWIP | RBWIP | RAWIP | 0000 |
| | | 15:0 | — | — | — | — | — | ICGARM | — | — | CCPTRIG | TRSET | TRCLR | ASEVT | SCEVT | ICDIS | ICOV | ICBNE | 0000 |
| 0840 | CCP8TMR | 31:16 | TMRH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | TMRL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0850 | CCP8PR | 31:16 | PRH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | PRL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0860 | CCP8RA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0870 | CCP8RB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CMPB<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0880 | CCP8BUF | 31:16 | BUFH<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | BUFL<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0900 | CCP9CON1 | 31:16 | OPSSRC | RTRGEN | — | — | OPS<3:0> | | | | TRIGEN | ONESHOT | ALTSYNC | SYNC<4:0> | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | CCPSLP | TMRSYNC | CLKSEL<2:0> | | | TMRPS<1:0> | | T32 | CCSEL | MOD<3:0> | | | | 0000 |
| 0910 | CCP9CON2 | 31:16 | OENSYNC | — | OCFEN | OCEEN | OCDEN | OCCEN | OCBEN | OCAEN | ICGSM<1:0> | | — | AUXOUT<1:0> | | ICS<2:0> | | | 0100 |
| | | 15:0 | PWMRSEN | ASDGM | — | SSDG | — | — | — | — | ASDG<7:0> | | | | | | | | 0000 |
| 0920 | CCP9CON3 | 31:16 | OETRIG | OSCNT<2:0> | | | — | — | — | — | — | — | POLACE | — | PSSACE<1:0> | | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

**FIGURE 16-1: I2Cx BLOCK DIAGRAM**



**REGISTER 17-1: UxMODE: UARTx MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | SLPEN | ACTIVE | — | — | — | CLKSEL<1:0> | | OVFDIS |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0>(1) | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **SLPEN:** UARTx Run During Sleep Enable bit
- 1 = UARTx clock runs during Sleep
- 0 = UARTx clock is turned off during Sleep

bit 22 **ACTIVE:** UARTx Running Status bit
- 1 = UARTx is active (UxMODE register shouldn't be updated)
- 0 = UARTx is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-17 **CLKSEL:** UARTx Clock Selection bits
- 11 = The UARTx clock is the Reference Output (REFO1) clock
- 10 = The UARTx clock is the FRC oscillator clock
- 01 = The UARTx clock is the SYSCLK
- 00 = The UARTx clock is the PBCLK

bit 16 **OVFDIS:** Run During Overflow Condition Mode bit
- 1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized
- 0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx is enabled; UARTx pins are controlled by UARTx, as defined by the UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled; all UARTx pins are controlled by the corresponding bits in the PORTx, TRISx and LATx registers, UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues operation when device enters Idle mode
- 0 = Continues operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

**Note 1:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

## 18.0 USB ON-THE-GO (OTG)

**Note 1:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS61126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation, with a minimum of external components. This module in Host mode is intended for use as an embedded host, and therefore, does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA Controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 18-1.

### 18.1 Reclaiming USB Pins When the USB Module is Operating

Select USB pins that are not used on all USB operating modes (USBID and VBUSON) can be reclaimed when the module is operating in a mode that does not require them. These pins can be reclaimed by clearing the appropriate device Configuration bit (refer to Register 26-1).

For example:

- USBID and VBUSON can be reclaimed in Device mode
- VBUSON can be reclaimed in Host mode if it is not used for the power VBUS control

### 18.2 Reclaiming USB Pins When the USB Module is Disabled

All USB signaling pins, D+, D-, VBUS, VBUSON and USBID, can be reclaimed and used for GPIO or other peripherals if available on the pin when the USB module is disabled. For proper operation of the RB10 and RB11 pins, the USB module must be disabled, but powered. Refer to **Section 18.1 "Reclaiming USB Pins When the USB Module is Operating"** for more information.

### 18.3 Introduction

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The dedicated USB DMA Controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Support for Host and Device
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking performed by Hardware
- Endpoint Buffering anywhere in System RAM
- Integrated DMA to access System RAM and Flash

**Note:** The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

**Note:** Adding any circuitry to the USB D+/D- pins, other than the connection to a USB connector, may degrade the USB signal quality and violate USB specifications.

**REGISTER 19-4: RTCTIME/ALMTIME: RTCC TIME/ALARM REGISTERS**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | HRTEN<2:0> | | | HRONE<3:0> | | | |
| 23:16 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | MINTEN<2:0> | | | MINONE<3:0> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SECTEN<3:0> | | | | SECONE<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.

bit 15-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 26-8: DEVID: DEVICE ID REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | VER<3:0>(1) | | | | ID<27:24>(1) | | | |
| 23:16 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<23:16>(1) | | | | | | | |
| 15:8 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<15:8>(1) | | | | | | | |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | ID<7:0>(1) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

**Note 1:** Reset values are dependent on the device variant.

**REGISTER 26-9: SYSKEY: SYSTEM UNLOCK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<31:24> | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<23:16> | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | SYSKEY<15:8> | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | R/W-1 |
| | SYSKEY<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

A write of 0xAA996655, followed by a write of 0x556699AA to SYSKEY, is required to unlock select system registers. Refer to Example 26-1.

Bit 0 Indicates System Lock Status:

1 = The system is unlocked

0 = The system is locked

## 28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

### 28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker