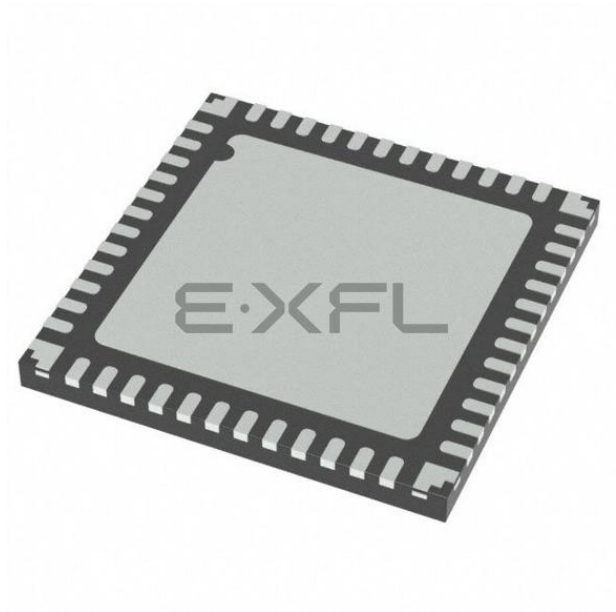
Microchip Technology - PIC32MM0064GPM048-I/M4 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm048-i-m4

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R-1
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC
15:8	R-0	R-1	R-1	R-1	U-0	U-0	U-0	R-0
	ISA<1:0>		ULRI	RXI	—	—	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '0'

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8 bits in width

bit 20-18 **MMAR<2:0>:** microMIPS™ Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit
1 = microMIPS is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits
01 = Only microMIPS is implemented

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace™ Hardware is Present bit
0 = The iFlowtrace hardware is not implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4-Kbyte page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1, HS	R/W-1, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	U-0
	—	—	—	—	—	—	CMR	—
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR(1)	SWR(1)	—	WDTO(1)	SLEEP(1)	IDLE(1,2)	BOR(1)	POR(1)

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PORIO:** VDD POR Flag bit
Set by hardware at detection of a VDD POR event.
1 = A Power-on Reset has occurred due to VDD voltage
0 = A Power-on Reset has not occurred due to VDD voltage

bit 30 **PORCORE:** Core Voltage POR Flag bit
Set by hardware at detection of a core POR event.
1 = A Power-on Reset has occurred due to core voltage
0 = A Power-on Reset has not occurred due to core voltage

bit 29-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary Configuration registers
0 = No error occurred during a read of the Primary Configuration registers

bit 26 **BCFGFAIL:** Primary/Alternate Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary and Alternate Configuration registers
0 = No error occurred during a read of the Primary and Alternate Configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit(1)
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit(1)
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit(1)
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: User software must clear these bits to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep.

REGISTER 8-14: DCHxSPTR: DMA CHANNEL x SOURCE POINTER REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to Byte 65,535 of the source

•

•

•

0000000000000001 = Points to Byte 1 of the source

0000000000000000 = Points to Byte 0 of the source

Note 1: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 8-15: DCHxDPTR: DMA CHANNEL x DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to Byte 65,535 of the destination

•

•

•

0000000000000001 = Points to Byte 1 of the destination

0000000000000000 = Points to Byte 0 of the destination

12.0 TIMER2 AND TIMER3

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-Bit Timer
- Synchronous Internal 16-Bit Gated Timer
- Synchronous External 16-Bit Timer

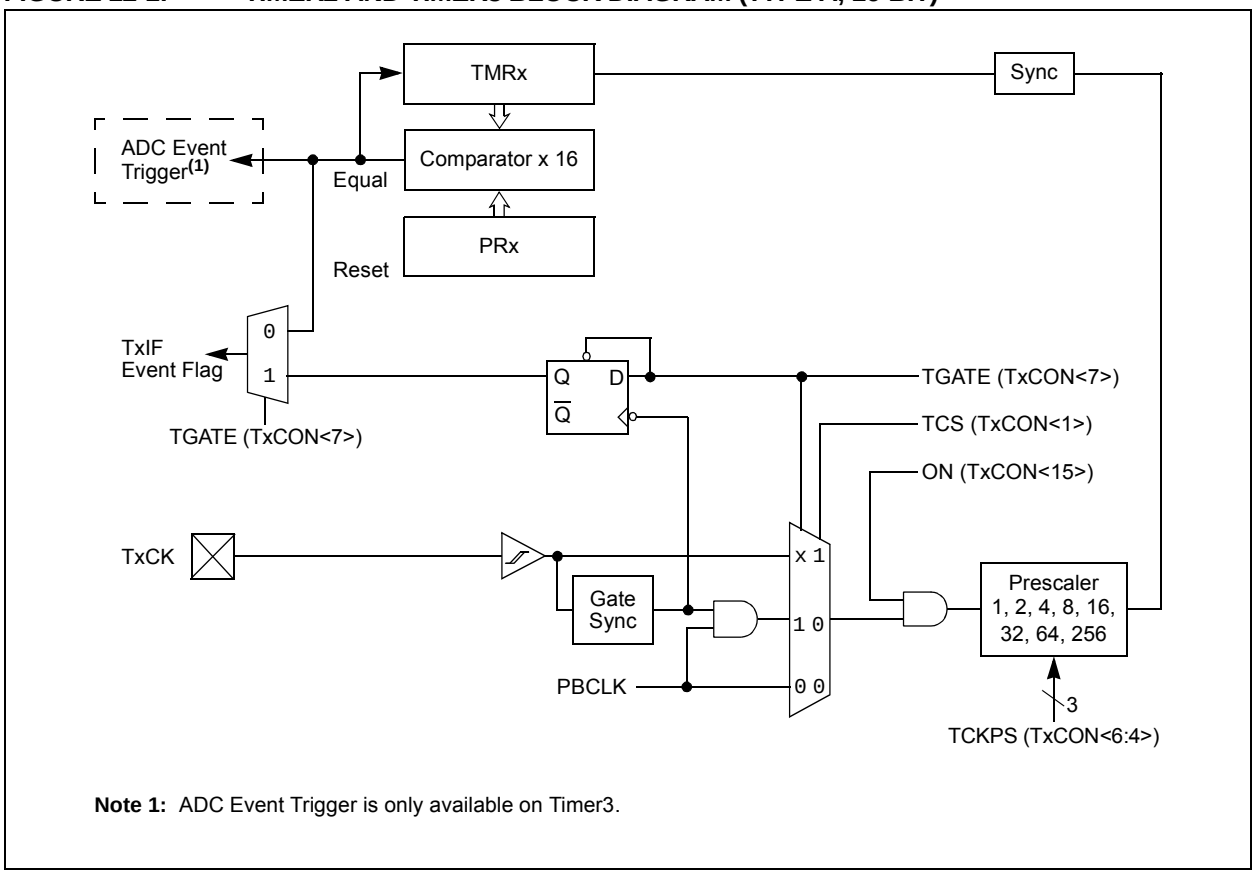
A single 32-bit synchronous timer is available by combining Timer2 with Timer3. The resulting 32-bit timer can operate in three modes:

- Synchronous Internal 32-Bit Timer
- Synchronous Internal 32-Bit Gated Timer
- Synchronous External 32-Bit

12.1 Additional Supported Features

- Selectable Clock Prescaler
- Timers Operational during CPU Idle
- ADC Event Trigger (only Timer3)
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 12-1: TIMER2 AND TIMER3 BLOCK DIAGRAM (TYPE A, 16-BIT)



Note 1: ADC Event Trigger is only available on Timer3.

13.0 WATCHDOG TIMER (WDT)

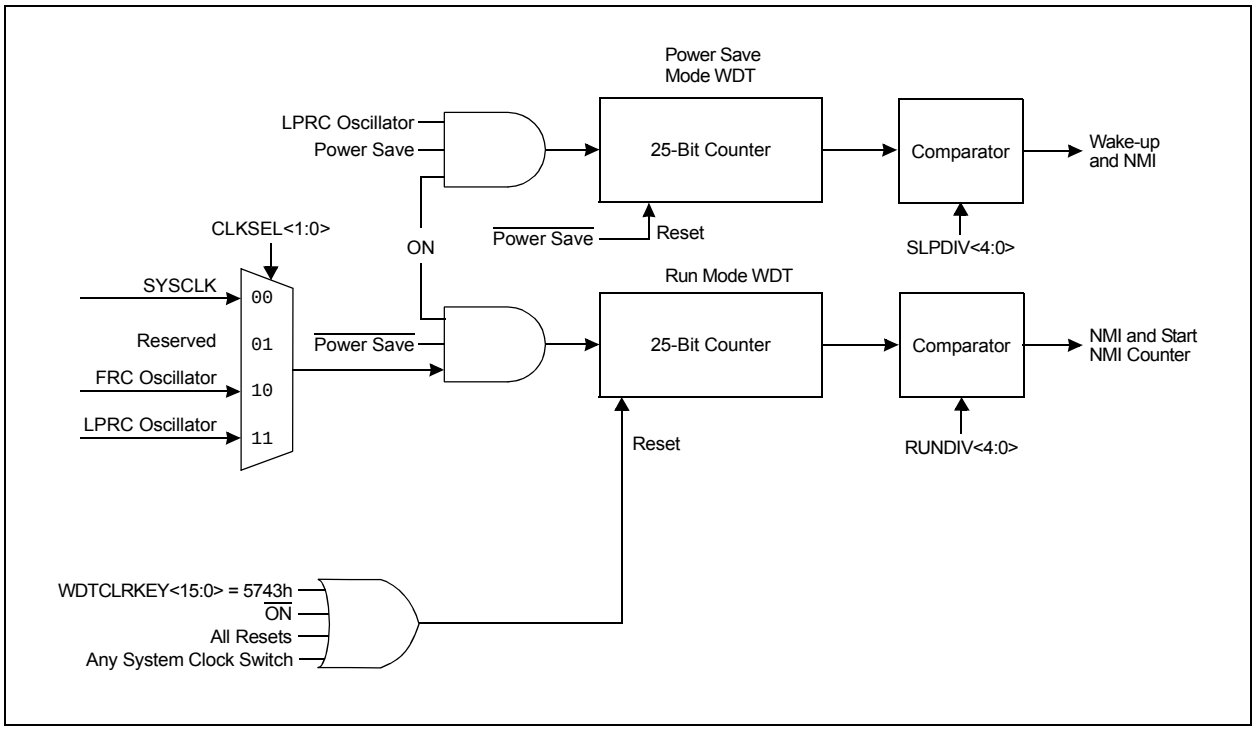
Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 13-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFO1 is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit(4)
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at end of data output time
0 = Input data is sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

20.0 12-BIT ADC CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

20.1 Introduction

The 12-bit ADC Converter with Threshold Detect includes the following features:

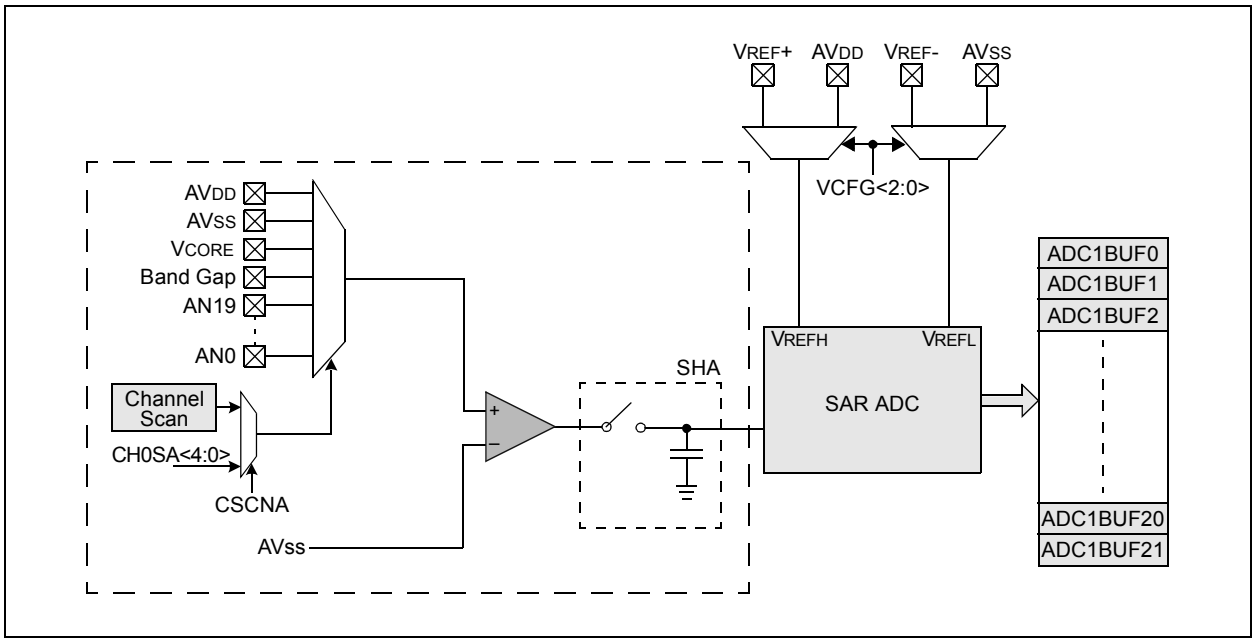
- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 300 ksps
- User-Selectable Resolution of 10 or 12 bits
- Up to 24 Analog Inputs (internal and external)
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold Amplifier (SHA)
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length Configurable Conversion Result Buffer
- Eight Options for Result Alignment and Encoding
- Configurable Interrupt Generation
- Operation during CPU Sleep and Idle modes

Figure 20-1 illustrates a block diagram of the 12-bit ADC. The 12-bit ADC has external analog inputs, AN0 through AN19, and 4 internal analog inputs connected to VDD, VSS, VCORE and band gap. In addition, there are two analog input pins for external voltage reference connections.

The analog inputs are connected through a multiplexer to the SHA. Unipolar differential conversions are possible on all inputs (see Figure 20-1).

The Automatic Input Scan mode sequentially converts multiple analog inputs. A special control register specifies which inputs will be included in the scanning sequence. The 12-bit ADC is connected to a 22-word result buffer. The 12-bit result is converted to one of eight output formats in either 32-bit or 16-bit word widths.

FIGURE 20-1: ADC BLOCK DIAGRAM



REGISTER 20-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC V_{R+}	ADC V_{R-}
000	AV_{DD}	AV_{SS}
001	AV_{DD}	External V_{REF-} Pin
010	External V_{REF+} Pin	AV_{SS}
011	External V_{REF+} Pin	External V_{REF-} Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ SHA Input for Input Multiplexer Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1 (ADC buffers split into 2 x 11-word buffers).
1 = ADC is currently filling Buffers 11-21, user should access data in 0-10
0 = ADC is currently filling Buffers 0-10, user should access data in 11-21

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 11-word buffers, ADC1BUF(0...10), ADC1BUF(11...21)
0 = Buffer configured as one 22-word buffer, ADC1BUF(0...21)

bit 0 **Unimplemented:** Read as '0'

TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name	Register Name and Bit Location
Universal Asynchronous Receiver Transmitter 2 (UART2)	U2MD	PMD5<1>
Universal Asynchronous Receiver Transmitter 3 (UART3)	U3MD	PMD5<2>
Serial Peripheral Interface 1 (SPI1)	SPI1MD	PMD5<8>
Serial Peripheral Interface 2 (SPI2)	SPI2MD	PMD5<9>
Serial Peripheral Interface 3 (SPI3)	SPI3MD	PMD5<10>
Inter-Integrated Circuit Interface 1 (I2C1)	I2C1MD	PMD5<16>
Inter-Integrated Circuit Interface 2 (I2C2)	I2C2MD	PMD5<17>
Inter-Integrated Circuit Interface 3 (I2C3)	I2C3MD	PMD5<18>
Universal Serial Bus (USB)	USBMD	PMD5<24>
Real-Time Clock and Calendar (RTCC)	RTCCMD	PMD6<0>
Reference Clock Output (REFO1)	REFOMD	PMD6<8>
Direct Memory Access (DMA)	DMAMD	PMD7<4>

NOTES:

The registers that require this unlocking sequence are listed in the Table 26-2.

TABLE 26-2: SYSTEM LOCKED REGISTERS

Register Name	Register Description	Peripheral
OSCCON	Oscillator Control	Oscillator
SPLLCON	System PLL Control	Oscillator
OSCTUN	FRC Tuning	Oscillator
PMDCON	Peripheral Module Disable Control	PMD
RSWRST	Software Reset	Reset
RPCON	Peripheral Pin Select Configuration	I/O Ports
PWRCON	Sleep Power Control	System
RTCCON1	RTCC Control	RTCC

The SYSKEY register read value indicates the status. A value of '0' indicates that the system registers are locked. A value of '1' indicates that the system registers are unlocked. For more information about the SYSKEY register refer to Table 26-5 and Register 26-9.

26.5 Band Gap Voltage Reference

PIC32MM0256GPM064 family devices have a precision voltage reference band gap circuit used by many modules. The analog buffers are implemented between the band gap circuit and these modules. The buffers are automatically enabled by the hardware if some part of the device needs the band gap reference. The stabilization time is required when the buffer is switched on. The software can enable these buffers in advance to allow the band gap voltage to stabilize before the module uses it. The ANGFG register contains bits to enable the band gap buffers for the comparators (VBGCMP bit) and ADC (VBGADC bit). Refer to Table 26-6 and Register 26-10 for more information.

26.6 Programming and Diagnostics

PIC32MM0256GPM064 family devices provide a complete range of programming and diagnostic features:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

26.7 Unique Device Identifier (UDID)

PIC32MM0256GPM064 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 32-bit program words. When taken together, these fields form a unique 160-bit identifier.

The UDID is stored in five read-only locations, located from 0xBFC41840 to 0xBFC41850 in the device configuration space. Table 26-7 lists the addresses of the Identifier Words.

26.8 Reserved Registers

PIC32MM0256GPM064 family devices have 3 reserved registers, located at 0xBF800400, 0xBF800480 and 0xBF802280. The application code must not modify these reserved locations. Table 26-8 lists the addresses of these reserved registers.

TABLE 26-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

28.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

28.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

28.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MM0256GPM064 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MM0256GPM064 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any general purpose digital or analog pin (not 5.5V tolerant) with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any general purpose digital or analog pin (5.5V tolerant) with respect to V_{SS}:
When V_{DD} = 0V: ..... -0.3V to +4.0V
When $V_{DD} \geq$ 2.0V: ..... -0.3V to +6.0V
Voltage on AV_{DD} with respect to V_{DD} ..... (V_{DD} – 0.3V) to (lesser of: 4.0V or (V_{DD} + 0.3V))
Voltage on AV_{SS} with respect to V_{SS} ..... -0.3V to +0.3V
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin(1) ..... 300 mA
Maximum output current sunk by I/O pin ..... 11 mA
Maximum output current sourced by I/O pin ..... 16 mA
Maximum output current sunk by I/O pin with increased current drive strength
(RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) ..... 17 mA
Maximum output current sourced by I/O pin with increased current drive strength
(RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) ..... 24 mA
Maximum current sunk by all ports ..... 300 mA
Maximum current sourced by all ports(1) ..... 300 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 29-1).

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 29-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	.21	V	IOL = 5.0 mA, VDD = 2V
DO16		OSC2/CLKO	—	—	.16	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	.12	V	IOL = 5.0 mA, VDD = 2V
	VOH	**Output High Voltage**					
DO20		I/O Ports	3.25	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2V
DO26		OSC2/CLKO	3.3	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.55	—	—	V	IOH = -1.0 mA, VDD = 2V

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

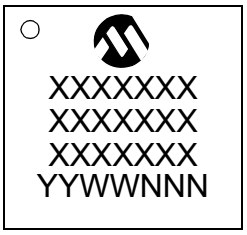
TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
		Program Flash Memory					
D130	EP	Cell Endurance	10000	20000	—	E/W	
D131	VPR	VDD for Read	2.0	—	3.6	V	
D132B		VDD for Self-Timed Write	2.0	—	3.6	V	
D133A	TIW	Self-Timed Double-Word Write Cycle Time	61.4	62.5	63.6	μs	8 bytes, data is not all '1's
		Self-Timed Row Write Cycle Time	1.41	1.44	1.47	ms	512 bytes, data is not all '1's; SYSCLK > 2 MHz
D133B	TIE	Self-Timed Page Erase Time	4.18	4.26	4.33	ms	2048 bytes
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D136	TCE	Self-Timed Chip Erase Time	16.6	16.9	17.3	ms	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

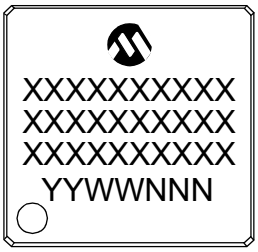
30.1 Package Marking Information (Continued)

40-Lead UQFN (5x5x0.5 mm)



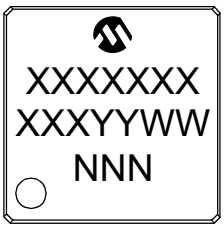
Example

48-Lead UQFN (6x6 mm)



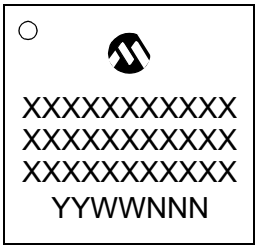
Example

48-Lead TQFP (7x7x1.0 mm)



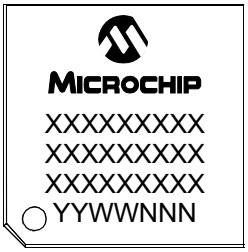
Example

64-Lead QFN (9x9x0.9 mm)

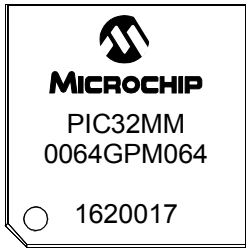


Example

64-Lead TQFP (10x10x1 mm)

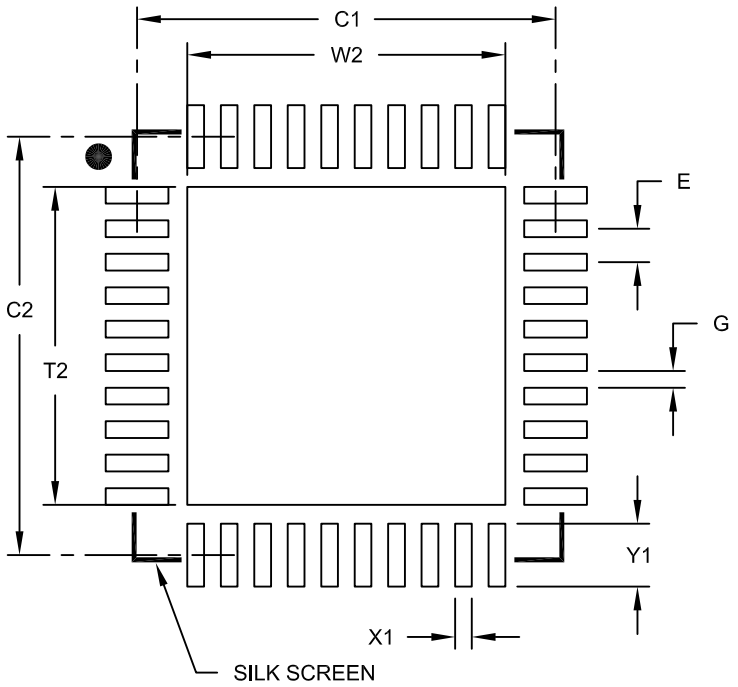


Example



40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

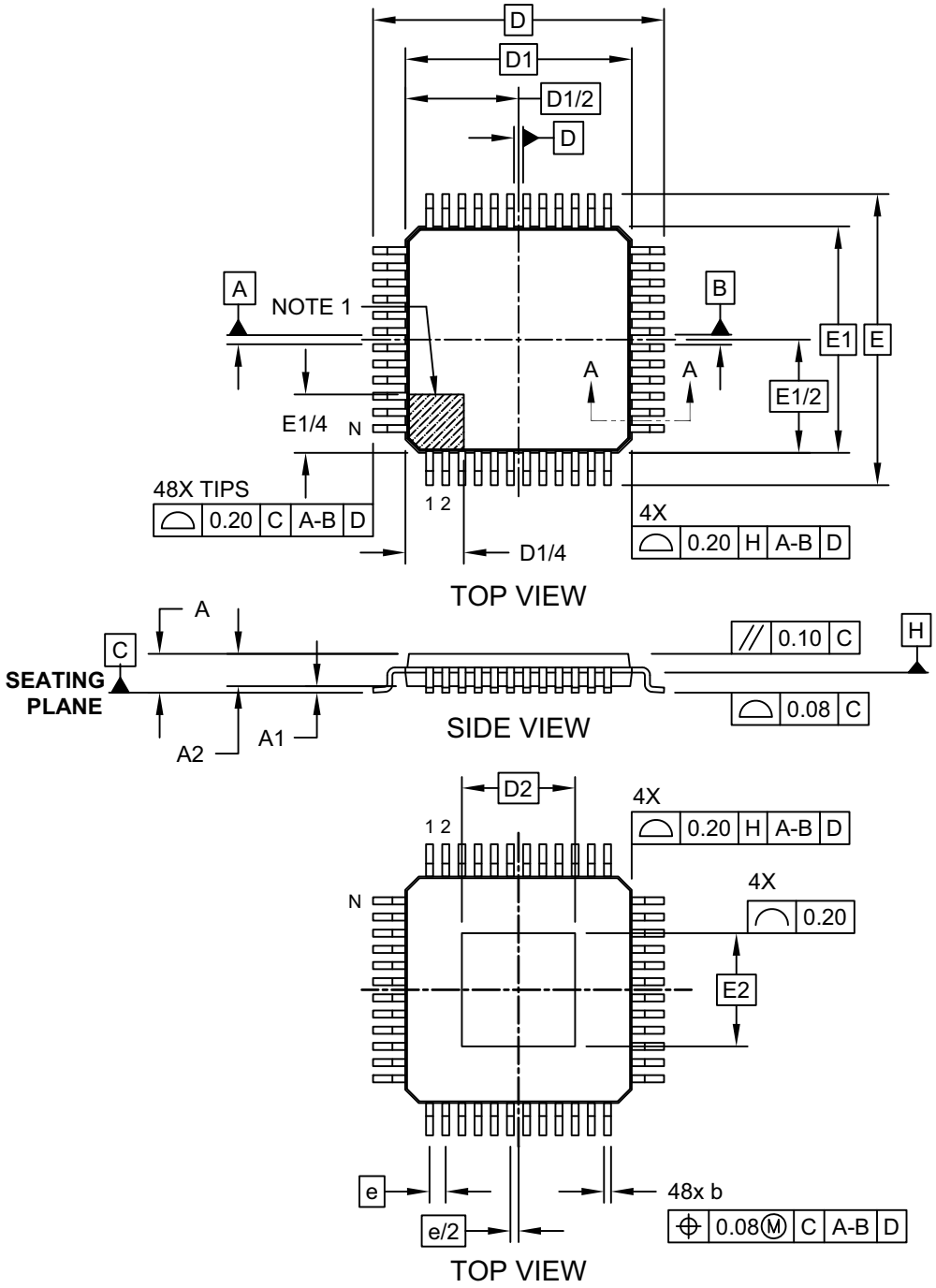
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-183A Sheet 1 of 2

NOTES: