Microchip Technology - PIC32MM0064GPM048-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP Exposed Pad
Supplier Device Package	48-TQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm048-i-pt

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RA0	2	27	33	36	21	11	I/O	ST/DIG	PORTA digital I/Os
RA1	3	28	34	37	22	12	I/O	ST/DIG	
RA2	9	6	7	7	32	25	I/O	ST/DIG	
RA3	10	7	8	8	33	26	I/O	ST/DIG	
RA4	12	9	10	10	36	29	I/O	ST/DIG	
RA5	—	—	—	—	—	54	I/O	ST/DIG	
RA6	—	—	—	—	20	10	I/O	ST/DIG	
RA7	—	—	—	—	14	1	I/O	ST/DIG	
RA8	—	—	—	—	34	27	I/O	ST/DIG	
RA9	—	—	11	11	37	30	I/O	ST/DIG	
RA10	—	—	—	—	13	64	I/O	ST/DIG	
RA11	—	—	—	—	—	8	I/O	ST/DIG	
RA12	—	—	—	—	—	7	I/O	ST/DIG	
RA13	—	—	—	—	—	6	I/O	ST/DIG	
RA14	—	—	—	—	—	59	I/O	ST/DIG	
RA15	—	—	—	—	8	58	I/O	ST/DIG	
RB0	4	1	35	38	23	13	I/O	ST/DIG	PORTB digital I/Os
RB1	5	2	36	39	24	14	I/O	ST/DIG	
RB2	6	3	1	1	25	15	I/O	ST/DIG	
RB3	7	4	2	2	26	16	I/O	ST/DIG	
RB4	11	8	9	9	35	28	I/O	ST/DIG	
RB5	14	11	15	15	45	43	I/O	ST/DIG	
RB6	15	12	16	16	46	44	I/O	ST/DIG	
RB7	16	13	17	17	47	46	I/O	ST/DIG	
RB8	17	14	18	18	48	48	I/O	ST/DIG	
RB9	18	15	19	20	1	49	I/O	ST/DIG	
RB10	21	18	24	27	9	60	I/O	ST/DIG	
RB11	22	19	25	28	10	61	I/O	ST/DIG	
RB13	24	21	27	30	12	63	I/O	ST/DIG	
RB14	25	22	28	31	15	2	I/O	ST/DIG	
RB15	26	23	29	32	16	3	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	r-0	U-0	U-0	U-0
	WR(1,3)	WREN(1)	WRERR(1,2)	LVDERR(1,2)	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1,3)

This bit cannot be cleared and can be set only when WREN = 1, and the unlock sequence has been performed.
1 = Initiates a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enables writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disables writes to the WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1,2)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage is detected (possible data corruption if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **Reserved:** Maintain as '0'

bit 10-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

2: These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).

3: This bit is only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

REGISTER 5-4: NVMDATAx: FLASH DATA x REGISTER (x = 0-1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATAx<31:0>:** Flash Data x bits

Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
26E0	RCON	31:16	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	C000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0003
26F0	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
2700	RNMICON	31:16	—	—	—	—	—	—	—	WDTR	SWNMI	—	—	—	GNMI	—	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
2710	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	SBOREN	RETEN	VREGS	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 8-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** DMA Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

REGISTER 8-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

11.1 Timer1 Control Register

TABLE 11-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
8010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
8020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>(2)																FFFF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

2: PR1 values of '0' and '1' are reserved.

12.0 TIMER2 AND TIMER3

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-Bit Timer
- Synchronous Internal 16-Bit Gated Timer
- Synchronous External 16-Bit Timer

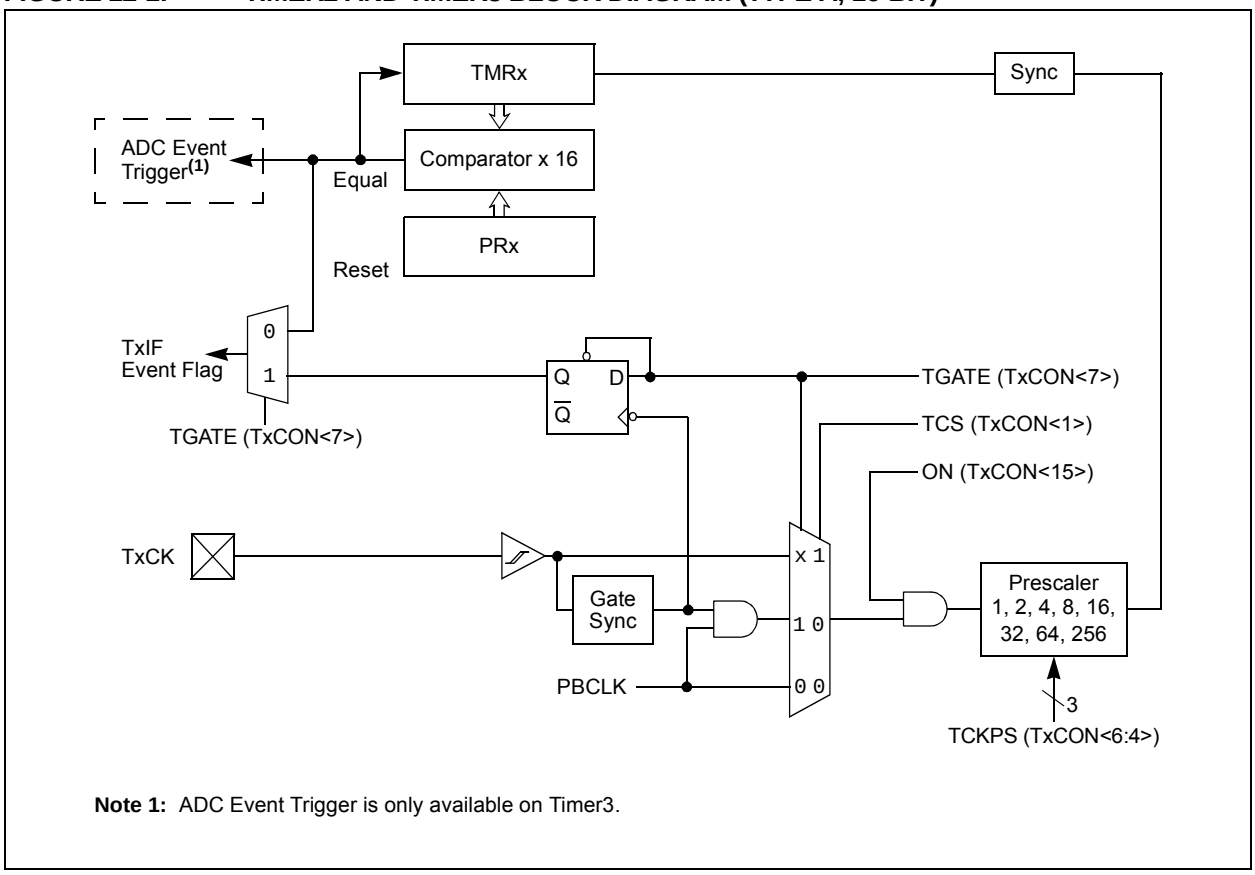
A single 32-bit synchronous timer is available by combining Timer2 with Timer3. The resulting 32-bit timer can operate in three modes:

- Synchronous Internal 32-Bit Timer
- Synchronous Internal 32-Bit Gated Timer
- Synchronous External 32-Bit

12.1 Additional Supported Features

- Selectable Clock Prescaler
- Timers Operational during CPU Idle
- ADC Event Trigger (only Timer3)
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 12-1: TIMER2 AND TIMER3 BLOCK DIAGRAM (TYPE A, 16-BIT)



Note 1: ADC Event Trigger is only available on Timer3.

REGISTER 18-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low speed
0 = Next token command to be executed at full speed

bit 6-0 **DEVADDR<6:0>:** 7-Bit USB Device Address bits

REGISTER 18-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
- 1 = Eye pattern test is enabled
- 0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
- 1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
- 0 = $\overline{OE}$ signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** USB Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 3 **LSDEV:** USB Low-Speed Device Enable bit
- 1 = USB macro operates in Low-Speed Device Only mode
- 0 = USB macro operates in OTG, Host or Fast Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
- 1 = USB module automatically suspends upon entry to Sleep mode; see the USUSPEND bit (U1PWRC<1>) in Register 18-5
- 0 = USB module does not automatically suspend upon entry to Sleep mode; software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

19.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

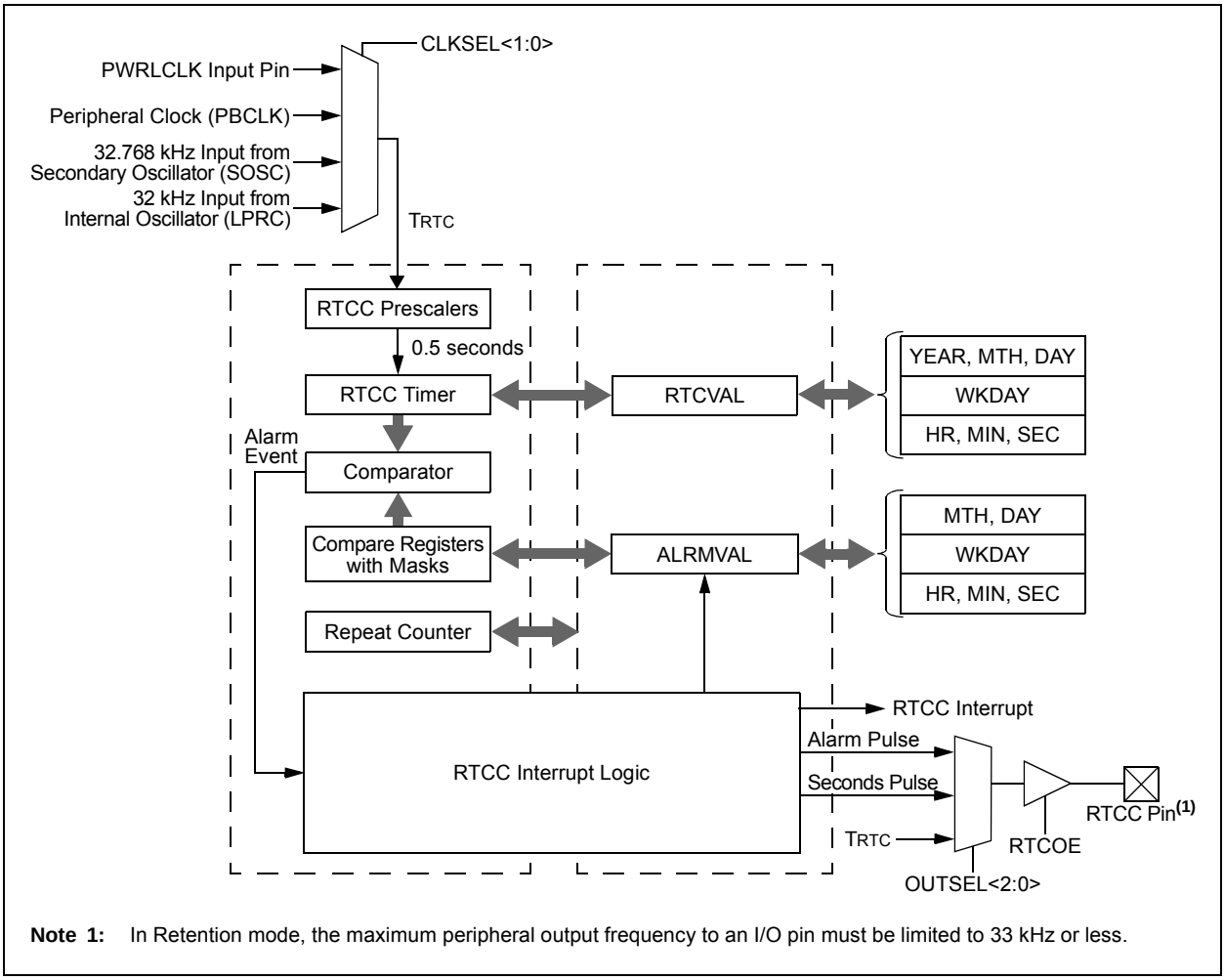
Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. "RTCC with Timestamp"** (DS60001362) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Key features of the RTCC module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Visibility of One-Half Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are Configurable for Half of a Second, 1 Second, 10 Seconds, 1 Minute, 10 Minutes, 1 Hour, 1 Day, 1 Week, 1 Month and 1 Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Uses External 32.768 kHz Crystal, 32 kHz Internal Oscillator, PWRLCLK Input Pin or Peripheral Clock
- Alarm Pulse, Seconds Clock or Internal Clock Output on RTCC Pin

FIGURE 19-1: RTCC BLOCK DIAGRAM



Note 1: In Retention mode, the maximum peripheral output frequency to an I/O pin must be limited to 33 kHz or less.

REGISTER 20-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 7-4 **SSRC<3:0>:** Conversion Trigger Source Select bits
1111 = CLC2 module event ends sampling and starts conversion
1110 = CLC1 module event ends sampling and starts conversion
1101 = SCCP6 module event ends sampling and starts conversion
1100 = SCCP5 module event ends sampling and starts conversion
1011 = SCCP4 module event ends sampling and starts conversion
1010 = MCCP3 module event ends sampling and starts conversion
1001 = MCCP2 module event ends sampling and starts conversion
1000 = MCCP1 module event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
0100-0011 = Reserved
0010 = Timer3 period match ends sampling and starts conversion
0001 = Active transition on INT0 pin ends sampling and starts conversion
0000 = Clearing the SAMP bit ends sampling and starts conversion

bit 3 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit ADC operation
0 = 10-bit ADC operation

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

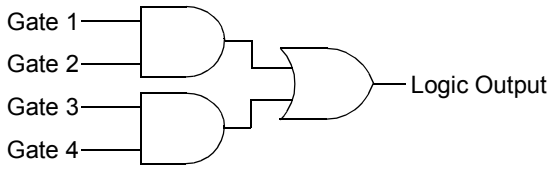
bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
0 = The ADC SHA is holding
When ASAM = 0, writing '1' to this bit starts sampling. When SSRC<3:0 = 0000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** ADC Conversion Status bit(1)
1 = Analog-to-Digital conversion is done
0 = Analog-to-Digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.
2: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).

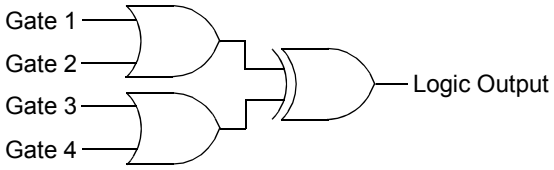
FIGURE 21-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

AND – OR



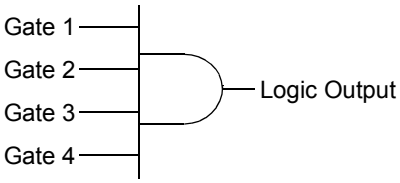
MODE<2:0> = 000

OR – XOR



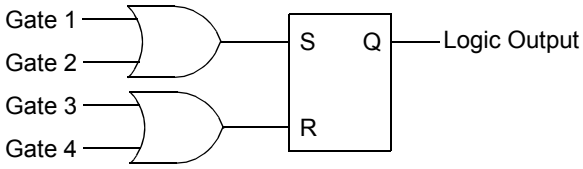
MODE<2:0> = 001

4-Input AND



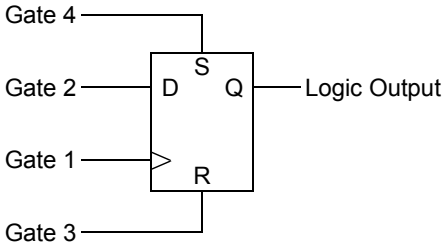
MODE<2:0> = 010

S-R Latch



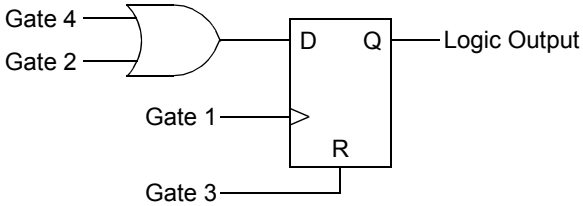
MODE<2:0> = 011

1-Input D Flip-Flop with S and R



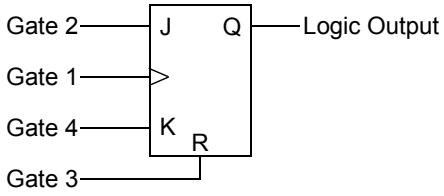
MODE<2:0> = 100

2-Input D Flip-Flop with R



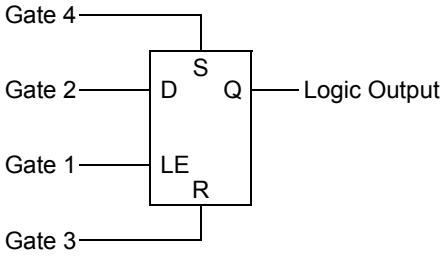
MODE<2:0> = 101

J-K Flip-Flop with R



MODE<2:0> = 110

1-Input Transparent Latch with S and R



MODE<2:0> = 111

21.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCON
- CLCxSEL
- CLCxGLS

The CLCx Control register (CLCxCON) is used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Source Select register (CLCxSEL) allows the user to select up to 4 data input sources using the 4 data input selection multiplexers. Each multiplexer has a list of 8 data sources available.

The CLCx Gate Logic Select register (CLCxGLS) allows the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these 8 signals are enabled, ORed together by the logic cell input gates.

REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	HLVDL<3:0>			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** HLVD Power Enable bit
- 1 = HLVD is enabled
- 0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** HLVD Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **VDIR:** Voltage Change Direction Select bit
- 1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
- 0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 10 **BGVST:** Band Gap Voltage Stable Flag bit
- 1 = Indicates that the band gap voltage is stable
- 0 = Indicates that the band gap voltage is unstable

bit 9 **IRVST:** Internal Reference Voltage Stable Flag bit
- 1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
- 0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 8 **HLEVT:** High/Low-Voltage Detection Event Status bit
- 1 = Indicates HLVD event is active
- 0 = Indicates HLVD event is not active

bit 7-4 **Unimplemented:** Read as '0'

REGISTER 26-1: FDEVOPT/AFDEVOPT: DEVICE OPTIONS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							
15:8	R/P	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	FVBUSIO	FUSBIDIO	—	—	—	—	—	—
7:0	r-1	r-1	r-1	R/P	R/P	r-1	r-1	r-1
	—	—	—	ALTI2C	SOSCHP	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **USERID<15:0>:** User ID bits (2 bytes which can programmed to any value)

bit 15 **FVBUSIO:** USB VBUS_ON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 14 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

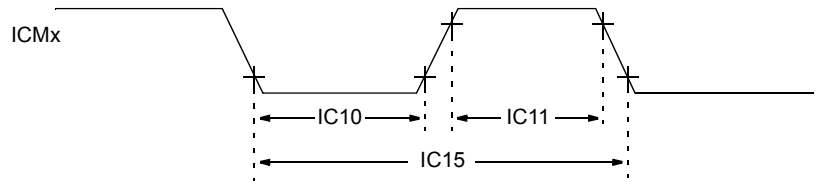
bit 13-5 **Reserved:** Program as '1'

bit 4 **ALTI2C:** Alternate I2C1 Location Select bit
1 = SDA1 and SCL1 are on pins, RB8 and RB9
0 = SDA1 and SCL1 are moved to alternate I^2C locations, RB5 and RC9

bit 3 **SOSCHP:** Secondary Oscillator (SOSC) High-Power Enable bit
1 = SOSC operates in normal power mode
0 = SOSC operates in High-Power mode

bit 2-0 **Reserved:** Program as '1'

FIGURE 29-6: MCCP AND SCCP INPUT CAPTURE MODE TIMING CHARACTERISTICS



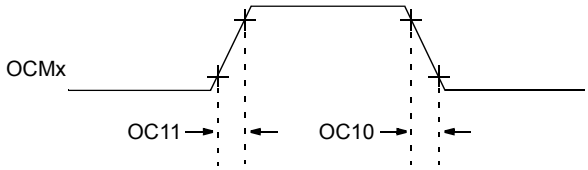
Note: Refer to Figure 29-2 for load conditions.

TABLE 29-25: MCCP AND SCCP INPUT CAPTURE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**
IC10	TccL	ICMx Input Low Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC11	TccH	ICMx Input High Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC15	TccP	ICMx Input Period	[(25 ns or 2 TPBCLK)/N] + 50 ns	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 29-7: MCCP AND SCCP OUTPUT COMPARE MODE TIMING CHARACTERISTICS



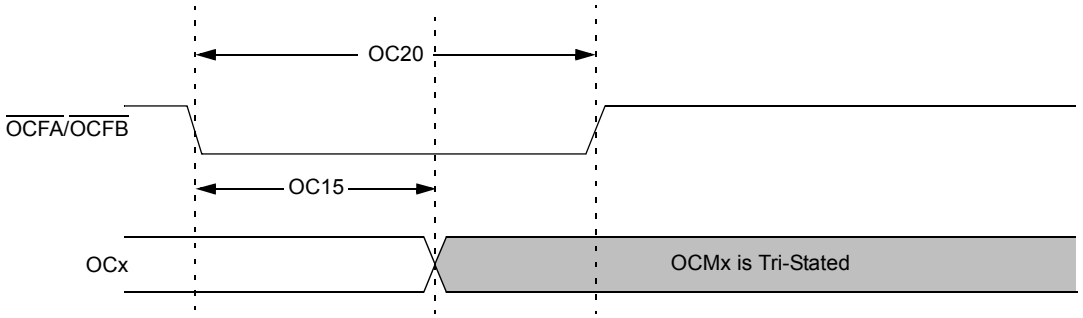
Note: Refer to Figure 29-2 for load conditions.

TABLE 29-26: MCCP AND SCCP OUTPUT COMPARE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCMx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCMx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 29-8: MCCP AND SCCP PWM MODE TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	10	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics(1)	Min.	Typical(2)	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.0V
			—	—	15	ns	VDD < 2.0V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(4)	2.5	—	12	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	
SP60	TssL2doV	$\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

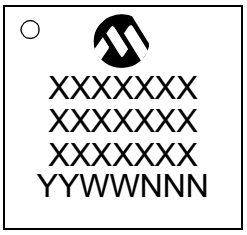
2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 10 pF load on all SPIx pins.

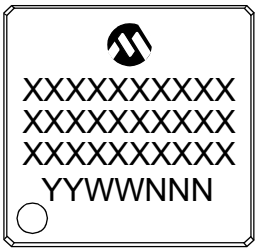
30.1 Package Marking Information (Continued)

40-Lead UQFN (5x5x0.5 mm)



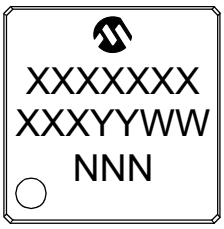
Example

48-Lead UQFN (6x6 mm)



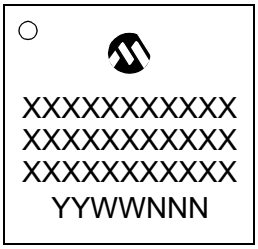
Example

48-Lead TQFP (7x7x1.0 mm)



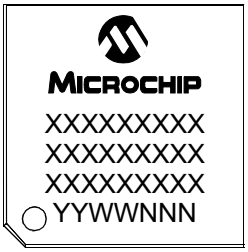
Example

64-Lead QFN (9x9x0.9 mm)

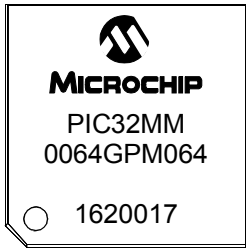


Example

64-Lead TQFP (10x10x1 mm)

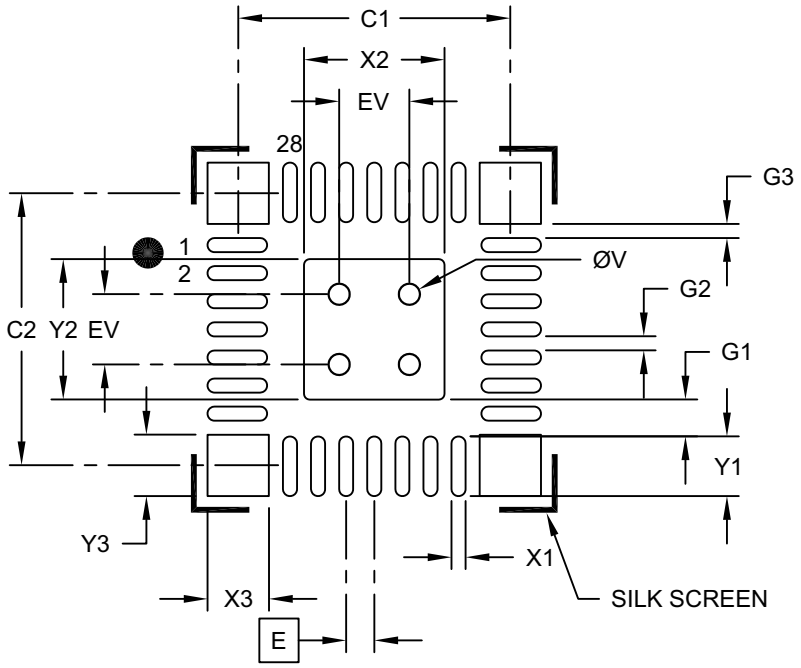


Example



28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			2.00
Center Pad Length	Y2			2.00
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.85
Contact Pad to Center Pad (X28)	G1		0.52	
Contact Pad to Pad (X24)	G2	0.20		
Contact Pad to Corner Pad (X8)	G3	0.20		
Corner Anchor Width (X4)	X3			0.78
Corner Anchor Length (X4)	Y3			0.78
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2333-M6 Rev B