# Microchip Technology - PIC32MM0064GPM048T-I/PT Datasheet

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | IrDA, LINbus, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 17x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP Exposed Pad |
| Supplier Device Package | 48-TQFP-EP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm048t-i-pt |

**TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN QFN/TQFP DEVICES**

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | **RP21**/SDI3/RA7 | 33 | OCM3B/RD3 |
| 2 | CVREF/AN9/C3INB/**RP16**/VBUSON/RB14 | 34 | REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1) |
| 3 | AN10/C3INA/REFCLKO/**RP17**/RB15(1) | 35 | OCM2B/RC3 |
| 4 | AVSS | 36 | OCM1E/INT3/RC4 |
| 5 | AVDD | 37 | AN15/OCM1D/RC5 |
| 6 | AN16/$\overline{\text{U1CTS}}$/RA13 | 38 | VSS |
| 7 | AN17/OCM1A/RA12 | 39 | VDD |
| 8 | AN18/RA11 | 40 | U1TX/RC12 |
| 9 | $\overline{\text{MCLR}}$ | 41 | OCM3D/RC14 |
| 10 | AN19/U1RX/RA6 | 42 | OCM3E/RC15 |
| 11 | PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0 | 43 | PGED3/**RP11**/ASDA1(2)/USBID/RB5 |
| 12 | PGED2/VREF-/AN1/**RP2**/OCM1F/RA1 | 44 | VBUS/RB6 |
| 13 | PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0 | 45 | OCM3F/RC10 |
| 14 | PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1 | 46 | **RP12**/SDA3/RB7 |
| 15 | AN4/C1INB/**RP8**/SDA2/OCM2E/RB2 | 47 | SCK1/RC13(1) |
| 16 | TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3 | 48 | TCK/**RP13**/SCL1/RB8(1) |
| 17 | VDD | 49 | TMS/**RP14**/SDA1/INT2/RB9(1) |
| 18 | VSS | 50 | **RP23**/RC6 |
| 19 | AN12/C2IND/T2CK/T2G/RC0 | 51 | **RP20**/RC7 |
| 20 | AN13/T3CK/T3G/RC1 | 52 | AN14/LVDIN/C2INC/RC8 |
| 21 | **RP19**/OCM2A/RC2 | 53 | OCM1B/RD1 |
| 22 | $\overline{\text{SS3}}$/FSYNC3/RC11 | 54 | OCM3A/RA5 |
| 23 | VDD | 55 | PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1) |
| 24 | VSS | 56 | VCAP |
| 25 | OSC1/CLKI/AN5/**RP3**/OCM1C/RA2 | 57 | VDD |
| 26 | OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1) | 58 | RTCC/RA15 |
| 27 | SDO3/RA8(1) | 59 | OCM3C/RA14 |
| 28 | SOSCI/AN7/**RP10**/RB4 | 60 | D-/RB10 |
| 29 | SOSCO/SCLKI/**RP5**/PWRLCLK/RA4 | 61 | D+/RB11 |
| 30 | **RP24**/RA9 | 62 | VUSB3V3 |
| 31 | SDI1/INT1/RD4 | 63 | AN8/**RP15**/SCL3/RB13(1) |
| 32 | $\overline{\text{SS1}}$/FSYNC1/INT0/RD2 | 64 | **RP22**/SCK3/RA10(1) |

**Note 1:** High drive strength pin.
**2:** Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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**TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Pin Name | Pin Number | | | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|---|---|
| | 28-Pin SSOP | 28-Pin QFN/ UQFN | 36-Pin QFN | 40-Pin UQFN | 48-Pin QFN/ TQFP | 64-Pin QFN/ TQFP | | | |
| INT0 | 26 | 23 | 29 | 32 | 16 | 32 | I | ST | External Interrupt 0 |
| INT1 | 25 | 22 | 28 | 31 | 15 | 31 | I | ST | External Interrupt 1 |
| INT2 | 18 | 15 | 19 | 20 | 1 | 49 | I | ST | External Interrupt 2 |
| INT3 | 2 | 27 | 33 | 36 | 40 | 36 | I | ST | External Interrupt 3 |
| LVDIN | 24 | 21 | 20 | 21 | 4 | 52 | I | ANA | High/Low-Voltage Detect input |
| $\overline{\text{MCLR}}$ | 1 | 26 | 32 | 35 | 19 | 9 | I | ST | Master Clear (device Reset) |
| OCM1A | 17 | 14 | 18 | 18 | 48 | 7 | O | DIG | MCCP1 Output A |
| OCM1B | 18 | 15 | 19 | 20 | 1 | 53 | O | DIG | MCCP1 Output B |
| OCM1C | 9 | 6 | 7 | 7 | 32 | 25 | O | DIG | MCCP1 Output C |
| OCM1D | 10 | 7 | 8 | 8 | 41 | 37 | O | DIG | MCCP1 Output D |
| OCM1E | 2 | 27 | 33 | 36 | 40 | 36 | O | DIG | MCCP1 Output E |
| OCM1F | 3 | 28 | 34 | 37 | 22 | 12 | O | DIG | MCCP1 Output F |
| OCM2A | 19 | 16 | 5 | 5 | 29 | 21 | O | DIG | MCCP2 Output A |
| OCM2B | 26 | 23 | 29 | 32 | 39 | 35 | O | DIG | MCCP2 Output B |
| OCM2C | 4 | 1 | 35 | 38 | 23 | 13 | O | DIG | MCCP2 Output C |
| OCM2D | 5 | 2 | 36 | 39 | 24 | 14 | O | DIG | MCCP2 Output D |
| OCM2E | 6 | 3 | 1 | 1 | 25 | 15 | O | DIG | MCCP2 Output E |
| OCM2F | 7 | 4 | 2 | 2 | 26 | 16 | O | DIG | MCCP2 Output F |
| OCM3A | 24 | 21 | 11 | 11 | 37 | 54 | O | DIG | MCCP3 Output A |
| OCM3B | 25 | 22 | 28 | 31 | 15 | 33 | O | DIG | MCCP3 Output B |
| OCM3C | 11 | 8 | 9 | 9 | 35 | 59 | O | DIG | MCCP3 Output C |
| OCM3D | 12 | 9 | 10 | 10 | 36 | 41 | O | DIG | MCCP3 Output D |
| OCM3E | 14 | 11 | 15 | 15 | 45 | 42 | O | DIG | MCCP3 Output E |
| OCM3F | 16 | 13 | 17 | 17 | 47 | 45 | O | DIG | MCCP3 Output F |
| OSC1 | 9 | 6 | 7 | 7 | 32 | 25 | — | — | Primary Oscillator crystal |
| OSC2 | 10 | 7 | 8 | 8 | 33 | 26 | — | — | Primary Oscillator crystal |
| PGEC1 | 5 | 2 | 36 | 39 | 24 | 14 | I | ST | ICSP™ Port 1 programming clock input |
| PGEC2 | 2 | 27 | 33 | 36 | 21 | 11 | I | ST | ICSP Port 2 programming clock input |
| PGEC3 | 19 | 16 | 21 | 22 | 5 | 55 | I | ST | ICSP Port 3 programming clock input |
| PGED1 | 4 | 1 | 35 | 38 | 23 | 13 | I/O | ST/DIG | ICSP Port 1 programming data |
| PGED2 | 3 | 28 | 34 | 37 | 22 | 12 | I/O | ST/DIG | ICSP Port 2 programming data |
| PGED3 | 14 | 11 | 15 | 15 | 45 | 43 | I/O | ST/DIG | ICSP Port 3 programming data |
| PWRLCLK | 12 | 9 | 10 | 10 | 36 | 29 | I | ST | Real-Time Clock 50/60 Hz clock input |

**Legend:** ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = $I^2C$/SMBus input buffer ANA = Analog level input/output

**TABLE 7-2: INTERRUPTS (CONTINUED)**

| Interrupt Source | MPLAB® XC32 Vector Name | Vector Number | Interrupt Related Bits Location | | | | Persistent Interrupt |
|---|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Subpriority | |
| RESERVED | | 26 | IFS0<26> | IEC0<26> | IPC6<20:18> | IPC6<17:16> | No |
| RESERVED | | 27 | IFS0<27> | IEC0<27> | IPC6<28:26> | IPC6<25:24> | No |
| RESERVED | | 28 | IFS0<28> | IEC0<28> | IPC7<4:2> | IPC7<1:0> | No |
| USB | _USB_VECTOR | 29 | IFS0<29> | IEC0<29> | IPC7<12:10> | IPC7<9:8> | No |
| RESERVED | | 30 | IFS0<30> | IEC0<30> | IPC7<20:18> | IPC7<17:16> | No |
| RESERVED | | 31 | IFS0<31> | IEC0<31> | IPC7<28:26> | IPC7<25:24> | No |
| Real-Time Clock Alarm | _RTCC_VECTOR | 32 | IFS1<0> | IEC1<0> | IPC8<4:2> | IPC8<1:0> | No |
| ADC Conversion | _ADC_VECTOR | 33 | IFS1<1> | IEC1<1> | IPC8<12:10> | IPC8<9:8> | No |
| RESERVED | | 34 | IFS1<2> | IEC1<2> | IPC8<20:18> | IPC8<17:16> | No |
| RESERVED | | 35 | IFS1<3> | IEC1<3> | IPC8<28:26> | IPC8<25:24> | No |
| High/Low-Voltage Detect | _HLVD_VECTOR | 36 | IFS1<4> | IEC1<4> | IPC9<4:2> | IPC9<1:0> | Yes |
| Logic Cell 1 | _CLC1_VECTOR | 37 | IFS1<5> | IEC1<5> | IPC9<12:10> | IPC9<9:8> | No |
| Logic Cell 2 | _CLC2_VECTOR | 38 | IFS1<6> | IEC1<6> | IPC9<20:18> | IPC9<17:16> | No |
| Logic Cell 3 | _CLC3_VECTOR | 39 | IFS1<7> | IEC1<7> | IPC9<28:26> | IPC9<25:24> | No |
| Logic Cell 4 | _CLC4_VECTOR | 40 | IFS1<8> | IEC1<8> | IPC10<4:2> | IPC10<1:0> | No |
| SPI1 Error | _SPI1_ERR_VECTOR | 41 | IFS1<9> | IEC1<9> | IPC10<12:10> | IPC10<9:8> | Yes |
| SPI1 Transmission | _SPI1_TX_VECTOR | 42 | IFS1<10> | IEC1<10> | IPC10<20:18> | IPC10<17:16> | Yes |
| SPI1 Reception | _SPI1_RX_VECTOR | 43 | IFS1<11> | IEC1<11> | IPC10<28:26> | IPC10<25:24> | Yes |
| SPI2 Error | _SPI2_ERR_VECTOR | 44 | IFS1<12> | IEC1<12> | IPC11<4:2> | IPC11<1:0> | Yes |
| SPI2 Transmission | _SPI2_TX_VECTOR | 45 | IFS1<13> | IEC1<13> | IPC11<12:10> | IPC11<9:8> | Yes |
| SPI2 Reception | _SPI2_RX_VECTOR | 46 | IFS1<14> | IEC1<14> | IPC11<20:18> | IPC11<17:16> | Yes |
| SPI3 Error | _SPI3_ERR_VECTOR | 47 | IFS1<15> | IEC1<15> | IPC11<28:26> | IPC11<25:24> | Yes |
| SPI3 Transmission | _SPI3_TX_VECTOR | 48 | IFS1<16> | IEC1<16> | IPC12<4:2> | IPC12<1:0> | Yes |
| SPI3 Reception | _SPI3_RX_VECTOR | 49 | IFS1<17> | IEC1<17> | IPC12<12:10> | IPC12<9:8> | Yes |
| RESERVED | | 50 | IFS1<18> | IEC1<18> | IPC12<20:18> | IPC12<17:16> | No |
| RESERVED | | 51 | IFS1<19> | IEC1<19> | IPC12<28:26> | IPC12<25:24> | No |
| RESERVED | | 52 | IFS1<20> | IEC1<20> | IPC13<4:2> | IPC13<1:0> | No |
| UART1 Reception | _UART1_RX_VECTOR | 53 | IFS1<21> | IEC1<21> | IPC13<12:10> | IPC13<9:8> | Yes |
| UART1 Transmission | _UART1_TX_VECTOR | 54 | IFS1<22> | IEC1<22> | IPC13<20:18> | IPC13<17:16> | Yes |
| UART1 Error | _UART1_ERR_VECTOR | 55 | IFS1<23> | IEC1<23> | IPC13<28:26> | IPC13<25:24> | Yes |

**TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 8B40 | DCH2DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8B50 | DCH2SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8B60 | DCH2DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8B70 | DCH2CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8B80 | DCH2CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8B90 | DCH2DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 8BA0 | DCH3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 8BB0 | DCH3ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 8BC0 | DCH3INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 8BD0 | DCH3SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 8BE0 | DCH3DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 8BF0 | DCH3SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8C00 | DCH3DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8C10 | DCH3SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 8C20 | DCH3DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

**REGISTER 8-1: DMACON: DMA CONTROLLER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | SUSPEND | DMABUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

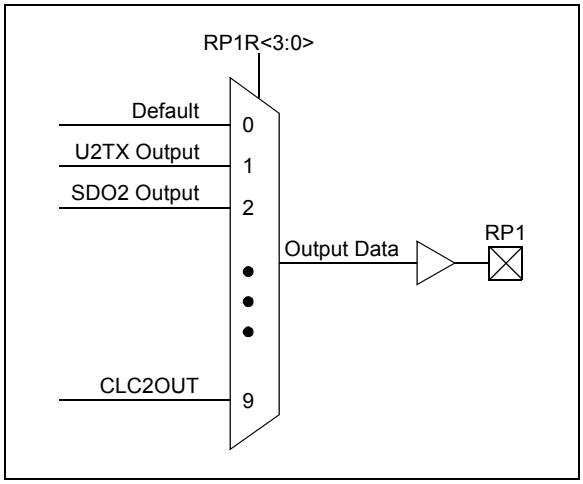
**Note 1:** The user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

### 10.9.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 4-bit fields. The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 10-4 and Figure 10-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 10-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RP0**




### 10.9.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MM0256GPM064 family devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

#### 10.9.6.1 Control Register Lock

Under normal operation, writes to the RPORx and RPINRx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit in the RPCON register. Clearing IOLOCK prevents writes to the control registers; setting IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

**TABLE 10-9: PERIPHERAL PIN SELECT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2B40 | RPOR3 | 31:16 | — | — | — | RP16R<4:0> | | | | | — | — | — | RP15R<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | RP14R<4:0> | | | | | — | — | — | RP13R<4:0> | | | | | 0000 |
| 2B50 | RPOR4 | 31:16 | — | — | — | RP20R<4:0> | | | | | — | — | — | RP19R<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | RP18R<4:0> | | | | | — | — | — | RP17R<4:0> | | | | | 0000 |
| 2B60 | RPOR5 | 31:16 | — | — | — | RP24R<4:0> | | | | | — | — | — | RP23R<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | RP22R<4:0> | | | | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

## 14.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

**Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. "Capture/Compare/PWM/ Timer (MCCP and SCCP)"** (DS60001381) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

### 14.1 Introduction

PIC32MM0256GPM064 family devices include nine Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
  - Backward compatible with previous input capture peripherals of the PIC32 family
  - 16-bit or 32-bit capture of time base on external event
  - Up to four-level deep FIFO capture buffer
  - Capture source input multiplexer
  - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
  - Backward compatible with previous output compare peripherals of the PIC32 family
  - Single Edge and Dual Edge Compare modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
  - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 14-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

**REGISTER 14-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)**

bit 20-16 **SYNC<4:0>:** CCPx Synchronization Source Select bits
11111 = Off
11110 = Reserved
...
11100 = Reserved
11011 = Time base is synchronized to the start of ADC conversion
11010 = Time base is synchronized to Comparator 3
11001 = Time base is synchronized to Comparator 2
11000 = Time base is synchronized to Comparator 1
10111 = Reserved
...
10010 = Reserved
10011 = Time base is synchronized to CLC4
10010 = Time base is synchronized to CLC3
10001 = Time base is synchronized to CLC2
10001 = Time base is synchronized to CLC1
01111 = Time base is synchronized to SCCP9
01110 = Time base is synchronized to SCCP8
01101 = Time base is synchronized to the INT4 Pin (Remappable)
01100 = Time base is synchronized to the INT3 Pin
01011 = Time base is synchronized to the INT2 Pin
01010 = Time base is synchronized to the INT1 Pin
01001 = Time base is synchronized to the INT0 Pin
01000 = Reserved
...
00101 = Reserved
00100 = Time base is synchronized to SCCP3
00011 = Time base is synchronized to SCCP2
00010 = Time base is synchronized to MCCP1
00001 = Time base is synchronized to this MCCP/SCCP
00000 = No external synchronization; timer rolls over at FFFFh or matches with the Timer Period register

bit 15 **ON:** CCPx Module Enable bit(1)
1 = Module is enabled with the operating mode specified by the MOD<3:0> bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CCPx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **CCPSLP:** CCPx Sleep Mode Enable bit
1 = Module continues to operate in Sleep modes
0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply
0 = Module time base clock is not synchronized to internal system clocks

**Note 1:** This control bit has no function in Input Capture modes.
**2:** This control bit has no function when TRIGEN = 0.
**3:** Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

**REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | MCLKSEL(1) | — | — | — | — | — | SPIFE | ENHBUF(1) |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | DISSDO(4) | MODE32 | MODE16 | SMP | CKE(2) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SSEN | CKP(3) | MSTEN | DISSDI(4) | STXISEL<1:0> | | SRXISEL<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FRMEN:** Framed SPI Support bit
- 1 = Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC1 input/output)
- 0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit (Framed SPI mode only)
- 1 = Frame sync pulse input (Slave mode)
- 0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
- 1 = Frame pulse is active-high
- 0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
- 1 = Slave select SPI support is enabled; the $\overline{SSx}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
- 0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
- 1 = Frame sync pulse is one character wide
- 0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
- 111 = Reserved
- 110 = Reserved
- 101 = Generates a frame sync pulse on every 32 data characters
- 100 = Generates a frame sync pulse on every 16 data characters
- 011 = Generates a frame sync pulse on every 8 data characters
- 010 = Generates a frame sync pulse on every 4 data characters
- 001 = Generates a frame sync pulse on every 2 data characters
- 000 = Generates a frame sync pulse on every data character

**Note 1:** These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.

**2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**3:** When AUDEN = 1, the SPI/$I^2S$ module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

**4:** These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

**REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)**

bit 5 **D/A:** Data/Address bit (when operating as $I^2C$ slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 2 **R/W:** Read/Write Information bit (when operating as $I^2C$ slave)
1 = Read – Indicates data transfer is output from slave
0 = Write – Indicates data transfer is input to slave
Hardware is set or clear after reception of an $I^2C$ device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with the received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of the data transmission.

**REGISTER 18-5: U1PWRC: USB POWER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY(1) | — | USUSPEND | USBPWR(1) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected, but an interrupt is pending; it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit(1)
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

**Note 1:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

**REGISTER 18-15: U1TOK: USB TOKEN REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PID<3:0>(1) | | | | EP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)

1101 = SETUP (TX) token type transaction
1001 = IN (RX) token type transaction
0001 = OUT (TX) token type transaction

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits

The 4-bit value must specify a valid endpoint.

**Note 1:** All other values not listed are reserved and must not be used.

**REGISTER 18-16: U1SOF: USB SOF THRESHOLD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical Values of the Threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

**REGISTER 18-20: U1CNFG1: USB CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | UTEYE | UOEMON | — | USBSIDL | LSDEV | — | — | UASUSPND |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
- 1 = Eye pattern test is enabled
- 0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
- 1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
- 0 = $\overline{OE}$ signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** USB Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 3 **LSDEV:** USB Low-Speed Device Enable bit
- 1 = USB macro operates in Low-Speed Device Only mode
- 0 = USB macro operates in OTG, Host or Fast Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
- 1 = USB module automatically suspends upon entry to Sleep mode; see the USUSPEND bit (U1PWRC<1>) in Register 18-5
- 0 = USB module does not automatically suspend upon entry to Sleep mode; software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

**REGISTER 20-3: AD1CON3: ADC CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADRC | EXTSAM | — | SAMC<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCS<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from the Fast RC (FRC) oscillator
0 = Clock derived from the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

## 25.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in the PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

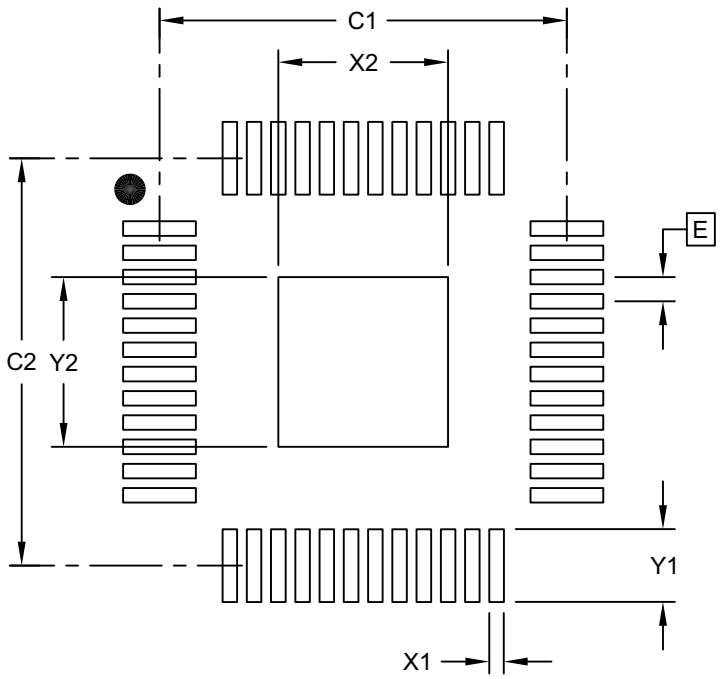
Table 25-1 lists the module disable bits locations for all modules.

**TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS**

| Peripheral | PMDx Bit Name | Register Name and Bit Location |
|---|---|---|
| Analog-to-Digital Converter (ADC) | ADCMD | PMD1<0> |
| Voltage Reference (VR) | VREFMD | PMD1<12> |
| High/Low-Voltage Detect (HLVD) | HLVDMD | PMD1<20> |
| Comparator 1 (CMP1) | CMP1MD | PMD2<0> |
| Comparator 2 (CMP2) | CMP2MD | PMD2<1> |
| Comparator 3 (CMP3) | CMP3MD | PMD2<2> |
| Configurable Logic Cell 1 (CLC1) | CLC1MD | PMD2<24> |
| Configurable Logic Cell 2 (CLC2) | CLC2MD | PMD2<25> |
| Configurable Logic Cell 3 (CLC3) | CLC3MD | PMD2<26> |
| Configurable Logic Cell 4 (CLC4) | CLC4MD | PMD2<27> |
| Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1) | CCP1MD | PMD3<8> |
| Multiple Outputs Capture/Compare/PWM/ Timer2 (MCCP2) | CCP2MD | PMD3<9> |
| Multiple Outputs Capture/Compare/PWM/ Timer3 (MCCP3) | CCP3MD | PMD3<10> |
| Single Output Capture/Compare/PWM/ Timer4 (SCCP4) | CCP4MD | PMD3<11> |
| Single Output Capture/Compare/PWM/ Timer5 (SCCP5) | CCP5MD | PMD3<12> |
| Single Output Capture/Compare/PWM/ Timer6 (SCCP6) | CCP6MD | PMD3<13> |
| Single Output Capture/Compare/PWM/ Timer7 (SCCP7) | CCP7MD | PMD3<14> |
| Single Output Capture/Compare/PWM/ Timer8 (SCCP8) | CCP8MD | PMD3<15> |
| Single Output Capture/Compare/PWM/ Timer9 (SCCP9) | CCP9MD | PMD3<16> |
| Timer1 (TMR1) | T1MD | PMD4<0> |
| Timer2 (TMR2) | T2MD | PMD4<1> |
| Timer3 (TMR3) | T3MD | PMD4<2> |
| Universal Asynchronous Receiver Transmitter 1 (UART1) | U1MD | PMD5<0> |

### 48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Thermal Tab

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Tab Width | X2 | | 3.50 | |
| Optional Center Tab Length | Y2 | | 3.50 | |
| Contact Pad Spacing | C1 | | 8.40 | |
| Contact Pad Spacing | C2 | | 8.40 | |
| Contact Pad Width (X48) | X1 | | | 0.30 |
| Contact Pad Length (X48) | Y1 | | | 1.50 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2183A

# APPENDIX A: REVISION HISTORY

## Revision A (January 2016)

This is the initial version of the document.

## Revision B (March 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Low-Power Modes"**, **"Peripheral Features"**, **"Microcontroller Features"** and **"Analog Features"** sections.
  - Changed program row size to 128 32-bit words in **Section 5.0 "Flash Program Memory"**.
  - Updated **Section 4.2 "Bus Matrix (BMX)"**, **Section 8.0 "Direct Memory Access (DMA) Controller"**, **Section 9.0 "Oscillator Configuration"**, **Section 9.2 "Clock Switching Operation"**, **Section 9.3 "FRC Active Clock Tuning"**, **Section 10.1 "CLR, SET and INV Registers"**, **Section 10.5 "I/O Port Write/Read Timing"**, **Section 10.6 "GPIO Port Merging"**, **Section 20.1 "Introduction"**, **Section 26.5 "Band Gap Voltage Reference"** and **Section 26.7 "Unique Device Identifier (UDID)"**.
  - Added the 36-Lead VQFN (M2) and 48-Lead UQFN (M4) packaging diagrams to **Section 30.0 "Packaging Information"**.
- Tables:
  - Updated Table 1-1, Table 7-2, Table 7-3, Table 9-1, Table 10-5, Table 10-6, Table 10-7, Table 10-8, Table 20-1, Table 26-3, Table 26-4, Table 26-6, Table 26-8, Table 29-2, Table 29-3, Table 29-4, Table 29-5, Table 29-6, Table 29-7, Table 29-8, Table 29-11, Table 29-14, Table 29-20 and Table 29-21.
  - Replaced Table 29-34 with Table 29-34, Table 29-35 and Table 29-36.
  - Removed previously numbered Table 29-35.
- Examples:
  - Updated Example 9-1.
- Figures:
  - Updated Figure 1-1, Figure 8-1, Figure 9-1, Figure 9-2 and Figure 22-1.
  - Added Figure 9-2.
- Registers:
  - Updated Register 6-4, Register 9-1, Register 9-2, Register 9-3, Register 9-5, Register 14-1, Register 19-1, Register 19-2, Register 26-1,Register 26-5 and Register 26-10.
  - Removed Register 9-7.

## Revision C (May 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Peripheral Features"** section.
  - Updated **Section 2.3 "Master Clear (MCLR) Pin"** and **Section 25.3 "Retention Sleep Mode"**.
- Tables:
  - Updated Table 29-4, Table 29-5, Table 29-6 and Table 29-7.
- Registers:
  - Updated Register 13-1.

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