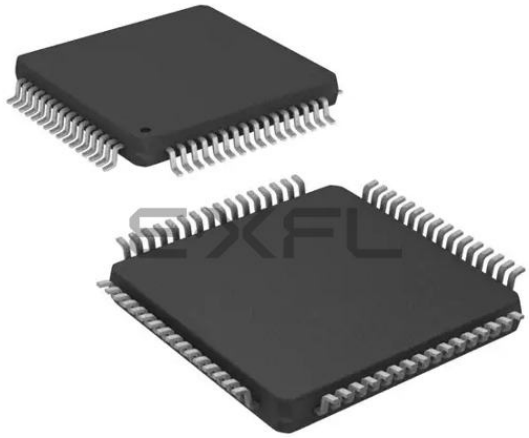
Microchip Technology - PIC32MM0064GPM064-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 20x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm064-i-pt

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-3	Reserved	Reserved in the microAptiv™ UC.
4	UserLocal	User information that can be written by privileged software and read via RDHWR Register 29.
5-6	Reserved	Reserved in the microAptiv UC.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-Privileged mode.
8	BadVAddr(1)	Reports the address for the most recent address related exception.
9	Count(1)	Processor cycle count.
10	Reserved	Reserved in the microAptiv UC.
11	Compare(1)	Timer interrupt control.
12	Status/ IntCtl/ SRSCtl/ SRSMap1/ View_IPL/ SRSMAP2	Processor status and control; interrupt control and shadow set control.
13	Cause(1)/ View_RIPL	Cause of last exception.
14	EPC(1)	Program Counter at last exception.
15	PRId/ EBase/ CDMMBase	Processor identification and revision; exception base address; Common Device Memory Map Base register.
16	CONFIG/ CONFIG1/ CONFIG2/ CONFIG3/ CONFIG7	Configuration registers.
7-22	Reserved	Reserved in the microAptiv UC.
23	Debug/ Debug2/ TraceControl/ TraceControl2/ UserTraceData1/ TraceBPC(2)	EJTAG Debug register. EJTAG Debug Register 2. EJTAG Trace Control register. EJTAG Trace Control Register 2. EJTAG User Trace Data 1 register. EJTAG Trace Breakpoint register.
24	DEPC(2)/ UserTraceData2	Program Counter at last debug exception. EJTAG User Trace Data 2 register.
25	PerfCtl0/ PerfCnt0/ PerfCtl1/ PerfCnt1	Performance Counter 0 control. Performance Counter 0. Performance Counter 1 control. Performance Counter 1.
26	ErrCtl	Software parity check enable.
27	CacheErr	Records information about SRAM parity errors.
28-29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC(1)	Program Counter at last error.
31	DeSAVE(2)	Debug Handler Scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used in debug.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
26E0	RCON	31:16	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	C000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0003
26F0	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
2700	RNMICON	31:16	—	—	—	—	—	—	—	WDTR	SWNMI	—	—	—	GNMI	—	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
2710	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	SBOREN	RETEN	VREGS	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{\text{MCLR}}$.	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-Maskable Interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	_general_exception_handler
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	_general_exception_handler
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	_general_exception_handler

REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	SRIPL<2:0>(1)		
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SIRQ<7:0>							

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level for Single Vector Mode bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits

11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

REGISTER 8-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** DMA Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

REGISTER 8-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

REGISTER 8-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	CHBUSY	—	—	—	—	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
- 1 = Channel is active or has been enabled
- 0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
- 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
- 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events if Disabled bit
- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit
- 1 = Allows channel to be chained
- 0 = Does not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit
- 1 = Channel is continuously enabled and not automatically disabled after a block transfer is complete
- 0 = Channel is disabled on a block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
- 1 = An event has been detected
- 0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
- 11 = Channel has Priority 3 (highest)
- 10 = Channel has Priority 2
- 01 = Channel has Priority 1
- 00 = Channel has Priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 8-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All Other modes:
Unused.

TABLE 10-4: OUTPUT PIN SELECTION

Output Function Number	Function	Output Name
0	None	Not Connected
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	C3OUT	Comparator 3 Output
4	U2TX	UART2 Transmit
5	$\overline{\text{U2RTS}}$	UART2 Request-to-Send
6	U3TX	UART3 Transmit
7	$\overline{\text{U3RTS}}$	UART3 Request-to-Send
8	SDO2	SPI2 Data Output
9	SCK2OUT	SPI2 Clock Output
10	SS2OUT	SPI2 Slave Select Output
11	OCM4	SCCP4 Output Compare Output
12	OCM5	SCCP5 Output Compare Output
13	OCM6	SCCP6 Output Compare Output
14	OCM7	SCCP7 Output Compare Output
15	OCM8	SCCP8 Output Compare Output
16	OCM9	SCCP9 Output Compare Output
17	CLC1OUT	CLC1 Output
18	CLC2OUT	CLC2 Output
19	CLC3OUT	CLC3 Output
20	CLC4OUT	CLC4 Output

TABLE 10-9: PERIPHERAL PIN SELECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2A00	RPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
2A20	RPINR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0												INT4R<4:0>					0000
2A30	RPINR2	31:16	—	—	—	ICM2R<4:0>					—	—	—	ICM1R<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2A40	RPINR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM3R<4:0>					0000
2A60	RPINR5	31:16	—	—	—	OCFBR<4:0>					—	—	—	OCFAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2A70	RPINR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TCKIBR<4:0>					—	—	—	TCKIAR<4:0>					0000
2A80	RPINR7	31:16	—	—	—	ICM8R<4:0>					—	—	—	ICM7R<4:0>					0000
		15:0	—	—	—	ICM6R<4:0>					—	—	—	ICM5R<4:0>					0000
2A90	RPINR8	31:16	—	—	—	U3RXR<4:0>					—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM9R<4:0>					0000
2AA0	RPINR9	31:16	—	—	—	U2CTSR<4:0>					—	—	—	U2RXR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2AB0	RPINR10	31:16	—	—	—	U3RTSR<4:0>					—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2AC0	RPINR11	31:16	—	—	—	—	—	—	—	—	—	—	—	SS2INR<4:0>					0000
		15:0	—	—	—	SCK2INR<4:0>					—	—	—	SDI2R<4:0>					0000
2AD0	RPINR12	31:16	—	—	—	CLCINBR<4:0>					—	—	—	CLCINAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2B10	RPOR0	31:16	—	—	—	RP4R<4:0>					—	—	—	RP3R<4:0>					0000
		15:0	—	—	—	RP2R<4:0>					—	—	—	RP1R<4:0>					0000
2B20	RPOR1	31:16	—	—	—	RP8R<4:0>					—	—	—	RP7R<4:0>					0000
		15:0	—	—	—	RP6R<4:0>					—	—	—	RP5R<4:0>					0000
2B30	RPOR2	31:16	—	—	—	RP12R<4:0>					—	—	—	RP11R<4:0>					0000
		15:0	—	—	—	RP10R<4:0>					—	—	—	RP9R<4:0>					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "UART"** (DS61107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

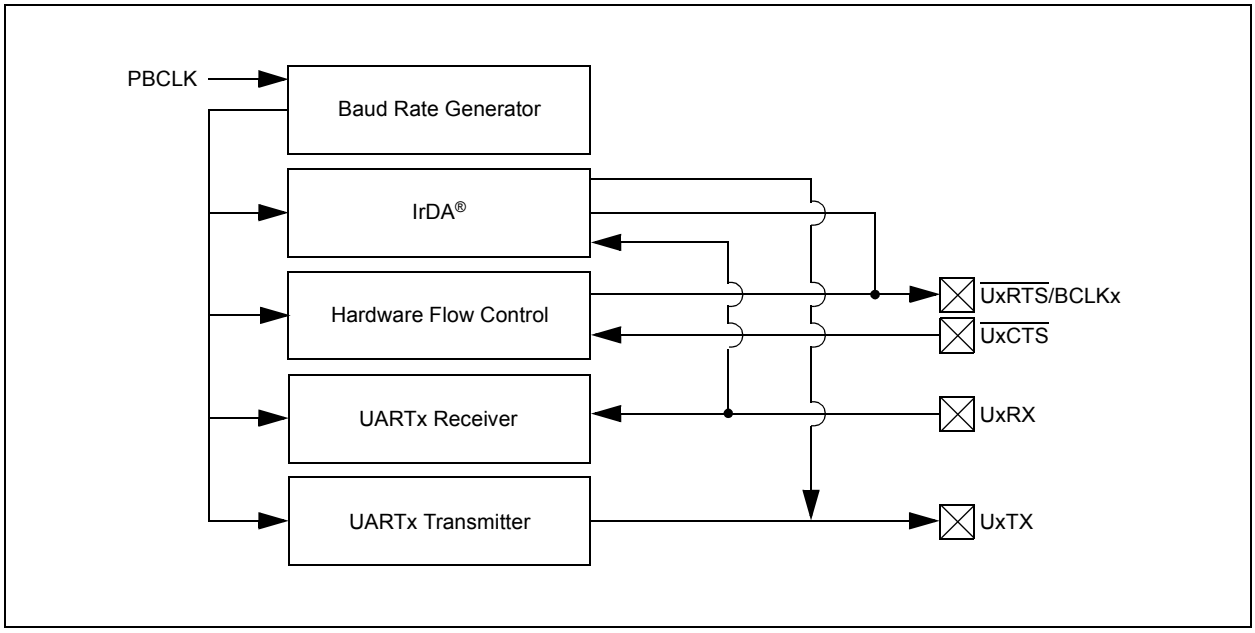
The UART module is one of the serial I/O modules available in the PIC32MM0256GPM064 family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN/J2602 and IrDA®. The module also supports the hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Auto-Baud Feature
- Hardware Flow Control Option
- Fully Integrated Baud Rate Generator (BRG) with 16-Bit Prescaler
- Baud rates ranging from 47.4 bps to 6.25 Mbps at 25 MHz
- 8-Level Deep First-In-First-Out (FIFO) Transmit Data Buffer
- 8-Level Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for Interrupt Only on Address Detect (9th bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- LIN/J2602 Protocol Support
- IrDA Encoder and Decoder with 16x Baud Clock Output for External IrDA Encoder/Decoder Support
- Supports Separate UART Baud Clock Input
- Ability to Continue to Run when a Receive Overflow Condition Exists
- Ability to Run and rEceive Data during Sleep mode

Figure 17-1 illustrates a simplified block diagram of the UART module.

FIGURE 17-1: UARTx SIMPLIFIED BLOCK DIAGRAM



18.0 USB ON-THE-GO (OTG)

Note 1: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS61126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation, with a minimum of external components. This module in Host mode is intended for use as an embedded host, and therefore, does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA Controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 18-1.

18.1 Reclaiming USB Pins When the USB Module is Operating

Select USB pins that are not used on all USB operating modes (USBID and VBUSON) can be reclaimed when the module is operating in a mode that does not require them. These pins can be reclaimed by clearing the appropriate device Configuration bit (refer to Register 26-1).

For example:

- USBID and VBUSON can be reclaimed in Device mode
- VBUSON can be reclaimed in Host mode if it is not used for the power VBUS control

18.2 Reclaiming USB Pins When the USB Module is Disabled

All USB signaling pins, D+, D-, VBUS, VBUSON and USBID, can be reclaimed and used for GPIO or other peripherals if available on the pin when the USB module is disabled. For proper operation of the RB10 and RB11 pins, the USB module must be disabled, but powered. Refer to **Section 18.1 "Reclaiming USB Pins When the USB Module is Operating"** for more information.

18.3 Introduction

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The dedicated USB DMA Controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Support for Host and Device
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking performed by Hardware
- Endpoint Buffering anywhere in System RAM
- Integrated DMA to access System RAM and Flash

Note: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

Note: Adding any circuitry to the USB D+/D- pins, other than the connection to a USB connector, may degrade the USB signal quality and violate USB specifications.

TABLE 18-1: USB OTG REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8670	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000
8680	U1FRML(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
8690	U1FRMH(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<2:0>			0000
86A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
86B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
86C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<7:0>								0000
86D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<7:0>								0000
86E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND	0001
8700	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8710	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8720	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8730	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8740	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8750	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8760	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

REGISTER 18-6: U1IR: USB INTERRUPT REGISTER (CONTINUED)

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
1 = Valid USB Reset has occurred
0 = No USB Reset has occurred

DETACHIF: USB Detach Interrupt bit (Host mode)(6)
1 = Peripheral detachment was detected by the USB module
0 = Peripheral detachment was not detected

Note 1: This bit is only valid if the HOSTEN bit is set (see Register 18-11), there is no activity on the USB for 2.5 µs and the current bus state is not SE0.
2: When not in Suspend mode, this interrupt should be disabled.
3: Clearing this bit will cause the STAT FIFO to advance.
4: Only error conditions enabled through the U1EIE register will set this bit.
5: Device mode.
6: Host mode.

REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half-second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

25.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in the PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

Table 25-1 lists the module disable bits locations for all modules.

TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
Analog-to-Digital Converter (ADC)	ADCMD	PMD1<0>
Voltage Reference (VR)	VREFMD	PMD1<12>
High/Low-Voltage Detect (HLVD)	HLVDMD	PMD1<20>
Comparator 1 (CMP1)	CMP1MD	PMD2<0>
Comparator 2 (CMP2)	CMP2MD	PMD2<1>
Comparator 3 (CMP3)	CMP3MD	PMD2<2>
Configurable Logic Cell 1 (CLC1)	CLC1MD	PMD2<24>
Configurable Logic Cell 2 (CLC2)	CLC2MD	PMD2<25>
Configurable Logic Cell 3 (CLC3)	CLC3MD	PMD2<26>
Configurable Logic Cell 4 (CLC4)	CLC4MD	PMD2<27>
Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1)	CCP1MD	PMD3<8>
Multiple Outputs Capture/Compare/PWM/ Timer2 (MCCP2)	CCP2MD	PMD3<9>
Multiple Outputs Capture/Compare/PWM/ Timer3 (MCCP3)	CCP3MD	PMD3<10>
Single Output Capture/Compare/PWM/ Timer4 (SCCP4)	CCP4MD	PMD3<11>
Single Output Capture/Compare/PWM/ Timer5 (SCCP5)	CCP5MD	PMD3<12>
Single Output Capture/Compare/PWM/ Timer6 (SCCP6)	CCP6MD	PMD3<13>
Single Output Capture/Compare/PWM/ Timer7 (SCCP7)	CCP7MD	PMD3<14>
Single Output Capture/Compare/PWM/ Timer8 (SCCP8)	CCP8MD	PMD3<15>
Single Output Capture/Compare/PWM/ Timer9 (SCCP9)	CCP9MD	PMD3<16>
Timer1 (TMR1)	T1MD	PMD4<0>
Timer2 (TMR2)	T2MD	PMD4<1>
Timer3 (TMR3)	T3MD	PMD4<2>
Universal Asynchronous Receiver Transmitter 1 (UART1)	U1MD	PMD5<0>

REGISTER 26-3: FPOR/AFPOR: POWER-UP SETTINGS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	LPBOREN	RETVR	BOREN<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Reserved:** Program as '1'

bit 3 **LPBOREN:** Low-Power BOR Enable bit
1 = Low-Power BOR is enabled when main BOR is disabled
0 = Low-Power BOR is disabled

bit 2 **RETVR:** Retention Voltage Regulator Enable bit
1 = Retention regulator is disabled
0 = Retention regulator is enabled and controlled by the RETEN bit during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits
11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Windowed mode is disabled
0 = Windowed mode is enabled

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(3)**					
DI10		I/O Pins with ST Buffer	VSS	—	0.2 VDD	V	
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	
DI16		OSC1 (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSC1 (HS mode)	VSS	—	0.2 VDD	V	
	VIH	**Input High Voltage(3)**					
DI20		I/O Pins with ST Buffer: Without 5V Tolerance With 5V Tolerance	 0.8 VDD 0.8 VDD	 — —	 VDD 5.5	 V V	
DI25		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI30	ICNPU	**CNPUx Pull-up Current**	150	350	450	μA	VDD = 3.3V, VPIN = VSS
DI30A	ICNPD	**CNPDx Pull-Down Current**	230	300	500	μA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current(2)**					
DI50		I/O Pins – 5V Tolerant	—	—	1	μA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI51		I/O Pins – Not 5V Tolerant	—	—	1	μA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{MCLR}$	—	—	1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1/CLKI	—	—	1	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes

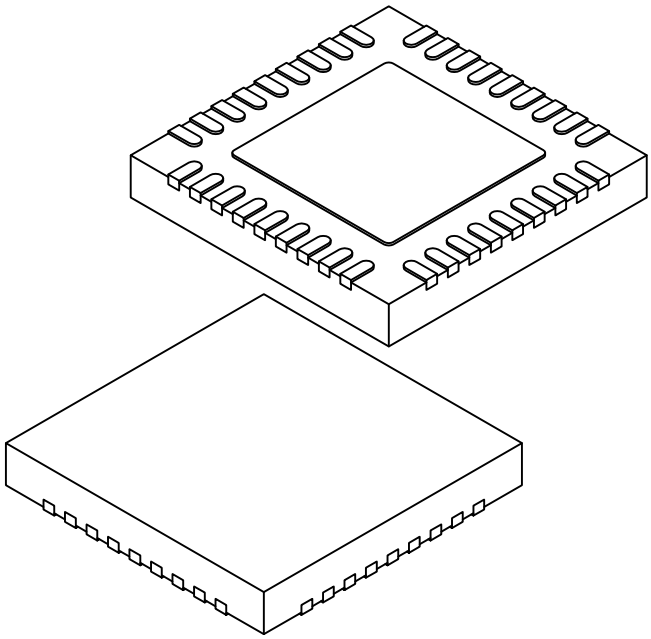
Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Negative current is defined as current sourced by the pin.

3: Refer to Table 1-1 for I/O pin buffer types.

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.45	0.55	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2