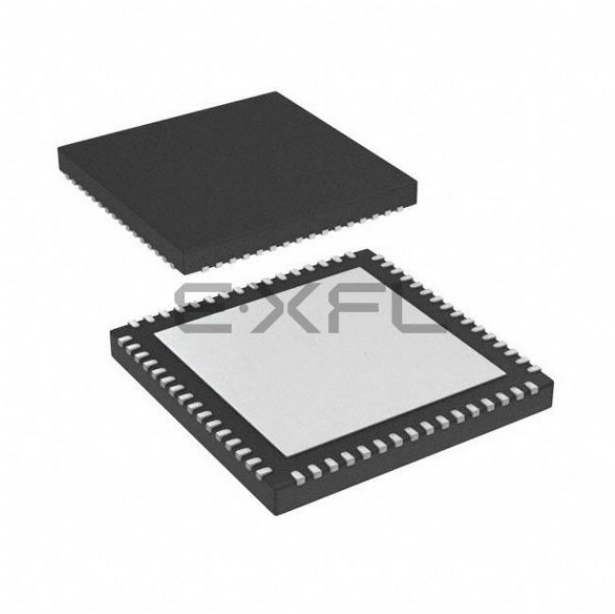
Microchip Technology - PIC32MM0064GPM064T-I/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 20x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0064gpm064t-i-mr

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RP21	—	—	—	—	14	1	I/O	ST/DIG	Remappable peripherals (input or output)
RP22	—	—	—	—	13	64	I/O	ST/DIG	
RP23	—	—	—	—	2	50	I/O	ST/DIG	
RP24	—	—	11	11	37	30	I/O	ST/DIG	
RTCC	25	22	28	31	8	58	O	DIG	Real-Time Clock/Calendar alarm/seconds output
SCK1	17	14	18	18	48	47	I/O	ST/DIG	SPI1 clock (input or output)
SCK3	24	21	27	30	13	64	I/O	ST/DIG	SPI3 clock (input or output)
SCL1	17	14	18	18	48	48	I/O	I2C	I2C1 synchronous serial clock input/output
ASCL1	19	16	21	22	5	55	I/O	I2C	Alternate I2C1 synchronous serial clock input/ output
SCL2	7	4	2	2	26	16	I/O	I2C	I2C2 synchronous serial clock input/output
SCL3	24	21	27	30	12	63	I/O	I2C	I2C3 synchronous serial clock input/output
SCLKI	12	9	10	10	36	29	I	ST	Secondary Oscillator digital clock input
SDA1	18	15	19	20	1	49	I/O	I2C	I2C1 data input/output
ASDA1	14	11	15	15	45	43	I/O	I2C	Alternate I2C1 data input/output
SDA2	6	3	1	1	25	15	I/O	I2C	I2C2 data input/output
SDA3	16	13	17	17	47	46	I/O	I2C	I2C3 data input/output
SDI1	25	22	28	31	15	31	I	ST	SPI1 data input
SDI3	16	13	17	17	14	1	I	ST	SPI3 data input
SDO1	18	15	19	20	38	34	O	DIG	SPI1 data output
SDO3	19	16	21	22	34	27	O	DIG	SPI3 data output
SOSCI	11	8	9	9	35	28	—	—	Secondary Oscillator crystal
SOSCO	12	9	10	10	36	29	—	—	Secondary Oscillator crystal
$\overline{SS1}$	26	23	29	32	16	32	I	ST	SPI1 slave select input
$\overline{SS3}$	14	11	15	15	45	22	I	ST	SPI3 slave select input
T1CK	18	15	19	20	38	34	I	ST	Timer1 external clock input
T2CK	18	15	3	3	27	19	I	ST	Timer2 external clock input
T3CK	19	16	4	4	28	20	I	ST	Timer3 external clock input
T1G	18	15	19	20	38	34	I	ST	Timer1 clock gate input
T2G	18	15	3	3	27	19	I	ST	Timer2 clock gate input
T3G	19	16	4	4	28	20	I	ST	Timer3 clock gate input
TCK	17	14	18	18	48	48	I	ST	JTAG clock input
TDI	7	4	2	2	26	16	I	ST	JTAG data input
TDO	19	16	21	22	5	55	O	DIG	JTAG data output
TMS	18	15	19	20	1	49	I	ST	JTAG mode select input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
U1BCLK	18	15	19	20	38	34	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{\text{U1CTS}}$	17	14	18	18	48	6	I	ST	UART1 Clear-to-Send
$\overline{\text{U1RTS}}$	18	15	19	20	38	34	O	DIG	UART1 Ready-to-Send
U1RX	26	23	29	32	20	10	I	ST	UART1 receive data input
U1TX	25	22	28	31	44	40	O	DIG	UART1 transmit data output
USBID	14	11	15	15	45	43	I	ST	USB OTG ID (OTG mode only)
USBOEN	19	16	21	22	5	55	O	—	USB transceiver output enable flag
VBUSON	25	22	28	31	15	2	O	—	USB host and On-The-Go (OTG) bus power control output
VBUS	15	12	16	16	46	44	P	—	USB VBUS connection (5V nominal)
VUSB3V3	23	20	26	29	11	62	P	—	USB transceiver power input (3.3V nominal)
VCAP	20	17	22	24	7	56	P	—	Core voltage regulator filter capacitor connection
VDD	13,28	10,25	13,23,31	13,26, 34	18,30, 43	17,23, 39,57	P	—	Digital modules power supply
VREF-	3	28	34	37	22	12	I	ANA	Analog-to-Digital Converter negative reference
VREF+	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter positive reference
VSS	8,27	5,24	6,12,30	6,12,33	6,17,31, 42	18,24, 38	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART2 Reception	_UART2_RX_VECTOR	56	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	57	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	58	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
UART3 Reception	_UART3_RX_VECTOR	59	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
UART3 Transmission	_UART3_TX_VECTOR	60	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
UART3 Error	_UART3_ERR_VECTOR	61	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
RESERVED		62	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	No
RESERVED		63	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	No
RESERVED		64	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	No
I2C1 Slave	_I2C1_SLAVE_VECTOR	65	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
I2C1 Master	_I2C1_MASTER_VECTOR	66	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
I2C1 Bus Collision	_I2C1_BUS_VECTOR	67	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
I2C2 Slave	_I2C2_SLAVE_VECTOR	68	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
I2C2 Master	_I2C2_MASTER_VECTOR	69	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
I2C2 Bus Collision	_I2C2_BUS_VECTOR	70	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
I2C3 Slave	_I2C3_SLAVE_VECTOR	71	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
I2C3 Master	_I2C3_MASTER_VECTOR	72	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
I2C3 Bus Collision	_I2C3_BUS_VECTOR	73	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	74	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	No
CCP1 Timer	_CCT1_VECTOR	75	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	76	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	No
CCP2 Timer	_CCT2_VECTOR	77	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	78	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	No
CCP3 Timer	_CCT3_VECTOR	79	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	No
CCP4 Input Capture or Output Compare	_CCP4_VECTOR	80	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	No
CCP4 Timer	_CCT4_VECTOR	81	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	No
CCP5 Input Capture or Output Compare	_CCP5_VECTOR	82	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	No
CCP5 Timer	_CCT5_VECTOR	83	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	No
CCP6 Input Capture or Output Compare	_CCP6_VECTOR	84	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	No
CCP6 Timer	_CCT6_VECTOR	85	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	No
CCP7 Input Capture or Output Compare	_CCP7_VECTOR	86	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	No
CCP7 Timer	_CCT7_VECTOR	87	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	No

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	VS<6:0>						
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-16 **VS<6:0>**: Vector Spacing bits

Spacing Between Vectors:
0000000 = 0 Bytes
0000001 = 8 Bytes
0000010 = 16 Bytes
0000100 = 32 Bytes
0001000 = 64 Bytes
0010000 = 128 Bytes
0100000 = 256 Bytes
1000000 = 512 Bytes
All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multivector Configuration bit

1 = Interrupt controller is configured for Multivectored mode
0 = Interrupt controller is configured for Single Vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
001 = Interrupts of Group Priority 1 start the interrupt proximity timer
000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

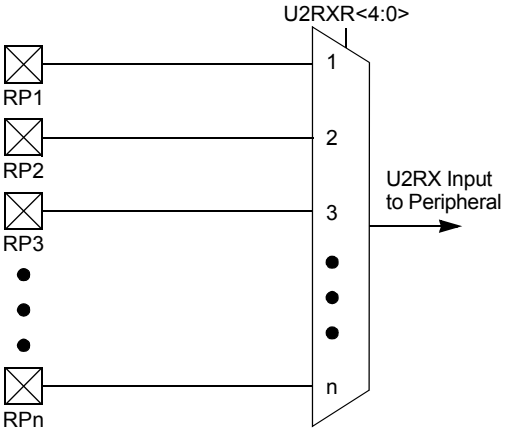
Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

10.9.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (refer to the peripheral pins listed in Table 10-2) are used to configure peripheral input mapping (see Register 10-1). Each register contains sets of 5-bit fields. Programming these bits with a number of the remappable pin will connect the peripheral to this RPn pin (refer to Table 10-3). For any given device, the valid range of values for any bit field is shown in Table 10-2.

For example, Figure 10-2 illustrates the remappable pin selection for the U2RX input.

FIGURE 10-2: REMAPPABLE INPUT EXAMPLE FOR U2RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 10-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
MCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
MCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
SCCP4 Input Capture	ICM4	RPINR3	ICM4R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
SCCP5 Input Capture	ICM5	RPINR7	ICM5R<4:0>
SCCP6 Input Capture	ICM6	RPINR7	ICM6R<4:0>
SCCP7 Input Capture	ICM7	RPINR7	ICM7R<4:0>
SCCP8 Input Capture	ICM8	RPINR7	ICM8R<4:0>
SCCP9 Input Capture	ICM9	RPINR8	ICM9R<4:0>
UART3 Receive	U3RX	RPINR8	U3RXR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR9	U2CTSR<4:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR10	U3CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

11.1 Timer1 Control Register

TABLE 11-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
8010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
8020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>(2)																FFFF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

2: PR1 values of '0' and '1' are reserved.

REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer1 On bit
1 = Timer1 is enabled
0 = Timer1 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)

bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
1 = Asynchronous write to TMR1 register is in progress
0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK Pin
00 = External clock comes from the Secondary Oscillator (SOSC)

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

12.0 TIMER2 AND TIMER3

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-Bit Timer
- Synchronous Internal 16-Bit Gated Timer
- Synchronous External 16-Bit Timer

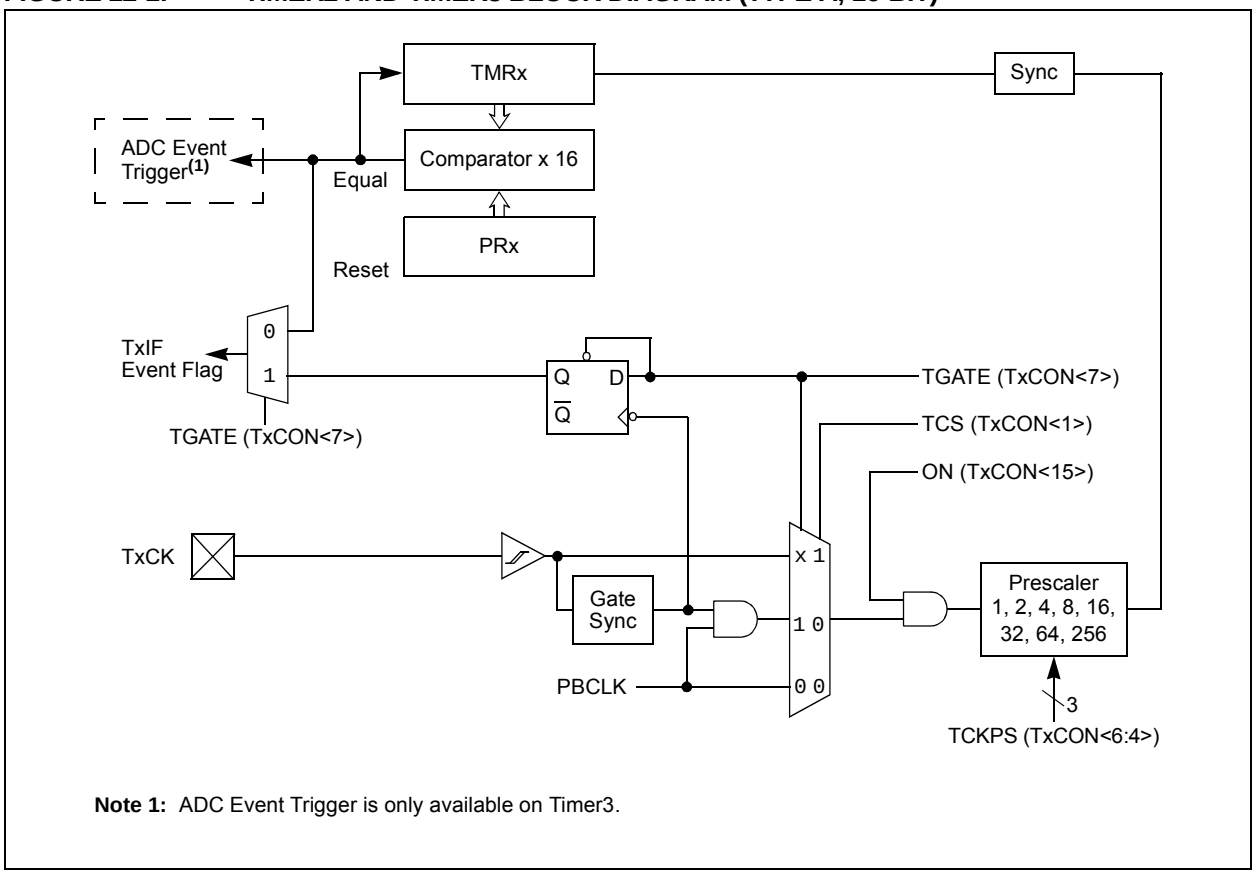
A single 32-bit synchronous timer is available by combining Timer2 with Timer3. The resulting 32-bit timer can operate in three modes:

- Synchronous Internal 32-Bit Timer
- Synchronous Internal 32-Bit Gated Timer
- Synchronous External 32-Bit

12.1 Additional Supported Features

- Selectable Clock Prescaler
- Timers Operational during CPU Idle
- ADC Event Trigger (only Timer3)
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 12-1: TIMER2 AND TIMER3 BLOCK DIAGRAM (TYPE A, 16-BIT)



Note 1: ADC Event Trigger is only available on Timer3.

REGISTER 14-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1
Auto-shutdown is controlled by CLC2 for MCCP2
Auto-shutdown is controlled by CLC3 for MCCP3
Auto-shutdown is controlled by CLC1 for SCCP4
Auto-shutdown is controlled by CLC2 for SCCP5
Auto-shutdown is controlled by CLC3 for SCCP6
Auto-shutdown is controlled by CLC4 for SCCP7
Auto-shutdown is controlled by CLC1 for SCCP8
Auto-shutdown is controlled by CLC2 for SCCP9
xxx1 xxxx = Auto-shutdown is controlled by the SCCP4 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP1 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx 1xxx = Auto-shutdown is controlled by the SCCP5 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP2 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx x1xx = Auto-shutdown is controlled by Comparator 3
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.
2: This pin is remappable from SCCP modules.

REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 5 **D/A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 2 **R/W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – Indicates data transfer is output from slave
0 = Write – Indicates data transfer is input to slave
Hardware is set or clear after reception of an I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with the received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of the data transmission.

REGISTER 18-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY(1)	—	USUSPEND	USBPWR(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected, but an interrupt is pending; it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit(1)
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

REGISTER 18-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-Bit Frame Number Lower bits
These register bits are updated with the current frame number whenever a SOF token is received.

REGISTER 18-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 Bits of the Frame Numbers bits
These register bits are updated with the current frame number whenever a SOF token is received.

23.0 VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference"** (DS61109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The CVREF module is a 32-TAP DAC that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently from them.

The module's supply reference can be provided from either the device VDD/VSS or an external voltage reference pin. The CVREF output is available for the comparators and for pin output.

The voltage reference has the following features:

- 32 Output Levels are Available
- Internally Connected to Comparators to Conserve Device Pins
- Output can be Connected to a Pin

A block diagram of the CVREF module is illustrated in Figure 23-1.

FIGURE 23-1: VOLTAGE REFERENCE BLOCK DIAGRAM

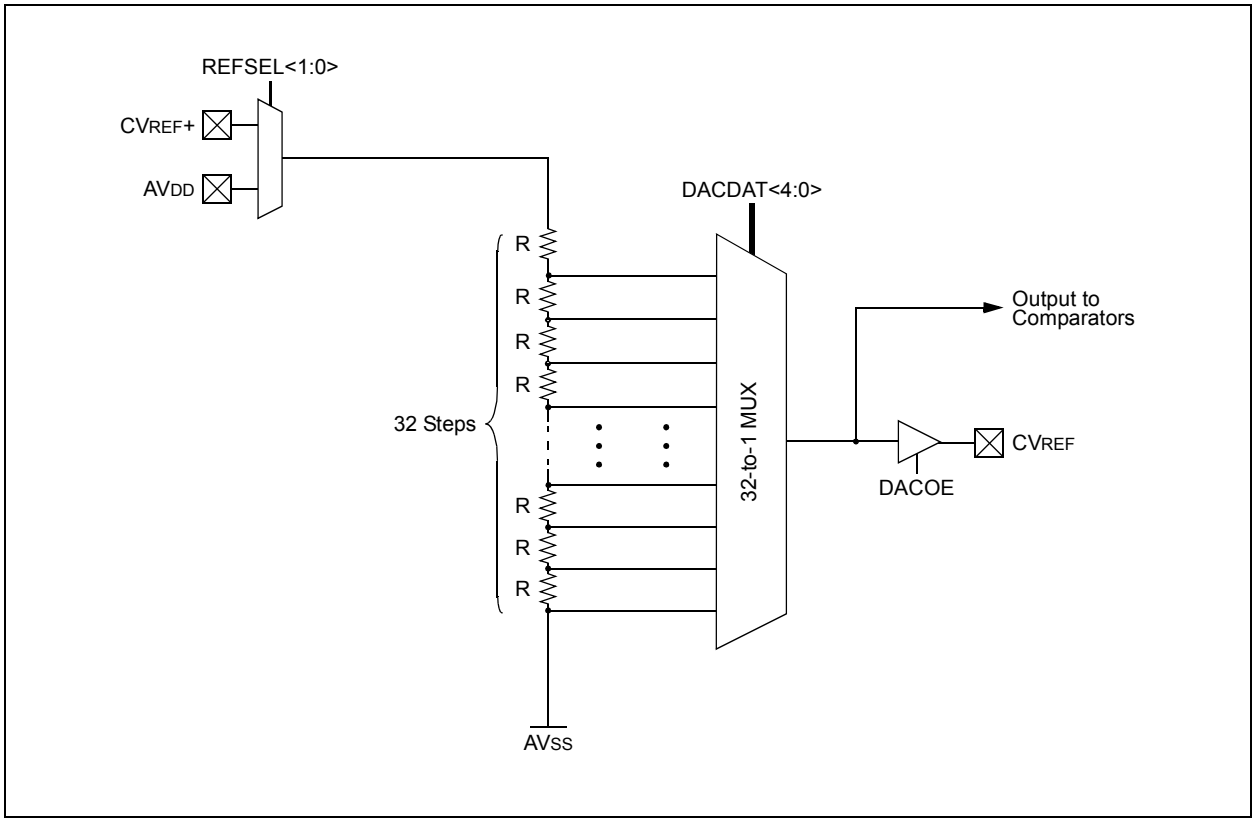


TABLE 29-14: COMPARATOR DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	-20	—	+20	mV	**(Note 1)**
D301	VICM	Input Common-Mode Voltage	VSS – 0.3V	—	VDD + 0.3V	V	**(Note 1)**
D307	TRESP	Response Time	—	150	—	ns	**(Note 2)**

Note 1: Parameters are characterized but not tested.

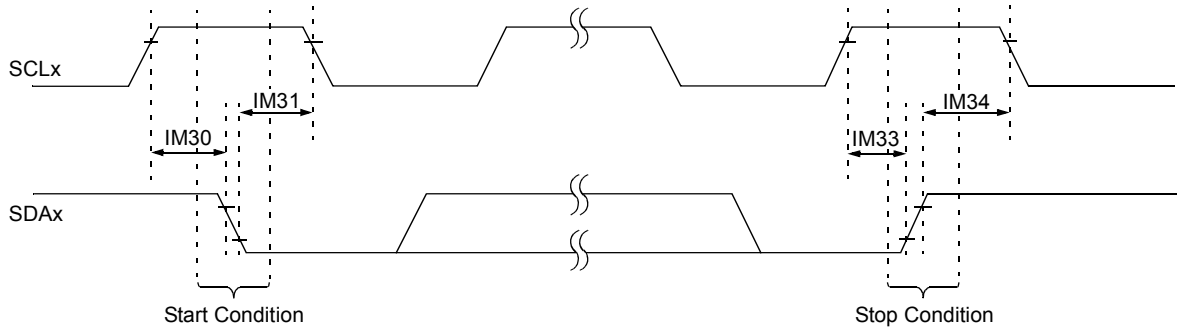
2: Measured with one input at VDD/2 and the other transitioning from VSS to VDD, 40 mV step, 15 mV overdrive.

TABLE 29-15: VOLTAGE REFERENCE DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VRD310	TSET	Settling Time	—	—	10	µs	**(Note 1)**
VRD311	VRAA	Absolute Accuracy	-1	—	1	LSb	
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ	

Note 1: Measures the interval while DACDAT<4:0> transitions from '11111' to '00000'.

FIGURE 29-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-2 for load conditions.

FIGURE 29-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

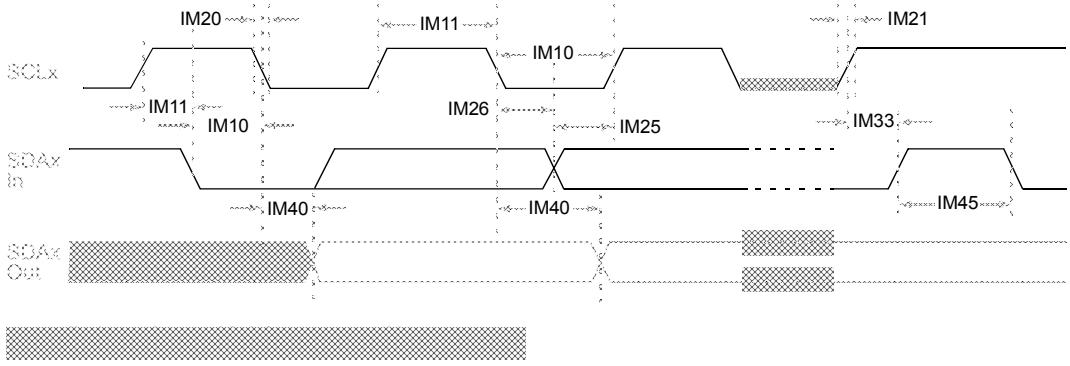


TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.(1)	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	

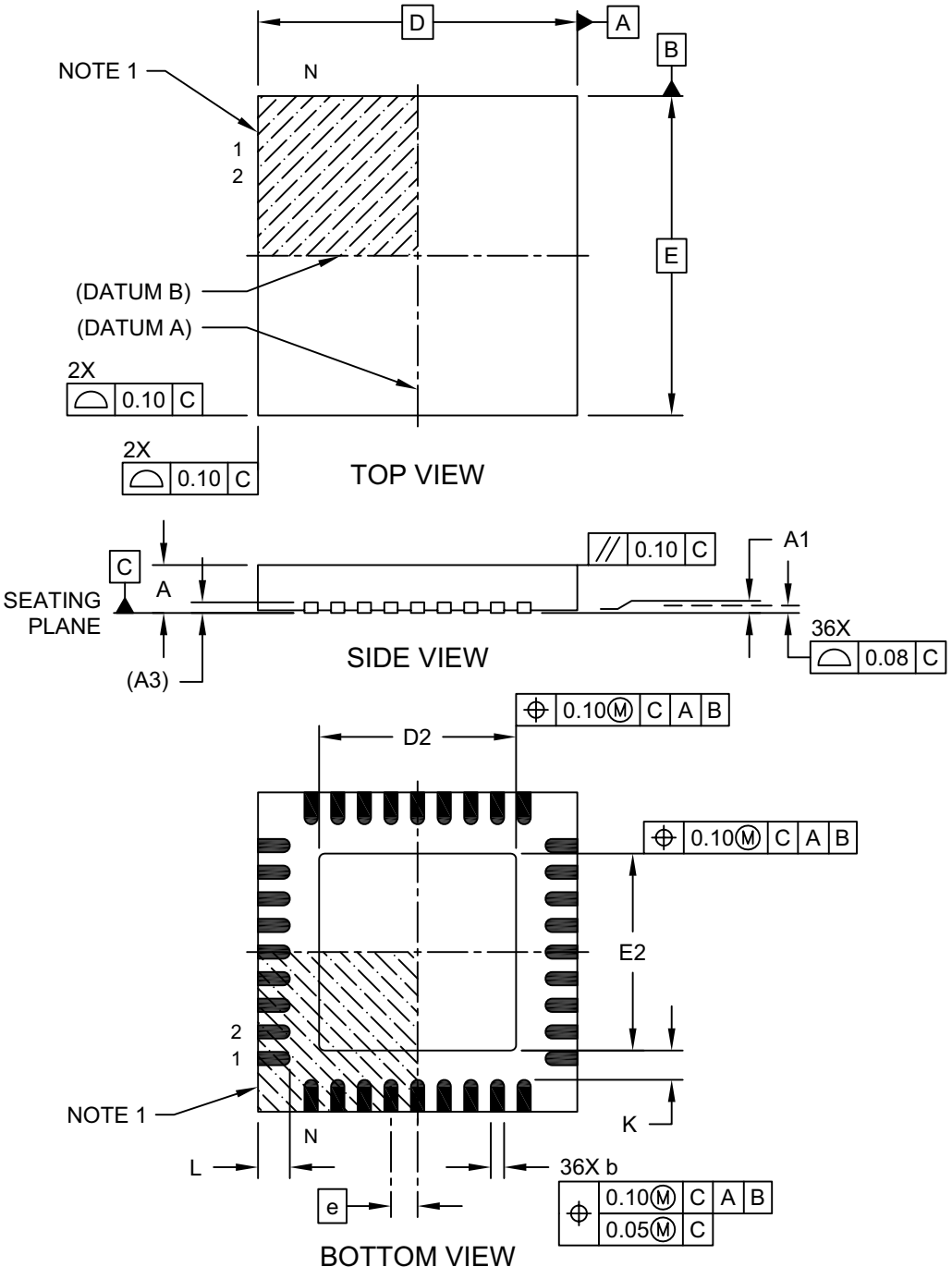
Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN]
SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (January 2016)

This is the initial version of the document.

Revision B (March 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Low-Power Modes"**, **"Peripheral Features"**, **"Microcontroller Features"** and **"Analog Features"** sections.
  - Changed program row size to 128 32-bit words in **Section 5.0 "Flash Program Memory"**.
  - Updated **Section 4.2 "Bus Matrix (BMX)"**, **Section 8.0 "Direct Memory Access (DMA) Controller"**, **Section 9.0 "Oscillator Configuration"**, **Section 9.2 "Clock Switching Operation"**, **Section 9.3 "FRC Active Clock Tuning"**, **Section 10.1 "CLR, SET and INV Registers"**, **Section 10.5 "I/O Port Write/Read Timing"**, **Section 10.6 "GPIO Port Merging"**, **Section 20.1 "Introduction"**, **Section 26.5 "Band Gap Voltage Reference"** and **Section 26.7 "Unique Device Identifier (UDID)"**.
  - Added the 36-Lead VQFN (M2) and 48-Lead UQFN (M4) packaging diagrams to **Section 30.0 "Packaging Information"**.
- Tables:
  - Updated Table 1-1, Table 7-2, Table 7-3, Table 9-1, Table 10-5, Table 10-6, Table 10-7, Table 10-8, Table 20-1, Table 26-3, Table 26-4, Table 26-6, Table 26-8, Table 29-2, Table 29-3, Table 29-4, Table 29-5, Table 29-6, Table 29-7, Table 29-8, Table 29-11, Table 29-14, Table 29-20 and Table 29-21.
  - Replaced Table 29-34 with Table 29-34, Table 29-35 and Table 29-36.
  - Removed previously numbered Table 29-35.
- Examples:
  - Updated Example 9-1.
- Figures:
  - Updated Figure 1-1, Figure 8-1, Figure 9-1, Figure 9-2 and Figure 22-1.
  - Added Figure 9-2.
- Registers:
  - Updated Register 6-4, Register 9-1, Register 9-2, Register 9-3, Register 9-5, Register 14-1, Register 19-1, Register 19-2, Register 26-1,Register 26-5 and Register 26-10.
  - Removed Register 9-7.

Revision C (May 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Peripheral Features"** section.
  - Updated **Section 2.3 "Master Clear (MCLR) Pin"** and **Section 25.3 "Retention Sleep Mode"**.
- Tables:
  - Updated Table 29-4, Table 29-5, Table 29-6 and Table 29-7.
- Registers:
  - Updated Register 13-1.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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