Microchip Technology - PIC32MM0128GPM028T-I/SS Datasheet

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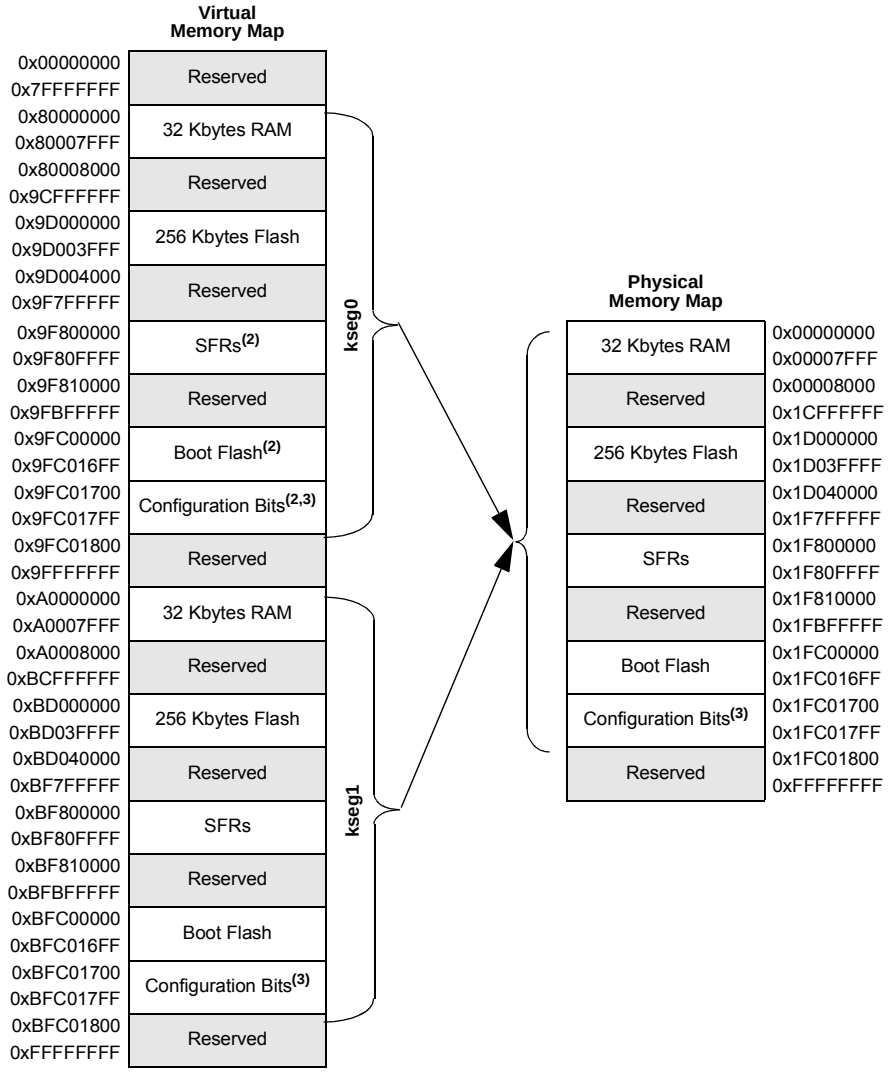
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0128gpm028t-i-ss

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

REGISTER 6-1: RCON: RESET CONTROL REGISTER (CONTINUED)

bit 3 **SLEEP:** Wake from Sleep Flag bit(1)
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake from Idle Flag bit(1,2)
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear these bits to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enables Software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 26.4 "System Registers Write Protection"** for details.
2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8A50	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8A60	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8A70	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
8A80	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
8A90	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
8AA0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
8AB0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8AC0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8AD0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
8AE0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8AF0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8B00	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
8B10	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8B20	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8B30	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

REGISTER 13-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to the upper 16 bits of this register address using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
On Reset, this bit is set to the inverse of the value of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

REGISTER 14-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	OPSSRC(1)	RTRGEN(2)	—	—	OPS<3:0>(3)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TMRPS<1:0>		T32	CCSEL	MOD<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OPSSRC:** Output Postscaler Source Select bit(1)
- 1 = Output postscaler scales the Special Event Trigger output events
- 0 = Output postscaler scales the timer interrupt events

bit 30 **RTRGEN:** Retrigger Enable bit(2)
- 1 = Time base can be retriggered when CCPTRIG = 1
- 0 = Time base may not be retriggered when CCPTRIG = 1

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **OPS<3:0>:** CCPx Interrupt Output Postscale Select bits(3)
- 1111 = Interrupt every 16th time base period match
- 1110 = Interrupt every 15th time base period match
- . . .
- 0100 = Interrupt every 5th time base period match
- 0011 = Interrupt every 4th time base period match or 4th input capture event
- 0010 = Interrupt every 3rd time base period match or 3rd input capture event
- 0001 = Interrupt every 2nd time base period match or 2nd input capture event
- 0000 = Interrupt after each time base period match or input capture event

bit 23 **TRIGEN:** CCPx Triggered Enable bit
- 1 = Triggered operation of the timer is enabled
- 0 = Triggered operation of the timer is disabled

bit 22 **ONESHOT:** One-Shot Mode Enable bit
- 1 = One-Shot Triggered mode is enabled; trigger duration is set by OSCNT<2:0>
- 0 = One-Shot Triggered mode is disabled

bit 21 **ALTSYNC:** CCPx Clock Select bit
- 1 = An alternate signal is used as the module synchronization output signal
- 0 = The module synchronization output signal is the Time Base Reset/rollover event

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

18.4 Powering the USB Transceiver

The VUSB3V3 pin is used to power the USB transceiver. During USB operation, this provides the power for USB transceiver drivers. When the USB module is disabled, this pin can be used to bias the transceiver circuit to prevent additional current draw when using RB10 and/or RB11 as GPIOs.

Available options for VUSB power:

1. For USB operation, an external power source is required. For voltage compliant USB operation, the voltage applied to VUSB3V3 must be in the range specified by Parameter USB313 in Table 29-38 regardless of the device operating voltage. If the device VDD voltage meets these requirements, it can be used to power VUSB3V3.
2. For non-USB operation with RB11 and/or RB10 as GPIOs, the USB module must be disabled and power applied to VUSB3V3 via VDD.
3. For non-USB operation without using RB11 and/or RB10, the VUSB3V3 pin should be connected to ground. This configuration has the lowest operating current.

Note:	To prevent additional current draw, VUSB3V3 must either be powered or grounded.

18.4.1 OPERATION OF PORT PINS SHARED WITH THE USB TRANSCEIVER

The USB transceiver shares pins with GPIO port pins. The D+ pin is shared with RB11 and the D- pin is shared with RB10. When the USB module is enabled, the pins are controlled by the module as D+ and D-, and are not usable as GPIOs. When the module is disabled, the pins can be used as RB11 and RB10 GPIOs if the VUSB3V3 pin is powered internally or externally. Refer to **Section 18.4 "Powering the USB Transceiver"** for more information.

REGISTER 18-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low speed
0 = Next token command to be executed at full speed

bit 6-0 **DEVADDR<6:0>:** 7-Bit USB Device Address bits

REGISTER 19-2: RTCCON2: RTCC CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	PS<1:0>		—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter for the seconds output.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **PS<1:0>:** Prescale Select bits
Sets the prescaler for the seconds output.
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

20.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- **AD1CON1: ADC Control Register 1**
- **AD1CON2: ADC Control Register 2**
- **AD1CON3: ADC Control Register 3**
- **AD1CON5: ADC Control Register 5**

  The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.
- **AD1CHS: ADC Input Select Register**

  The AD1CHS register selects the input pins to be connected to the SHA.
- **AD1CSS: ADC Input Scan Select Register**

  The AD1CSS register selects inputs to be sequentially scanned.
- **AD1CHIT: ADC Compare Hit Register**

  The AD1CHIT register indicates the channels meeting specified comparison requirements.

Table 20-1 provides a summary of all ADC related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

REGISTER 20-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HSC	R/W-0, HSC
	SSRC<3:0>				MODE12	ASAM	SAMP(2)	DONE(1)

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit
1 = ADC module is operating
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** ADC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits

For 12-Bit Operation (MODE12 bit = 1):
111 = Signed fractional 32-bit (DOUT = sddd dddd dddd 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dddd 0000 0000 0000 0000 0000)
101 = Signed integer 32-bit (DOUT = ssss ssss ssss ssss ssss sddd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)
011 = Signed fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dddd 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dddd 0000)
001 = Signed integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sddd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)

For 10-Bit Operation (MODE12 bit = 0):
111 = Signed fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
101 = Signed integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
011 = Signed fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
001 = Signed integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

Note 1: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.

2: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).

TABLE 21-1: CLC1, CLC2 AND CLC3 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2480	CLC1CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2490	CLC1SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
24A0	CLC1GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2500	CLC2CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2510	CLC2SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2520	CLC2GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2580	CLC3CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2590	CLC3SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
25A0	CLC3GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2600	CLC4CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2610	CLC4SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2620	CLC4GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = Unused
110 = MCCP1 OCMP compare match event
101 = DMA Channel 0 interrupt
100 = ADC end of conversion
011 = UART1 TX out
010 = CMP1 out
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = Unused
110 = MCCP1 OCMP compare match event
101 = DMA Channel 1 interrupt
100 = ADC end of conversion
011 = UART2 TX out
010 = CMP1 out
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = Reserved
110 = MCCP2 OCMP compare match event
101 = DMA Channel 0 interrupt
100 = ADC end of conversion
011 = UART3 TX out
010 = CMP1 out
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = Reserved
110 = MCCP3 OCMP compare match event
101 = DMA Channel 1 interrupt
100 = ADC end of conversion
011 = Reserved
010 = CMP1 out
001 = CLC3 out
000 = CLCINB I/O pin

bit 7 **Unimplemented:** Read as '0'

REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits
11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Windowed mode is disabled
0 = Windowed mode is enabled

REGISTER 26-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by the SOSC)
- 0 = External clock connected to the SOSCO pin is used (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = CLKO/OSC2 pin operates as normal I/O
- 0 = System clock is connected to the CLKO/OSC2 pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator enable
- 0 = Secondary Oscillator disable

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

REGISTER 26-8: DEVID: DEVICE ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	VER<3:0>(1)				ID<27:24>(1)			
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<23:16>(1)							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<15:8>(1)							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

Note 1: Reset values are dependent on the device variant.

REGISTER 26-9: SYSKEY: SYSTEM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	R/W-1
	SYSKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

A write of 0xAA996655, followed by a write of 0x556699AA to SYSKEY, is required to unlock select system registers. Refer to Example 26-1.

Bit 0 Indicates System Lock Status:

1 = The system is unlocked

0 = The system is locked

NOTES:

27.0 INSTRUCTION SET

The PIC32MM0256GPM064 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0256GPM064 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note:	Refer to the *"MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set"* at www.imgtec.com for more information.

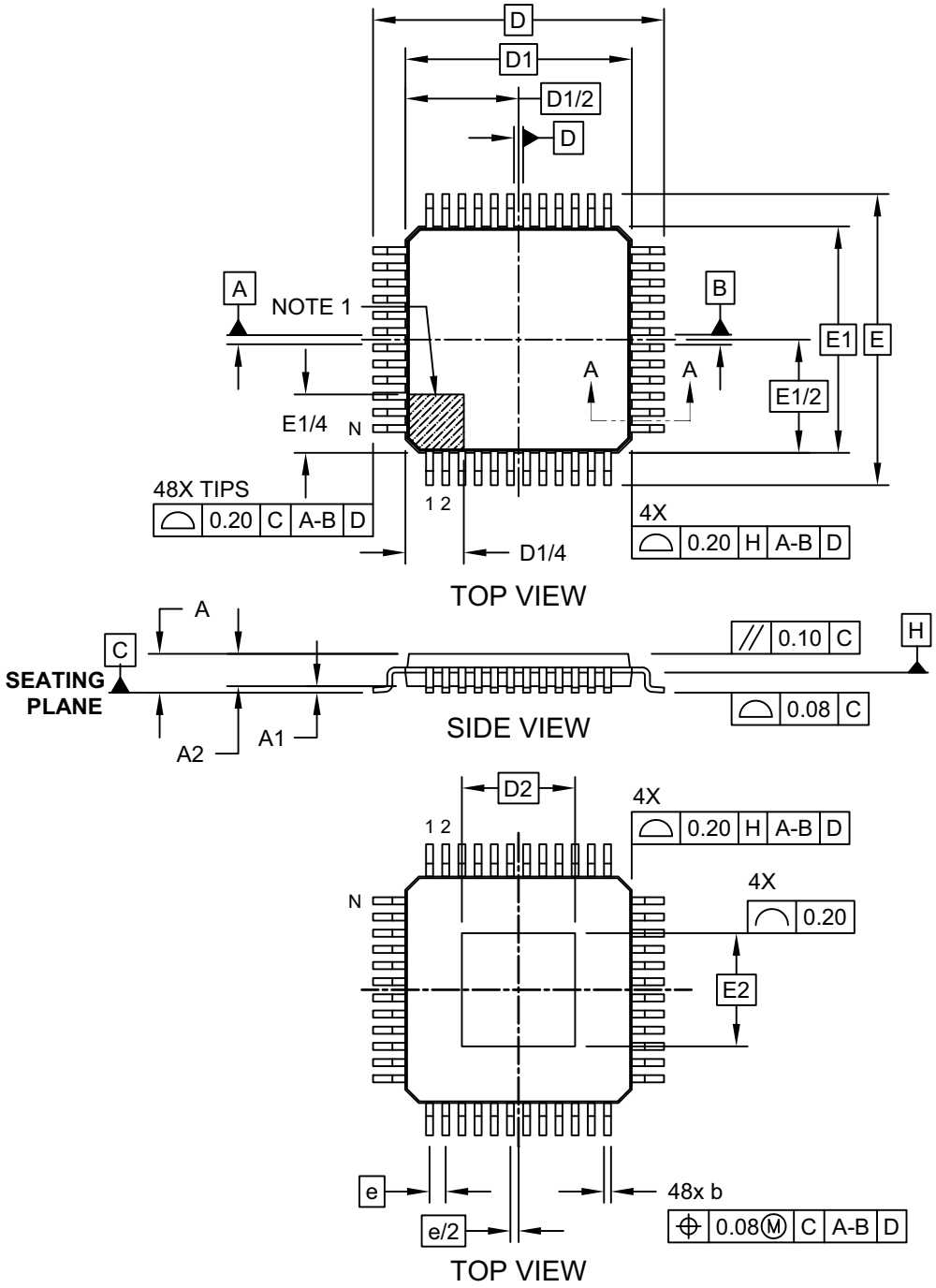
TABLE 29-23: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (Low)	2	—	—	μs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	1	—	μs	Device running or in Idle
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	VDD ≤ VBOR
SY45	TRST	Internal State Reset Time	—	25	—	μs	
SY71	TPM	Program Memory Wake-up Time	—	22	—	μs	Sleep wake-up with VREGS = 0
			—	3.8	—	μs	Sleep wake-up with VREGS = 1
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	163	—	μs	Sleep wake-up with VREGS = 0
			—	23	—	μs	Sleep wake-up with VREGS = 1

Note 1: Parameters are for design guidance and are not tested.

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-183A Sheet 1 of 2