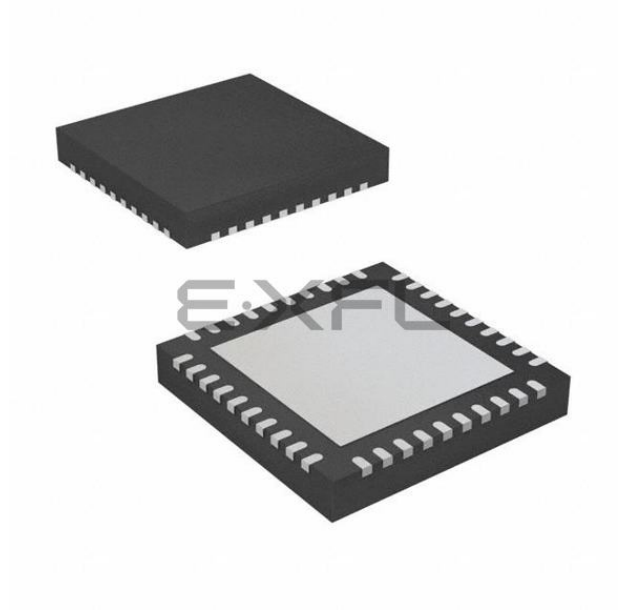
Microchip Technology - PIC32MM0128GPM036-I/MV Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0128gpm036-i-mv

Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I^2C	USB	Packages
							Dedicated 16-Bit Timers	UART(1)/LIN/J2602	MCCP(4)	SCCP(3)	CLC	SPI(2)/I^2S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.

2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.

3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
INT0	26	23	29	32	16	32	I	ST	External Interrupt 0
INT1	25	22	28	31	15	31	I	ST	External Interrupt 1
INT2	18	15	19	20	1	49	I	ST	External Interrupt 2
INT3	2	27	33	36	40	36	I	ST	External Interrupt 3
LVDIN	24	21	20	21	4	52	I	ANA	High/Low-Voltage Detect input
$\overline{\text{MCLR}}$	1	26	32	35	19	9	I	ST	Master Clear (device Reset)
OCM1A	17	14	18	18	48	7	O	DIG	MCCP1 Output A
OCM1B	18	15	19	20	1	53	O	DIG	MCCP1 Output B
OCM1C	9	6	7	7	32	25	O	DIG	MCCP1 Output C
OCM1D	10	7	8	8	41	37	O	DIG	MCCP1 Output D
OCM1E	2	27	33	36	40	36	O	DIG	MCCP1 Output E
OCM1F	3	28	34	37	22	12	O	DIG	MCCP1 Output F
OCM2A	19	16	5	5	29	21	O	DIG	MCCP2 Output A
OCM2B	26	23	29	32	39	35	O	DIG	MCCP2 Output B
OCM2C	4	1	35	38	23	13	O	DIG	MCCP2 Output C
OCM2D	5	2	36	39	24	14	O	DIG	MCCP2 Output D
OCM2E	6	3	1	1	25	15	O	DIG	MCCP2 Output E
OCM2F	7	4	2	2	26	16	O	DIG	MCCP2 Output F
OCM3A	24	21	11	11	37	54	O	DIG	MCCP3 Output A
OCM3B	25	22	28	31	15	33	O	DIG	MCCP3 Output B
OCM3C	11	8	9	9	35	59	O	DIG	MCCP3 Output C
OCM3D	12	9	10	10	36	41	O	DIG	MCCP3 Output D
OCM3E	14	11	15	15	45	42	O	DIG	MCCP3 Output E
OCM3F	16	13	17	17	47	45	O	DIG	MCCP3 Output F
OSC1	9	6	7	7	32	25	—	—	Primary Oscillator crystal
OSC2	10	7	8	8	33	26	—	—	Primary Oscillator crystal
PGEC1	5	2	36	39	24	14	I	ST	ICSP™ Port 1 programming clock input
PGEC2	2	27	33	36	21	11	I	ST	ICSP Port 2 programming clock input
PGEC3	19	16	21	22	5	55	I	ST	ICSP Port 3 programming clock input
PGED1	4	1	35	38	23	13	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	3	28	34	37	22	12	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	14	11	15	15	45	43	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	12	9	10	10	36	29	I	ST	Real-Time Clock 50/60 Hz clock input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

7.2 Interrupts

The PIC32MM0256GPM064 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS61108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_EXTERNAL_0_VECTOR	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_EXTERNAL_3_VECTOR	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
PORTD Change Notification	_CHANGE_NOTICE_D_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
RESERVED		12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
RESERVED		13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
RESERVED		14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
RESERVED		15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
RESERVED		16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	No
Timer1	_TIMER_1_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
Timer2	_TIMER_2_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer3	_TIMER_3_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
RESERVED		20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	No
RESERVED		21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	No
RESERVED		22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No
Comparator 1	_COMPARATOR_1_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Comparator 2	_COMPARATOR_2_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Comparator 3	_COMPARATOR_3_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	No

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	IPC20	31:16	—	—	—	CCT5IP<2:0>			CCT5IS<1:0>		—	—	—	CCP5IP<2:0>			CCP5IS<1:0>		0000
		15:0	—	—	—	CCT4IP<2:0>			CCT4IS<1:0>		—	—	—	CCP4IP<2:0>			CCP4IS<1:0>		0000
F210	IPC21	31:16	—	—	—	CCT7IP<2:0>			CCT7IS<1:0>		—	—	—	CCP7IP<2:0>			CCP7IS<1:0>		0000
		15:0	—	—	—	CCT6IP<2:0>			CCT6IS<1:0>		—	—	—	CCP6IP<2:0>			CCP6IS<1:0>		0000
F220	IPC22	31:16	—	—	—	CCT9IP<2:0>			CCT9IS<1:0>		—	—	—	CCP9IP<2:0>			CCP9IS<1:0>		0000
		15:0	—	—	—	CCT8IP<2:0>			CCT8IS<1:0>		—	—	—	CCP8IP<2:0>			CCP8IS<1:0>		0000
F230	IPC23	31:16	—	—	—	CPCIP<2:0>			CPCIS<1:0>		—	—	—	NVMIP<2:0>			NVMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	FSTIP<2:0>			FSTIS<1:0>		0000
F240	IPC24	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	ECCBEIP<2:0>			ECCBEIS<1:0>		—	—	—	—	—	—	—	—	0000
F250	IPC25	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 8-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate an LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 8-12: DCHxSSIZ: DMA CHANNEL x SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535-byte source size
•
•
•
0000000000000010 = 2-byte source size
0000000000000001 = 1-byte source size
0000000000000000 = 65,536-byte source size

REGISTER 8-13: DCHxDSIZ: DMA CHANNEL x DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535-byte destination size
•
•
•
0000000000000010 = 2-byte destination size
0000000000000001 = 1-byte destination size
0000000000000000 = 65,536-byte destination size

TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0430	CCP4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0440	CCP4TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0450	CCP4PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0460	CCP4RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0470	CCP4RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0480	CCP4BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0500	CCP5CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0510	CCP5CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0520	CCP5CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0530	CCP5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0540	CCP5TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0550	CCP5PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0560	CCP5RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0570	CCP5RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0580	CCP5BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 11 **STRICT:** Strict I^2C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced; device does not respond to reserved address space or generates addresses in reserved address space
0 = Strict I^2C reserved address rule is not enabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with the SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^2C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on the SDAx and SCLx pins and transmits the ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

TABLE 18-1: USB OTG REGISTER MAP (CONTINUED)

Virtual Address (BF88_ #)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8770	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8780	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8790	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

REGISTER 18-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
1 = No cable is attached or a "Type B" cable has been inserted into the USB receptacle
0 = A "Type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
1 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has been stable for the previous 1 ms
0 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
1 = The VBUS voltage is above VA_SESS_VLD (as defined in the USB OTG Specification) on the A or B-device
0 = The VBUS voltage is below VA_SESS_VLD on the A or B-device

bit 2 **SESEND:** B-Device Session End Indicator bit
1 = The VBUS voltage is above VB_SESS_END (as defined in the USB OTG Specification) on the B-device
0 = The VBUS voltage is below VB_SESS_END on the B-device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
1 = The VBUS voltage is above VA_VBUS_VLD (as defined in the USB OTG Specification) on the A-device
0 = The VBUS voltage is below VA_VBUS_VLD on the A-device

REGISTER 18-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** Stall Handshake Interrupt Enable bit
- 1 = Stall interrupt is enabled
- 0 = Stall interrupt is disabled

bit 6 **ATTACHIE:** Attach Interrupt Enable bit
- 1 = Attach interrupt is enabled
- 0 = Attach interrupt is disabled

bit 5 **RESUMEIE:** Resume Interrupt Enable bit
- 1 = Resume interrupt is enabled
- 0 = Resume interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB error interrupt is enabled
- 0 = USB error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
2: Device mode.
3: Host mode.

19.1 RTCC Control Registers

TABLE 19-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>								0000
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>																0000
		15:0	FDIV<4:0>					—	—	—	—	—	PS<1:0>		—	—	CLKSEL<1:0>		0000
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

bit 11 **WRLOCK:** RTCC Registers Write Lock bit
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

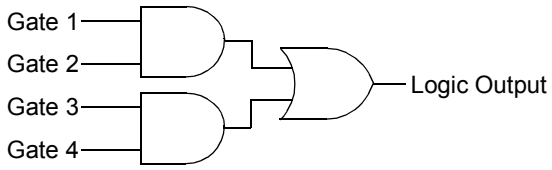
bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
• • •
011 = Reserved
010 = RTCC input clock source (user-defined divided output based on the combination of the RTCCON2 bits, DIV<15:0> and PS<1:0>)
001 = Seconds clock
000 = Alarm event

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

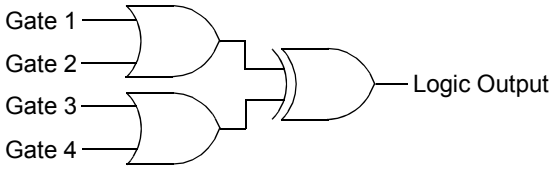
FIGURE 21-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

AND – OR



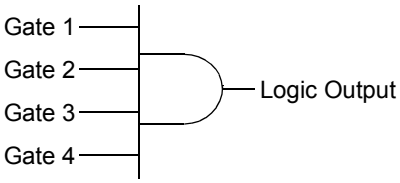
MODE<2:0> = 000

OR – XOR



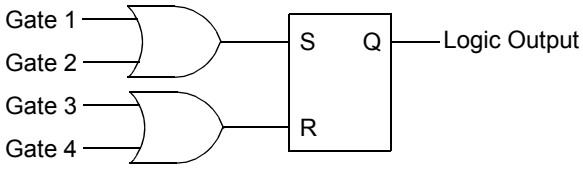
MODE<2:0> = 001

4-Input AND



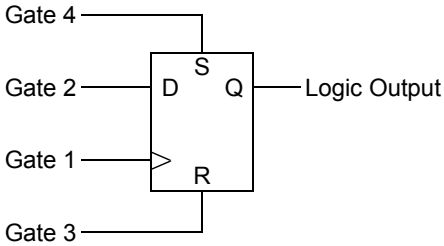
MODE<2:0> = 010

S-R Latch



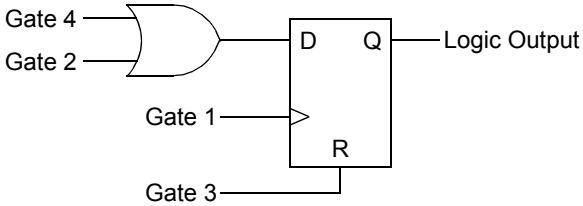
MODE<2:0> = 011

1-Input D Flip-Flop with S and R



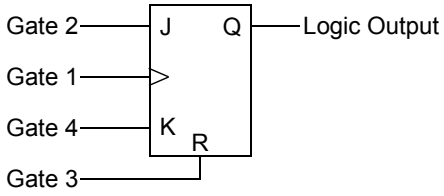
MODE<2:0> = 100

2-Input D Flip-Flop with R



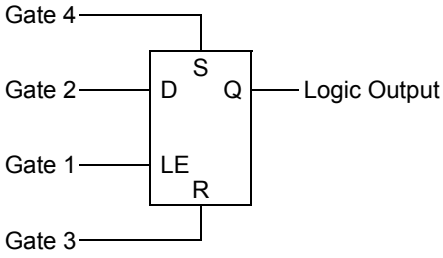
MODE<2:0> = 101

J-K Flip-Flop with R



MODE<2:0> = 110

1-Input Transparent Latch with S and R



MODE<2:0> = 111

REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS4<2:0>			—	DS3<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS2<2:0>			—	DS1<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = MCCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = MCCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

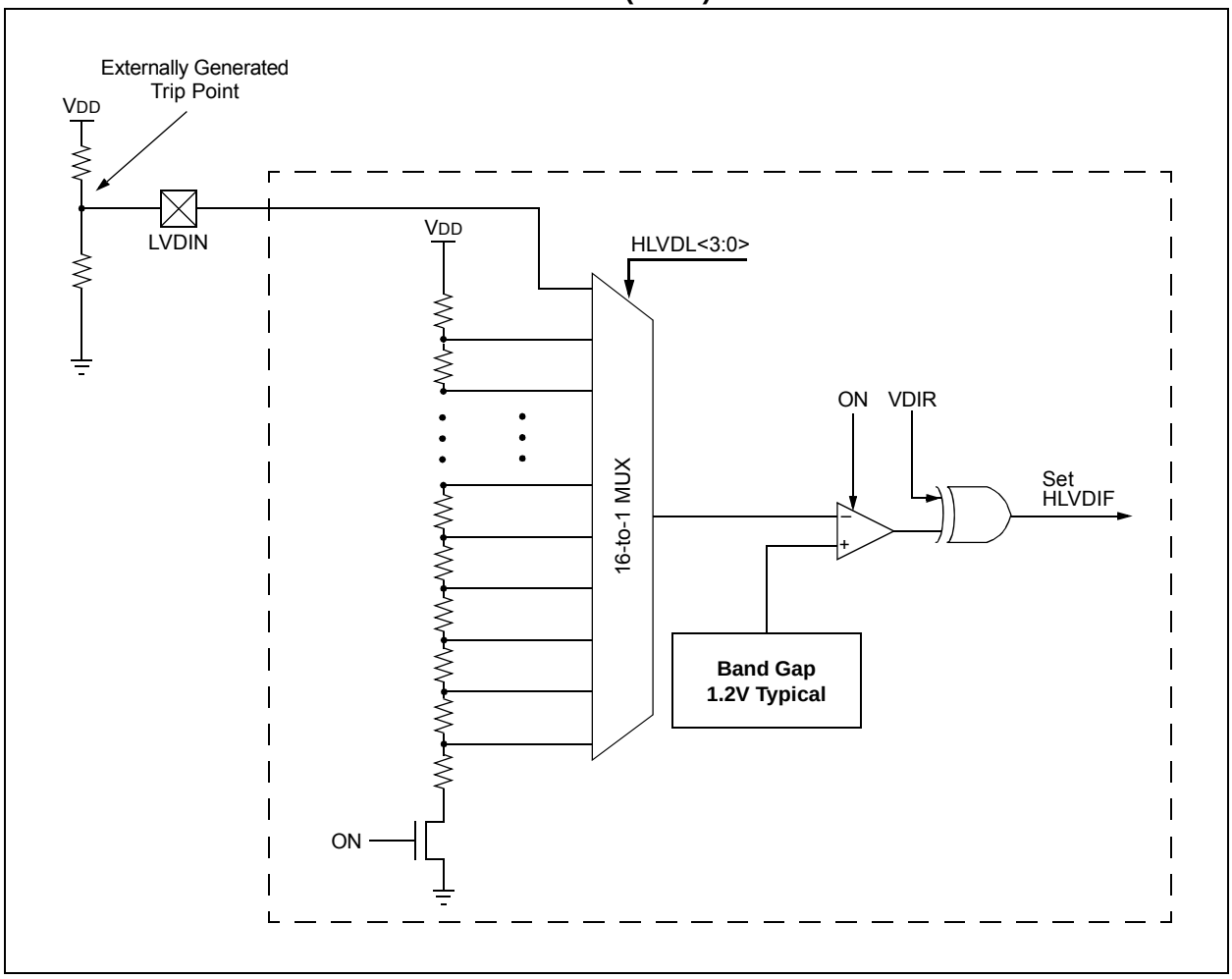
24.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 24-1) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

FIGURE 24-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	HLVDL<3:0>			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** HLVD Power Enable bit
- 1 = HLVD is enabled
- 0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** HLVD Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **VDIR:** Voltage Change Direction Select bit
- 1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
- 0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 10 **BGVST:** Band Gap Voltage Stable Flag bit
- 1 = Indicates that the band gap voltage is stable
- 0 = Indicates that the band gap voltage is unstable

bit 9 **IRVST:** Internal Reference Voltage Stable Flag bit
- 1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
- 0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 8 **HLEVT:** High/Low-Voltage Detection Event Status bit
- 1 = Indicates HLVD event is active
- 0 = Indicates HLVD event is not active

bit 7-4 **Unimplemented:** Read as '0'

TABLE 26-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

28.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

28.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

28.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

28.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.