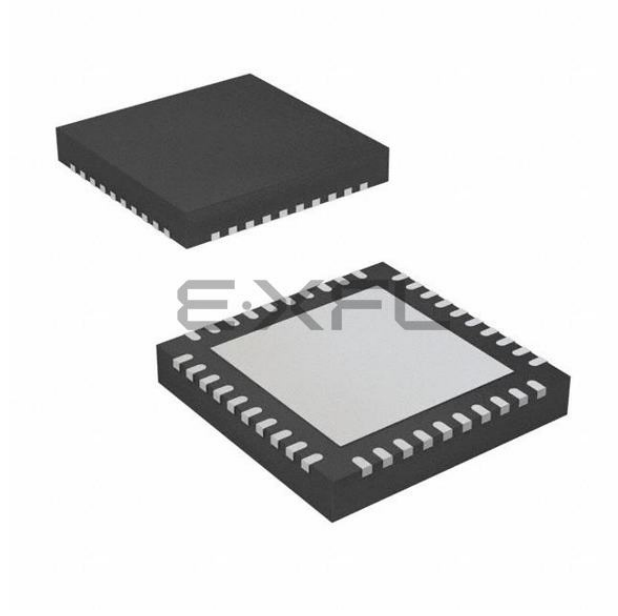
Microchip Technology - PIC32MM0128GPM036T-I/MV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0128gpm036t-i-mv

4.0 MEMORY ORGANIZATION

PIC32MM microcontrollers provide 4 GBytes of unified virtual memory address space. All memory regions, including program memory, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The data memory can be made executable, allowing the CPU to execute code from data memory.

Key features include:

- 32-Bit Native Data Width
- Separate Boot Flash Memory (BFM) for Protected Code
- Robust Bus Exception Handling to Intercept Runaway Code
- Simple Memory Mapping with Fixed Mapping Translation (FMT) Unit

The PIC32MM0256GPM064 family devices implement two address spaces: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions. Physical addresses are used by peripherals, such as Flash controllers, that access memory independently of the CPU.

The virtual address space is divided into two segments of 512 Mbytes each, labeled kseg0 and kseg1. The Program Flash Memory (PFM) and Data RAM Memory (DRM) are accessible from either kseg0 or kseg1, while the Boot Flash Memory (BFM) and peripheral SFRs are accessible only from kseg1.

The Fixed Mapping Translation (FMT) unit translates the memory segments into corresponding physical address regions. Figure 4-1 through Figure 4-3 illustrate the fixed mapping scheme, implemented by the PIC32MM0256GPM064 family core, between the virtual and physical address space.

The mapping of the memory segments depends on the CPU error level, set by the ERL bit in the CPU STATUS register. Error level is set (ERL = 1) by the CPU on a Reset, Soft Reset or Non-Maskable Interrupt (NMI). In this mode, the CPU can access memory by the physical address. This mode is provided for compatibility with other MIPS processor cores that use a TLB-based MMU. The C start-up code clears the ERL bit to zero, so that when application software starts up, it sees the proper virtual to physical memory mapping.

4.1 Alternate Configuration Bits Space

Every Configuration Word has an associated Alternate Word (designated by the letter A as the first letter in the name of the word). During device start-up, Primary Words are read, and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and Alternate Words are used. If uncorrectable ECC errors are found in Primary and Alternate Words, the BCFGFAIL (RCON<26>) flag is set, and the default configuration is used. The Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. The Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768.

4.2 Bus Matrix (BMX)

The BMX is a switch fabric that connects the system bus initiators (Flash controller, CPU instruction, CPU data, system DMA and USB) to bus targets (RAM, Flash and peripherals without integrated DMA). All data and instructions are transferred through this bus. Only one initiator can connect to a given target at a time. Multiple initiators can be active at one time provided each one has a separate target. Multiple priority modes (Round Robin, Fixed CPU Highest and Fixed CPU Lowest) are available to allow the priority to be tailored to the application needs. Mode 0 is a Fixed Priority mode with the CPU having the highest priority (refer to Table 4-1). For most applications, this mode should be sufficient; however, it is possible for the CPU to generate sufficient bus traffic to 'starve' the other initiators attempting to access Flash memory, preventing them from performing transfers in the required time limit. If this 'starvation' occurs, the Round Robin or CPU Lowest mode should be chosen.

Mode 1 is a Fixed Priority mode with the CPU having the lowest priority (refer to Table 4-1). This mode can reduce the latency of DMA transfers because the DMA engines have a higher priority than the CPU.

Mode 2 is a Round Robin or Rotating Priority mode. The initiator's priority for each target rotates with every access. This ensures, not that the initiator is starved, but the latency for accesses changes with every access; this makes the latency variable.

The Arbitration mode is selected by the BMXARB<1:0> bits (CFGCON<25:24>).

Note:	The CPU has two initiators: one for data and the other for instructions. In all Arbitration modes, the CPU data initiator has higher priority than the CPU instruction initiator.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	_general_exception_handler
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	_general_exception_handler
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	_general_exception_handler
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	_general_exception_handler
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	_general_exception_handler
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

NOTES:

13.1 Watchdog Timer Control Registers

TABLE 13-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3990	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 14-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1
Auto-shutdown is controlled by CLC2 for MCCP2
Auto-shutdown is controlled by CLC3 for MCCP3
Auto-shutdown is controlled by CLC1 for SCCP4
Auto-shutdown is controlled by CLC2 for SCCP5
Auto-shutdown is controlled by CLC3 for SCCP6
Auto-shutdown is controlled by CLC4 for SCCP7
Auto-shutdown is controlled by CLC1 for SCCP8
Auto-shutdown is controlled by CLC2 for SCCP9
xxx1 xxxx = Auto-shutdown is controlled by the SCCP4 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP1 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx 1xxx = Auto-shutdown is controlled by the SCCP5 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP2 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx x1xx = Auto-shutdown is controlled by Comparator 3
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.
2: This pin is remappable from SCCP modules.

REGISTER 14-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	OETRIG	OSCNT<2:0>			—	OUTM<2:0>(1)		
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	POLACE	POLBDF(1)	PSSACE<1:0>		PSSBDF<1:0>(1)	
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DT<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **OETRIG:** PWM Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1), the module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 30-28 **OSCNT<2:0>:** One-Shot Event Count bits
Extends the duration of a one-shot trigger event by an additional n clock cycles (n + 1 total cycles).
111 = 7 timer count periods (8 cycles total)
110 = 6 timer count periods (7 cycles total)
101 = 5 timer count periods (6 cycles total)
100 = 4 timer count periods (5 cycles total)
011 = 3 timer count periods (4 cycles total)
010 = 2 timer count periods (3 cycles total)
001 = 1 timer count period (2 cycles total)
000 = Does not extend the one-shot trigger event (the event takes 1 timer count period)

bit 27 **Unimplemented:** Read as '0'

bit 26-24 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 23-22 **Unimplemented:** Read as '0'

bit 21 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 20 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

Note 1: These bits are implemented in MCCP modules only.

REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event

bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFO1 is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit(4)
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at end of data output time
0 = Input data is sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

18.5 Control Registers

REGISTER 18-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to Clear bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = Change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input was detected
- 0 = No change on the session valid input was detected

REGISTER 18-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** Stall Handshake Interrupt Enable bit
- 1 = Stall interrupt is enabled
- 0 = Stall interrupt is disabled

bit 6 **ATTACHIE:** Attach Interrupt Enable bit
- 1 = Attach interrupt is enabled
- 0 = Attach interrupt is disabled

bit 5 **RESUMEIE:** Resume Interrupt Enable bit
- 1 = Resume interrupt is enabled
- 0 = Resume interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB error interrupt is enabled
- 0 = USB error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
2: Device mode.
3: Host mode.

19.1 RTCC Control Registers

TABLE 19-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>								0000
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>																0000
		15:0	FDIV<4:0>					—	—	—	—	—	PS<1:0>		—	—	CLKSEL<1:0>		0000
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

24.1 High/Low-Voltage Detect Registers

TABLE 24-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2920	HLVDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT	—	—	—	—	HLVDL<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

25.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family "Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes the power-saving features for the PIC32MM0256GPM064 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

25.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a Wake-up Delay based on the Oscillator Selection
- The Fail-Safe Clock Monitor (FSCM) does not Operate During Sleep mode
- The BOR Circuit remains Operative during Sleep mode
- The WDT, if Enabled, is not automatically Cleared prior to Entering Sleep mode
- Some Peripherals can Continue to Operate at Limited Functionality in Sleep mode; these Peripherals include I/O Pins that Detect a Change in the Input Signal, WDT, ADC, UART and Peripherals that use an External Clock Input or the Internal LPRC Oscillator (e.g., RTCC and Timer1)
- I/O Pins Continue to Sink or Source Current in the Same Manner as they do when the Device is not in Sleep

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than or equal to the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

25.2 Standby Sleep Mode

Standby Sleep mode places the voltage regulator in Standby mode. This mode draws less power than Sleep mode but has a longer wake-up time. Standby Sleep mode is entered by setting the VREGS bit (PWRCON<0>) prior to entering Sleep by executing a `WAIT` instruction. All peripherals that can operate in Sleep mode can operate in Standby Sleep mode.

25.3 Retention Sleep Mode

Retention Sleep uses a separate voltage regulator to provide the lowest power Sleep mode. This mode has a longer wake-up time than Sleep or Standby Sleep. This mode is entered by clearing the RETVR Configuration bit (FPOR<2>) and setting the RETEN bit (PWRCON<1>), prior to entering Sleep mode, and executing a `WAIT` instruction.

Only select peripherals, such as Timer1, WDT, RTCC and REFO, can operate in Retention Sleep mode.

Note:	In Retention mode, the maximum peripheral output frequency to an I/O pin must be less than 33 kHz.

Note:	When $\overline{\text{MCLR}}$ is used to wake the device from Retention Sleep, a POR Reset will occur.

25.4 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits
11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Windowed mode is disabled
0 = Windowed mode is enabled

REGISTER 26-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
- 11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
- 10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
- 01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
- 1 = Crystal is used (RA4 and RB4 pins are controlled by the SOSC)
- 0 = External clock connected to the SOSCO pin is used (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
- 1 = CLKO/OSC2 pin operates as normal I/O
- 0 = System clock is connected to the CLKO/OSC2 pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
- 11 = Primary Oscillator is disabled
- 10 = HS Oscillator mode is selected
- 01 = XT Oscillator mode is selected
- 00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
- 1 = Two-Speed Start-up is enabled
- 0 = Two-Speed Start-up is disabled

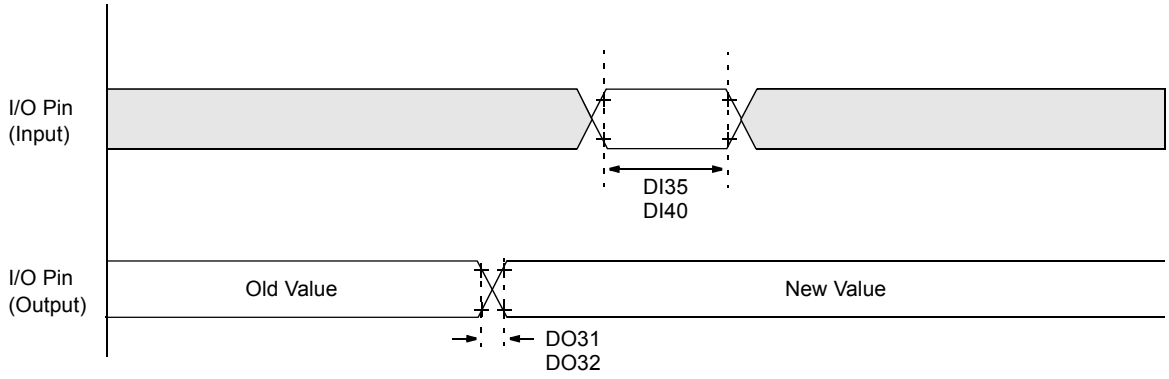
bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Secondary Oscillator enable
- 0 = Secondary Oscillator disable

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
- 1 = FRC oscillator is selected as the PLL reference input on a device Reset
- 0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

FIGURE 29-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-22: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	TCY	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	TCY	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics(1)	Min.	Typical(2)	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.0V
			—	—	15	ns	VDD < 2.0V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(4)	2.5	—	12	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	
SP60	TssL2doV	$\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	

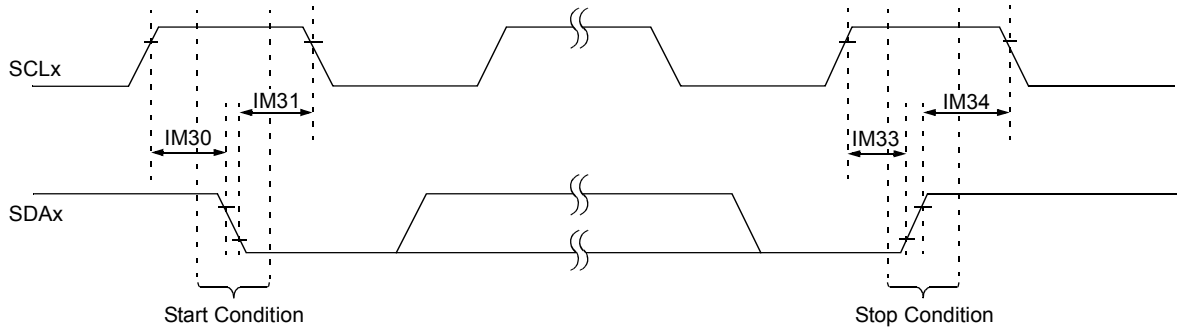
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 10 pF load on all SPIx pins.

FIGURE 29-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-2 for load conditions.

FIGURE 29-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

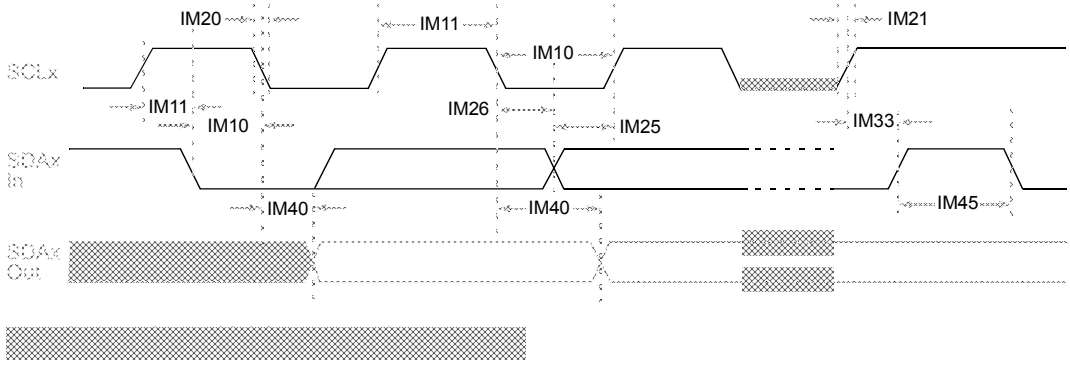


TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.(1)	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	

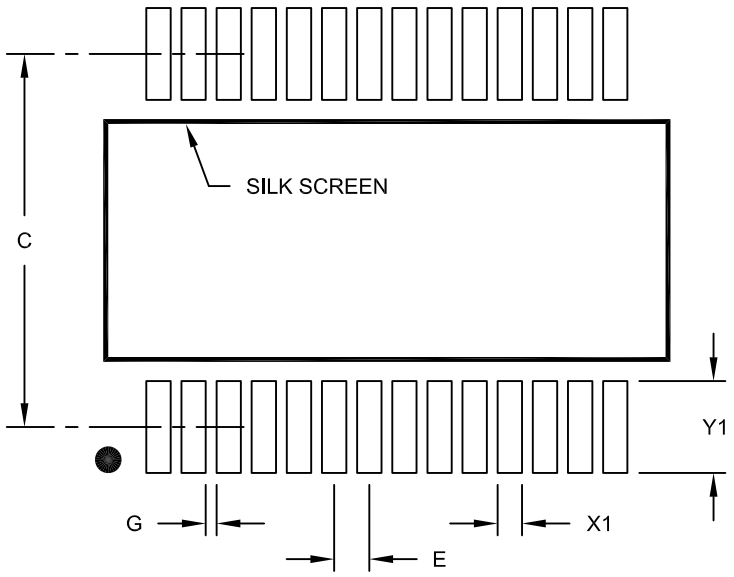
Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

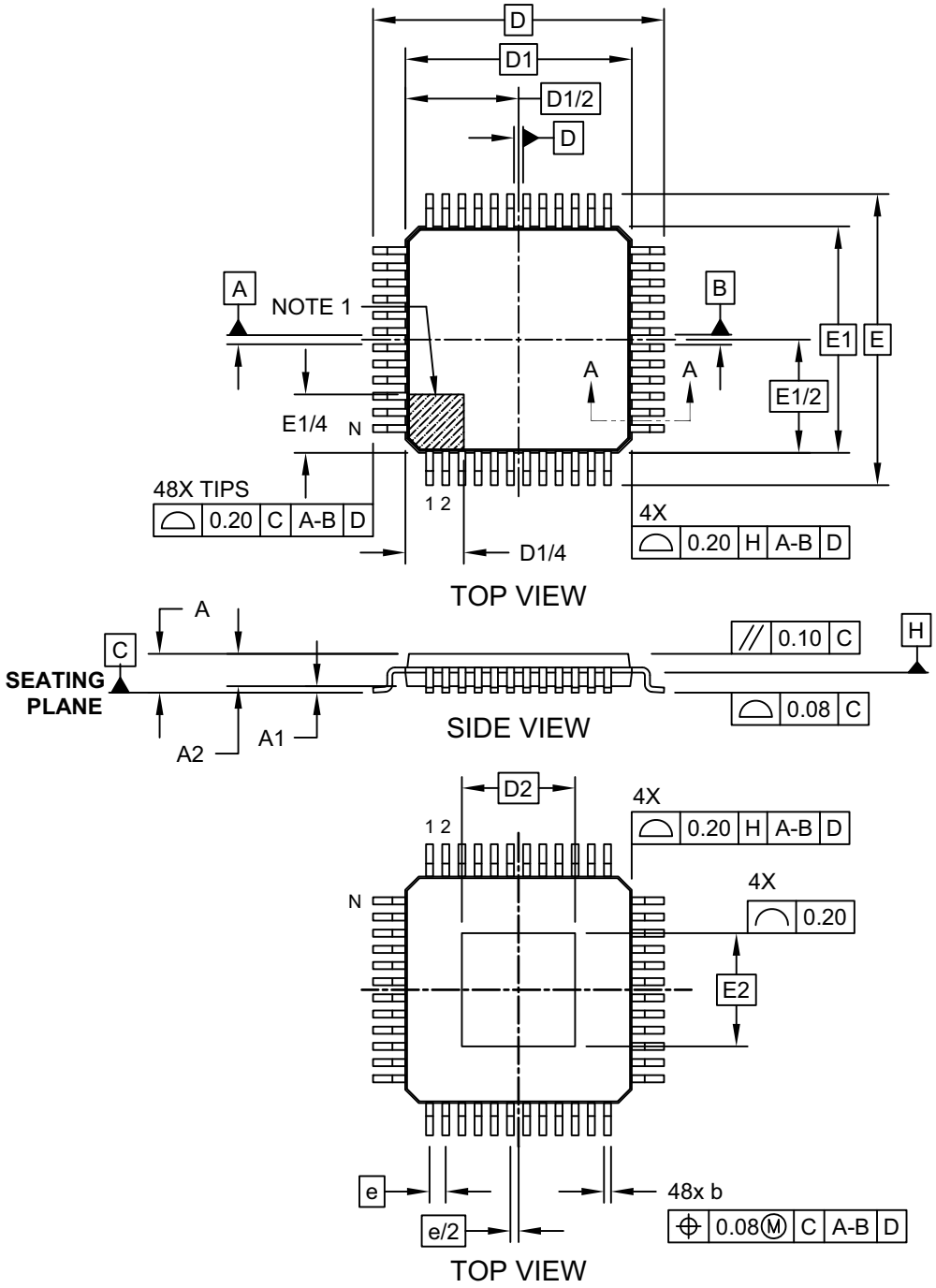
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-183A Sheet 1 of 2