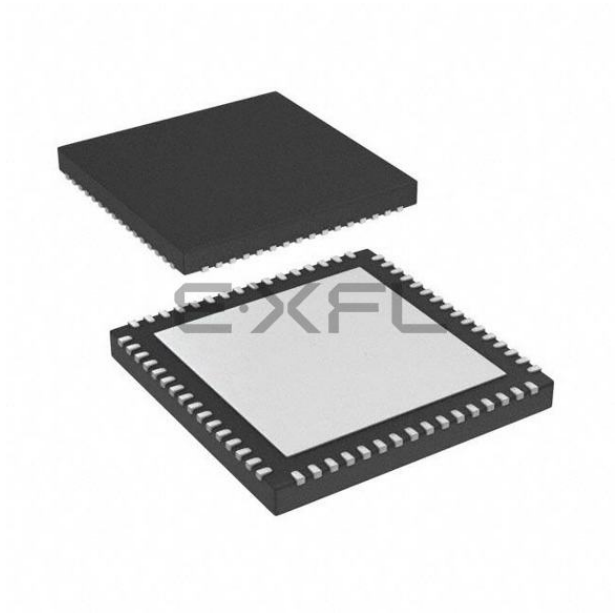
Microchip Technology - PIC32MM0128GPM064-I/MR Datasheet



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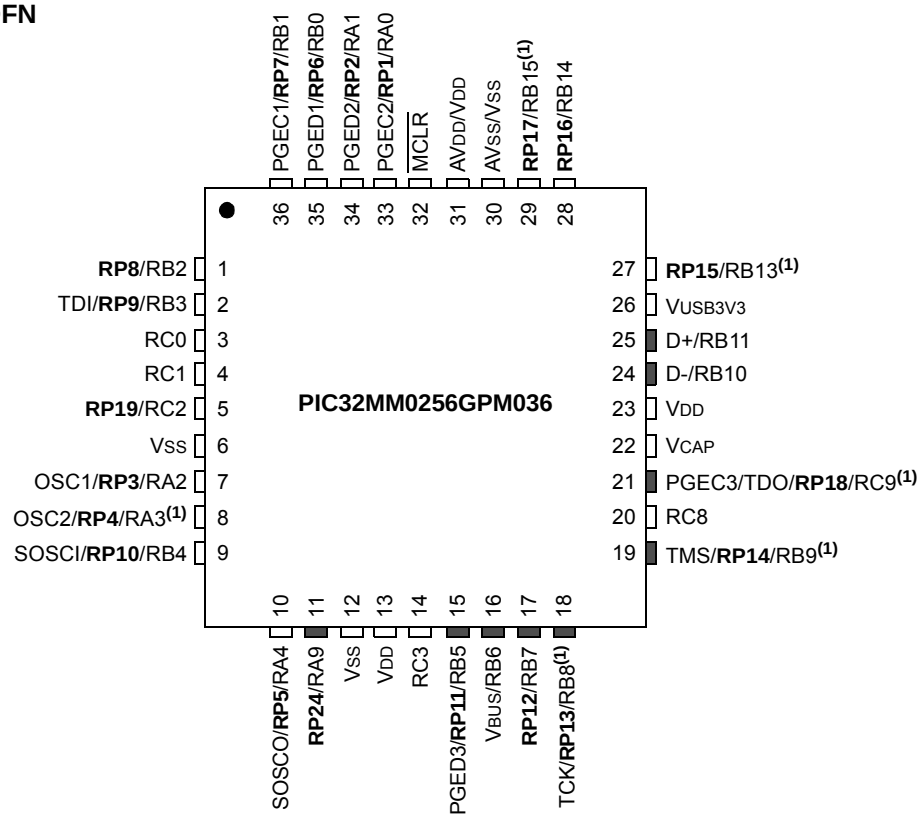
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 20x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0128gpm064-i-mr

Pin Diagrams (Continued)

36-Pin QFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN QFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	19	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	20	AN14/LVDIN/C2INC/RC8
3	AN12/C2IND/T2CK/T2G/RC0	21	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/SDO3/RC9(1)
4	AN13/T3CK/T3G/RC1	22	VCAP
5	**RP19**/OCM2A/RC2	23	VDD
6	VSS	24	D-/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	D+/RB11
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	26	VUSB3V3
9	SOSCI/AN7/**RP10**/OCM3C/RB4	27	AN8/**RP15**/SCL3/SCK3/RB13(1)
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	28	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
11	**RP24**/OCM3A/RA9	29	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
12	VSS	30	AVSS/VSS
13	VDD	31	AVDD/VDD
14	RC3	32	MCLR
15	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	33	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	VBUS/RB6	34	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP12**/SDA3/SDI3/OCM3F/RB7	35	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

FIGURE 3-1: PIC32MM0256GPM064 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

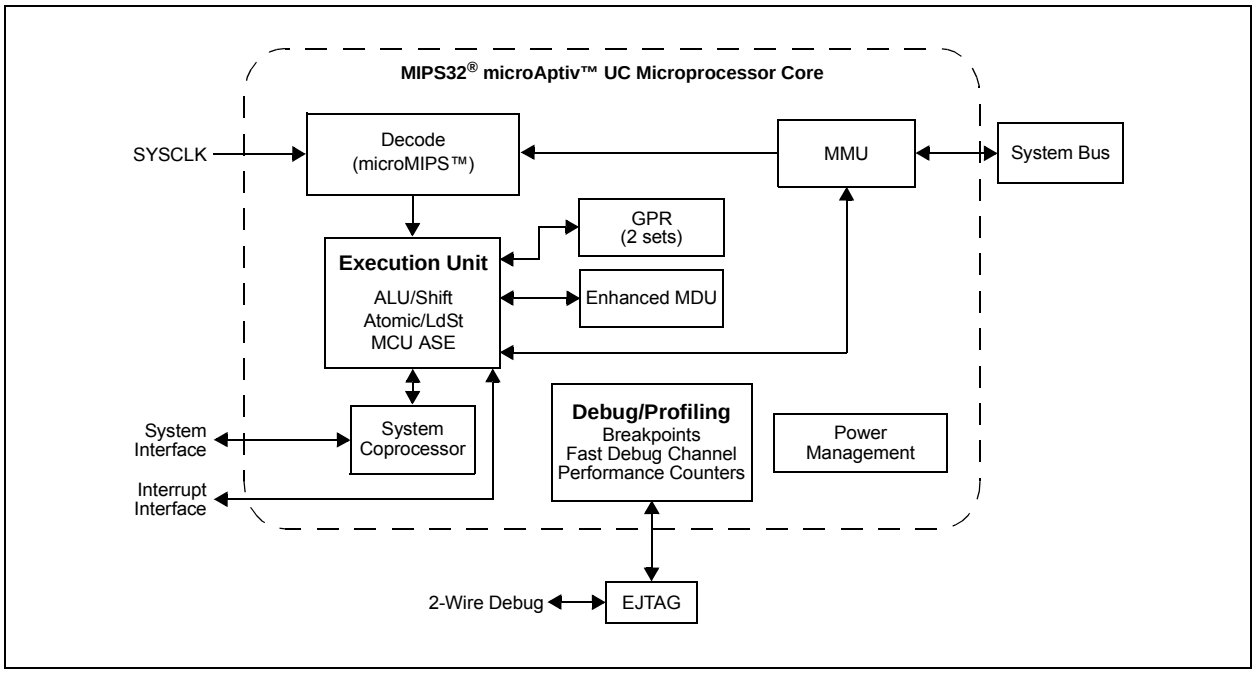
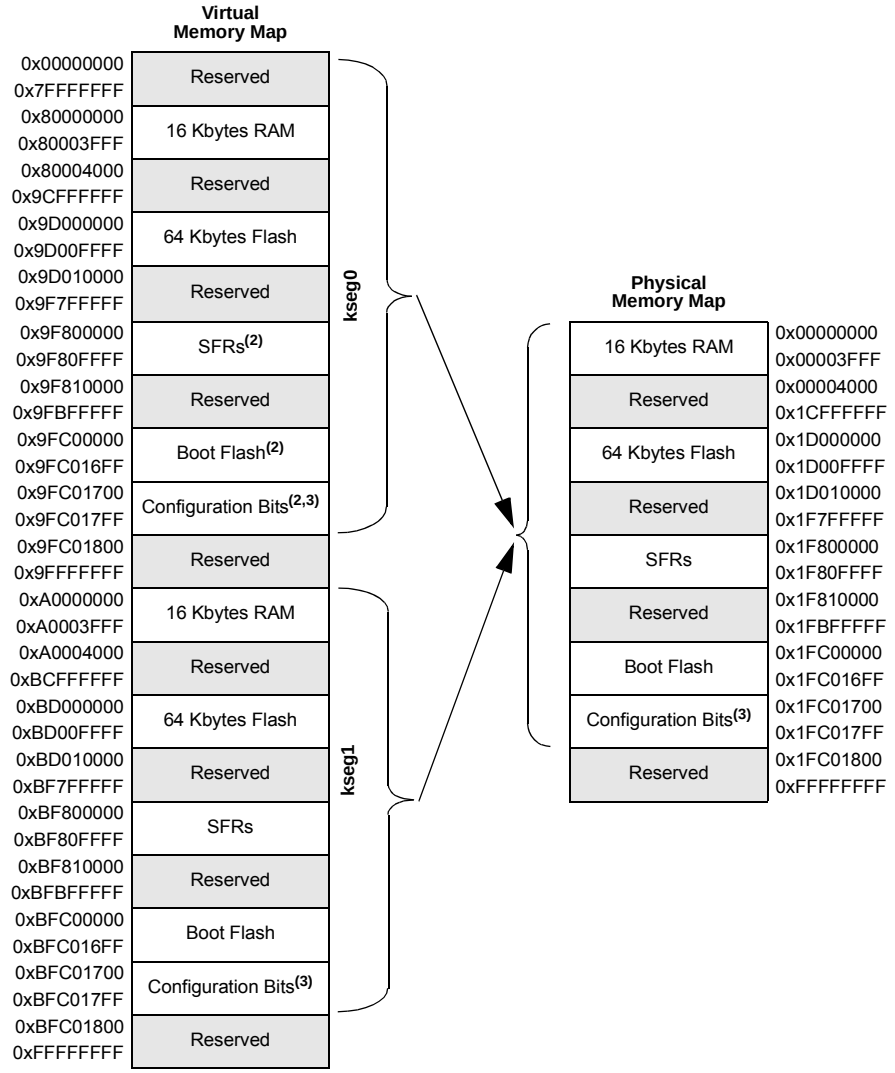


FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority 3 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority 3 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority 2 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority 2 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

NOTES:

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
1 = Device will enter Sleep mode when a WAIT instruction is executed
0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
1 = Enables the Secondary Oscillator
0 = Disables the Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(1)
1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

Note:	Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

REGISTER 9-6: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SRC	LOCK	POL	ORNG	ORPOL
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Self-Tune Enable bit
- 1 = FRC self-tuning is enabled; the TUNx bits are controlled by hardware
- 0 = FRC self-tuning is disabled; the TUNx bits are readable and writable

bit 14 **Reserved:** Used by debugger

bit 13 **SIDL:** FRC Self-Tune Stop in Idle bit
- 1 = Self-tuning stops during Idle mode
- 0 = Self-tuning continues during Idle mode

bit 12 **SRC:** FRC Self-Tune Reference Clock Source bit
- 1 = The USB host clock is used to tune the FRC
- 0 = The 32.768 kHz SOSC clock is used to tune the FRC

bit 11 **LOCK:** FRC Self-Tune Lock Status bit
- 1 = FRC accuracy is currently within ±0.2% of the SRC reference accuracy
- 0 = FRC accuracy may not be within ±0.2% of the SRC reference accuracy

bit 10 **POL:** FRC Self-Tune Lock Interrupt Polarity bit
- 1 = A self-tune lock interrupt is generated when LOCK is '0'
- 0 = A self-tune lock interrupt is generated when LOCK is '1'

bit 9 **ORNG:** FRC Self-Tune Out of Range Status bit
- 1 = SRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
- 0 = SRC reference clock is within the tunable range; tuning is performed

bit 8 **ORPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit
- 1 = A self-tune out of range interrupt is generated when STOR is '0'
- 0 = A self-tune out of range interrupt is generated when STOR is '1'

bit 7-6 **Unimplemented:** Read as '0'

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

TABLE 18-1: USB OTG REGISTER MAP

Virtual Address (BF88_ #)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8440	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
8450	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
8460	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
8470	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
8480	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
8600	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
8610	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
8620	U1EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
8630	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
8640	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>(4)				DIR	PPBI	—	—	0000
8650	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE(4)	SE0(4)	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
8660	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

REGISTER 20-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC V_{R+}	ADC V_{R-}
000	AV_{DD}	AV_{SS}
001	AV_{DD}	External V_{REF-} Pin
010	External V_{REF+} Pin	AV_{SS}
011	External V_{REF+} Pin	External V_{REF-} Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ SHA Input for Input Multiplexer Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1 (ADC buffers split into 2 x 11-word buffers).
1 = ADC is currently filling Buffers 11-21, user should access data in 0-10
0 = ADC is currently filling Buffers 0-10, user should access data in 11-21

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 11-word buffers, ADC1BUF(0...10), ADC1BUF(11...21)
0 = Buffer configured as one 22-word buffer, ADC1BUF(0...21)

bit 0 **Unimplemented:** Read as '0'

21.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCON
- CLCxSEL
- CLCxGLS

The CLCx Control register (CLCxCON) is used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Source Select register (CLCxSEL) allows the user to select up to 4 data input sources using the 4 data input selection multiplexers. Each multiplexer has a list of 8 data sources available.

The CLCx Gate Logic Select register (CLCxGLS) allows the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these 8 signals are enabled, ORed together by the logic cell input gates.

REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = SCCP4 OCMP compare match event
101 = SCCP4 OCM4 output
100 = UART1 RX in
011 = SPI1 SDO1 out
010 = CMP2 out
001 = CLC1 out
000 = CLCINA I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = SCCP4 OCMP compare match event
101 = SCCP4 OCM4 output
100 = UART2 RX in
011 = SPI2 SDO2 out
010 = CMP2 out
001 = CLC2 out
000 = CLCINA I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = SCCP6 OCMP compare match event
101 = SCCP6 OCM6A output
100 = UART3 RX in
011 = SPI3 SDO3 out
010 = CMP2 out
001 = CLC3 out
000 = CLCINA I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = SCCP6 OCMP compare match event
101 = SCCP6 OCM2A output
100 = Reserved
011 = Reserved
010 = CMP2 out
001 = CLC4 out
000 = CLCINA I/O pin

bit 3 **Unimplemented:** Read as '0'

26.9 Configuration Word Registers

TABLE 26-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits															
			31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	FVBUSIO	FUSBIDIO	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ALTI2C	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

REGISTER 26-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	—	—	—	—	BMXERRDIS	—	BMXARB<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-P	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **BMXERRDIS:** Bus Matrix (BMX) Exception Error Disable bit
1 = Disables BMX error exception generation(1)
0 = Enables BMX error exception generation

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **BMXARB<1:0>:** Bus Matrix Arbitration Mode Select bits
11 = Reserved
10 = Mode 2 – Round Robin
01 = Mode 1 – Fixed with CPU as the lowest priority
00 = Mode 0 – Fixed with CPU as the highest priority

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits
11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit
1 = Enables 4-wire JTAG
0 = Disables 4-wire JTAG

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Maintain as '1'

Note 1: An exception is not generated when an unimplemented address is accessed. The returned value on a read operation of unimplemented memory is 0x00000000.

TABLE 26-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

28.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

28.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

29.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC32MM0256GPM064 family AC characteristics and timing parameters.

TABLE 29-16: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C Operating voltage VDD range as described in **Section 29.1 "DC Characteristics"**.

FIGURE 29-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

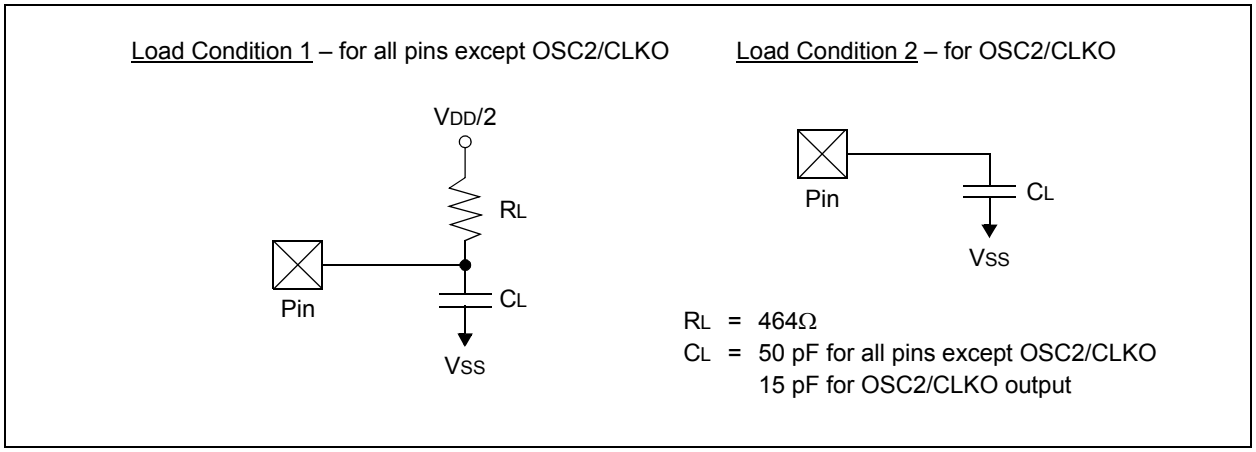


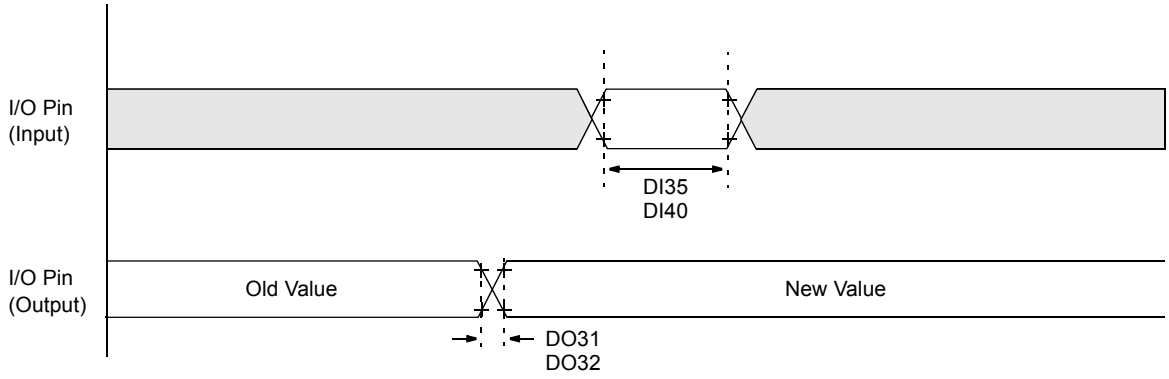
TABLE 29-17: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO50	COSCO	OSC2/CLKO Pin	—	—	TBD	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	CIO	All I/O Pins and OSC2	—	—	TBD	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	TBD	pF	In I^2C mode

Legend: TBD = To Be Determined

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-4: CLKO AND I/O TIMING CHARACTERISTICS



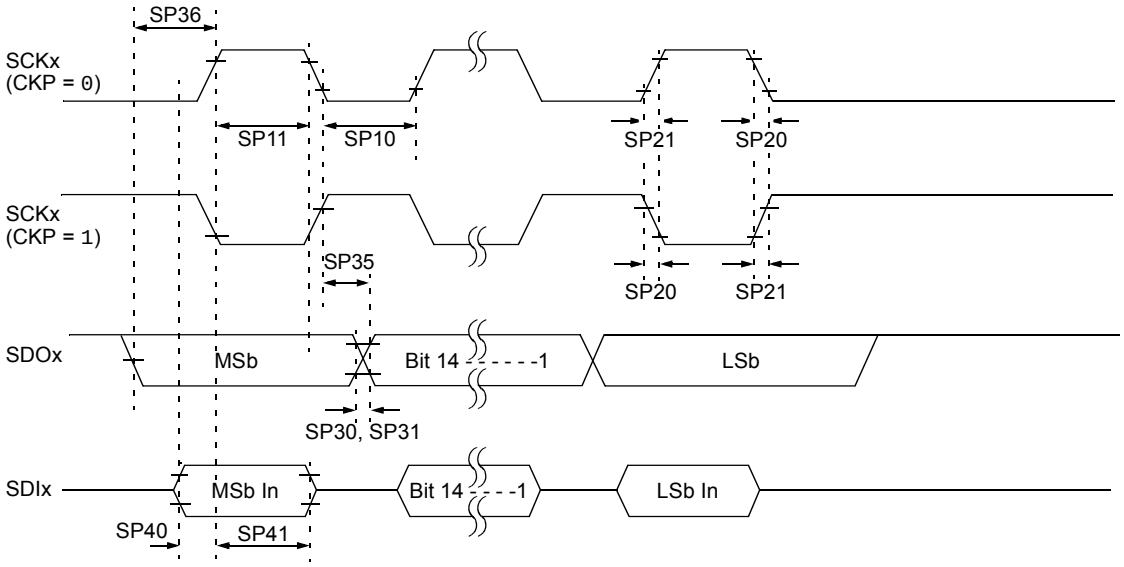
Note: Refer to Figure 29-2 for load conditions.

TABLE 29-22: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	TCY	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	TCY	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 29-10: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	Tsck/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	Tsck/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.0V
			—	—	10	ns	VDD < 2.0V
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.0V
			10	—	—	ns	VDD < 2.0V
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.0V
			10	—	—	ns	VDD < 2.0V

Note 1: These parameters are characterized but not tested in manufacturing.

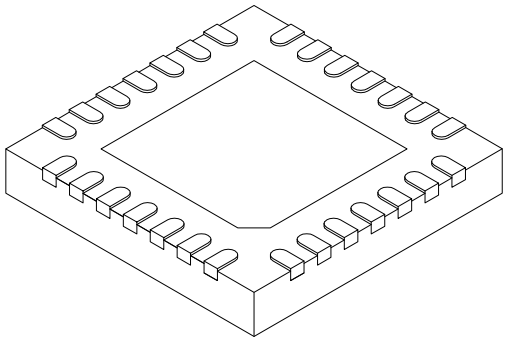
2: Data in the "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 10 pF load on all SPIx pins.

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

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