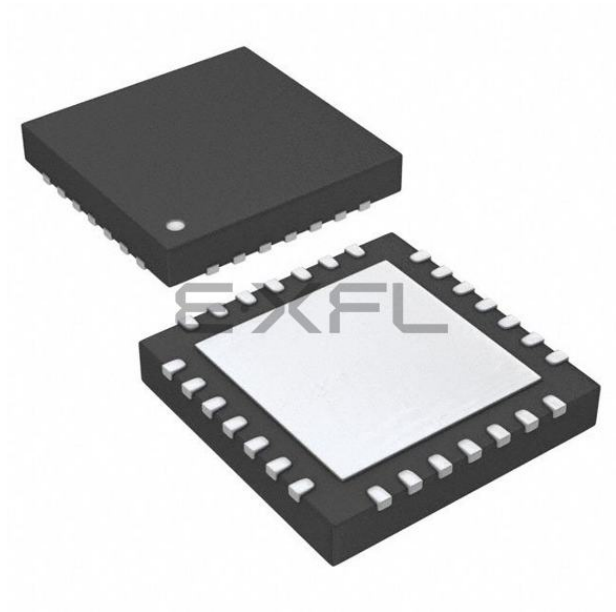
Microchip Technology - PIC32MM0256GPM028-I/ML Datasheet



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Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm028-i-ml

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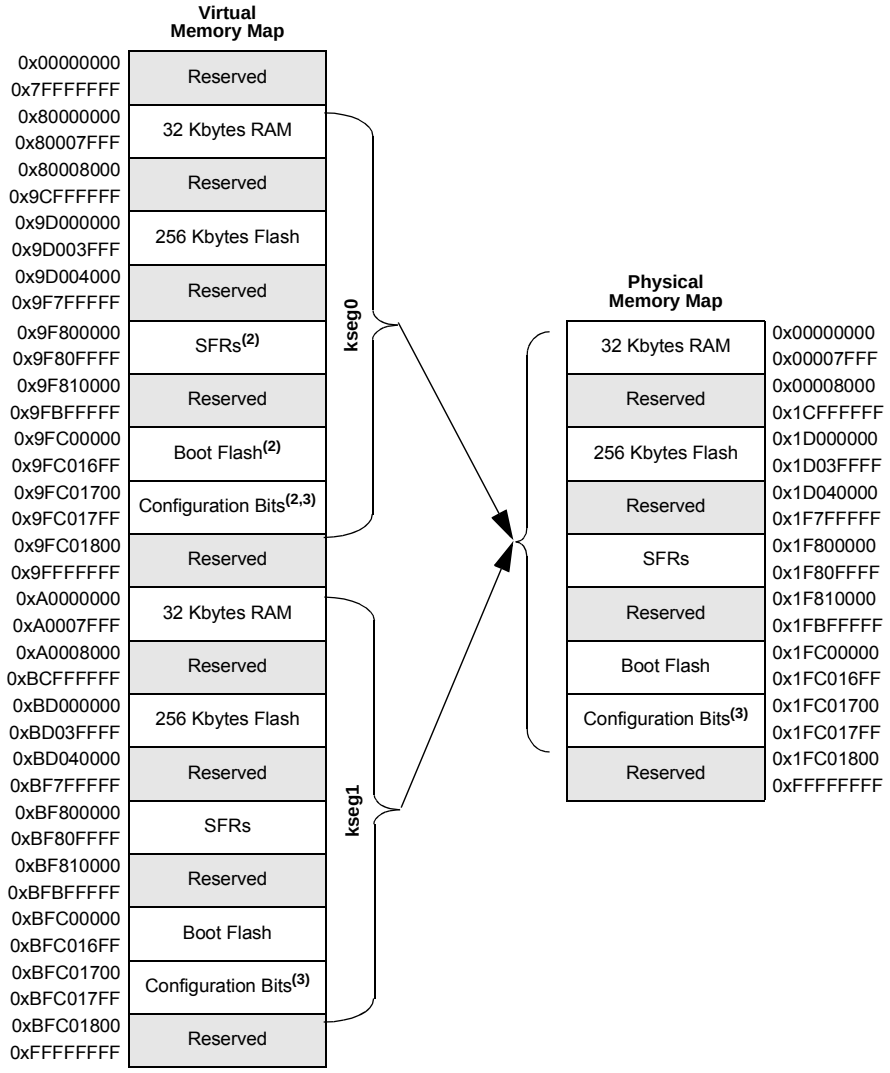
FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

5.2 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2930	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	r	—	—	—	—	—	—	—	NVMOP<3:0>				0000
2940	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
2950	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
2960	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
2970	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
2980	NVMSRCADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
2990	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
29A0	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BWPULOCK	—	—	—	—	BWP2	BWP1	BWP0	—	—	—	—	—	—	—	—	8700

Legend: — = unimplemented, read as '0'; r = Reserved bit. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

REGISTER 5-4: NVMDATAx: FLASH DATA x REGISTER (x = 0-1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATAx<31:0>:** Flash Data x bits

Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1, HS	R/W-1, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	U-0
	—	—	—	—	—	—	CMR	—
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR(1)	SWR(1)	—	WDTO(1)	SLEEP(1)	IDLE(1,2)	BOR(1)	POR(1)

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PORIO:** VDD POR Flag bit
Set by hardware at detection of a VDD POR event.
1 = A Power-on Reset has occurred due to VDD voltage
0 = A Power-on Reset has not occurred due to VDD voltage

bit 30 **PORCORE:** Core Voltage POR Flag bit
Set by hardware at detection of a core POR event.
1 = A Power-on Reset has occurred due to core voltage
0 = A Power-on Reset has not occurred due to core voltage

bit 29-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary Configuration registers
0 = No error occurred during a read of the Primary Configuration registers

bit 26 **BCFGFAIL:** Primary/Alternate Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary and Alternate Configuration registers
0 = No error occurred during a read of the Primary and Alternate Configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit(1)
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit(1)
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit(1)
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: User software must clear these bits to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep.

7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS61108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0256GPM064 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The PIC32MM0256GPM064 family device interrupt module includes the following features:

- Single Vector or Multivector Mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for Each Vector
- Four User-Selectable Subpriority Levels within Each Priority
- One Shadow Register Set that can be Used for Any Priority Level, Eliminating Software Context Switch and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors' Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

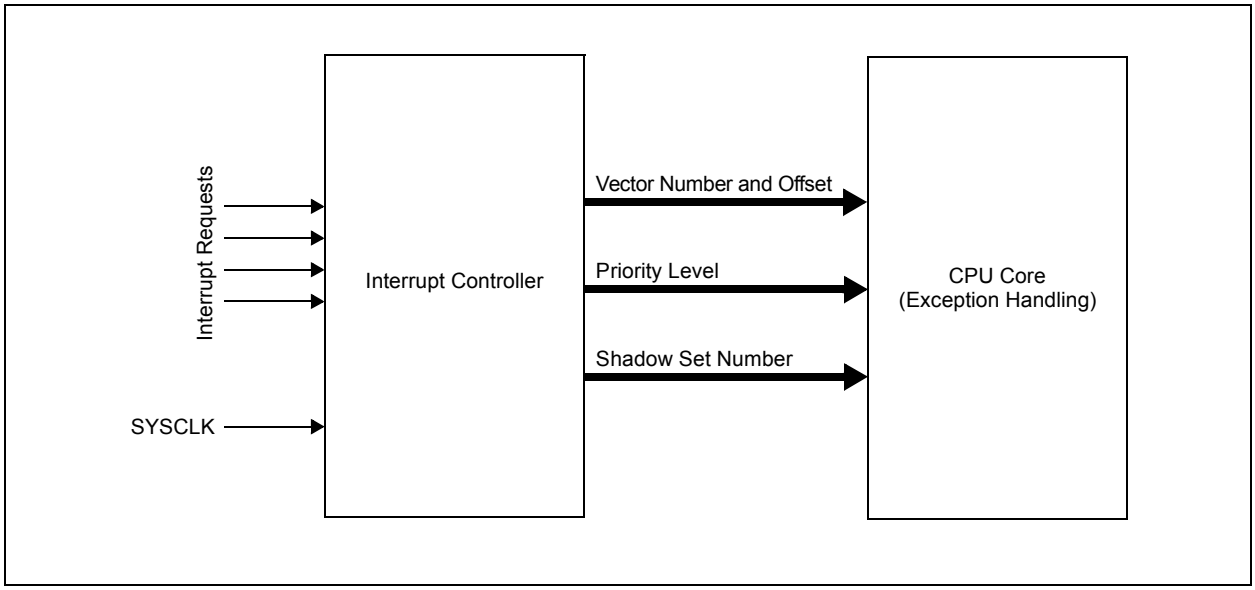


TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
RESERVED		26	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	No
RESERVED		27	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
RESERVED		28	IFS0<28>	IEC0<28>	IPC7<4:2>	IPC7<1:0>	No
USB	_USB_VECTOR	29	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	No
RESERVED		30	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	No
RESERVED		31	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Real-Time Clock Alarm	_RTCC_VECTOR	32	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
ADC Conversion	_ADC_VECTOR	33	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	No
RESERVED		34	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	No
RESERVED		35	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
High/Low-Voltage Detect	_HLVD_VECTOR	36	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	Yes
Logic Cell 1	_CLC1_VECTOR	37	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	No
Logic Cell 2	_CLC2_VECTOR	38	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	No
Logic Cell 3	_CLC3_VECTOR	39	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
Logic Cell 4	_CLC4_VECTOR	40	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
SPI1 Error	_SPI1_ERR_VECTOR	41	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
SPI1 Transmission	_SPI1_TX_VECTOR	42	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
SPI1 Reception	_SPI1_RX_VECTOR	43	IFS1<11>	IEC1<11>	IPC10<28:26>	IPC10<25:24>	Yes
SPI2 Error	_SPI2_ERR_VECTOR	44	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
SPI2 Transmission	_SPI2_TX_VECTOR	45	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
SPI2 Reception	_SPI2_RX_VECTOR	46	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
SPI3 Error	_SPI3_ERR_VECTOR	47	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
SPI3 Transmission	_SPI3_TX_VECTOR	48	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
SPI3 Reception	_SPI3_RX_VECTOR	49	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
RESERVED		50	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	No
RESERVED		51	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	No
RESERVED		52	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	No
UART1 Reception	_UART1_RX_VECTOR	53	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
UART1 Transmission	_UART1_TX_VECTOR	54	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
UART1 Error	_UART1_ERR_VECTOR	55	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F100	IPC4	31:16	—	—	—	T3IP<2:0>			T3IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
		15:0	—	—	—	T1IP<2:0>			T1IS<1:0>		—	—	—	—	—	—	—	—	0000
F110	IPC5	31:16	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F120	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CMP3IP<2:0>			CMP3IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
F130	IPC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	—	—	—	—	—	0000
F140	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
F150	IPC9	31:16	—	—	—	CLC3IP<2:0>			CLC3IS<1:0>		—	—	—	CLC2IP<2:0>			CLC2IS<1:0>		0000
		15:0	—	—	—	CLC1IP<2:0>			CLC1IS<1:0>		—	—	—	LVDIP<2:0>			LVDIS<1:0>		0000
F160	IPC10	31:16	—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	CLC4IP<2:0>			CLC4IS<1:0>		0000
F170	IPC11	31:16	—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		0000
		15:0	—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
F180	IPC12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
F190	IPC13	31:16	—	—	—	U1EIP<2:0>			U1EIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	—	—	—	—	—	0000
F1A0	IPC14	31:16	—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
		15:0	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
F1B0	IPC15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>		—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		0000
F1C0	IPC16	31:16	—	—	—	I2C1BCIP<2:0>			I2C1BCIS<1:0>		—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		0000
		15:0	—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		—	—	—	—	—	—	—	—	0000
F1D0	IPC17	31:16	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>		—	—	—	I2C2BCIP<2:0>			I2C2BCIS<1:0>		0000
		15:0	—	—	—	I2C2MIP<2:0>			I2C2MIS<1:0>		—	—	—	I2C2SIP<2:0>			I2C2SIS<1:0>		0000
F1E0	IPC18	31:16	—	—	—	CCT1IP<2:0>			CCT1IS<1:0>		—	—	—	CCP1IP<2:0>			CCP1IS<1:0>		0000
		15:0	—	—	—	I2C3BCIP<2:0>			I2C3BCIS<1:0>		—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
F1F0	IPC19	31:16	—	—	—	CCT3IP<2:0>			CCT3IS<1:0>		—	—	—	CCP3IP<2:0>			CCP3IS<1:0>		0000
		15:0	—	—	—	CCT2IP<2:0>			CCT2IS<1:0>		—	—	—	CCP2IP<2:0>			CCP2IS<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	SRIPL<2:0>(1)		
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SIRQ<7:0>							

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level for Single Vector Mode bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits

11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

9.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0256GPM064 family oscillator system has the following modules and features:

- A Total of Five External and Internal Oscillator Options as Clock Sources
- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- On-Chip User-Selectable Divisor Postscaler on Select Oscillator Sources
- Software-Controllable Switching between Various Clock Sources
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output

A block diagram of the oscillator system is provided in Figure 9-1.

9.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0256GPM064 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

9.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in FOSC must be programmed to '0'. (Refer to **Section 26.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSC<2:0> control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

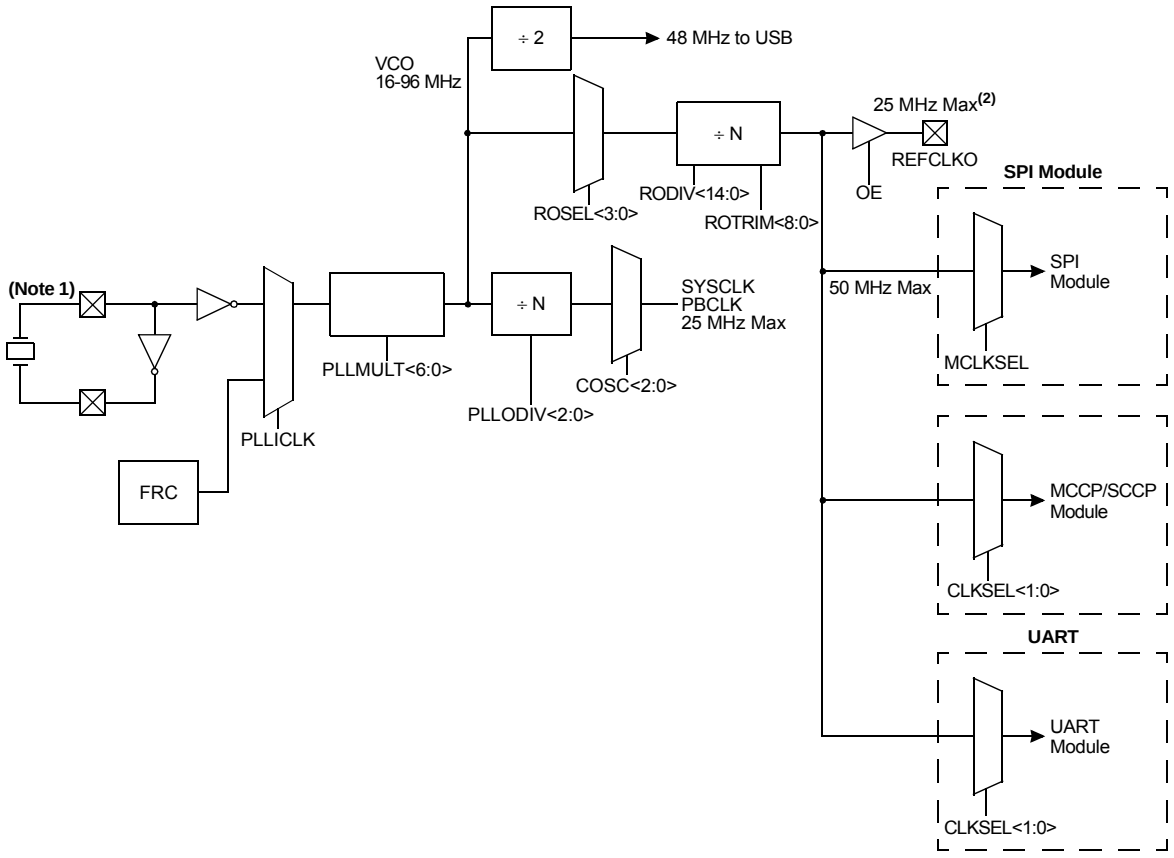
The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register.
3. Write the appropriate value to the NOSC<2:0> bits (OSCCON<10:8>) for the new oscillator source.
4. Set the OSWEN bit to initiate the oscillator switch.

FIGURE 9-2: REFERENCE OSCILLATOR



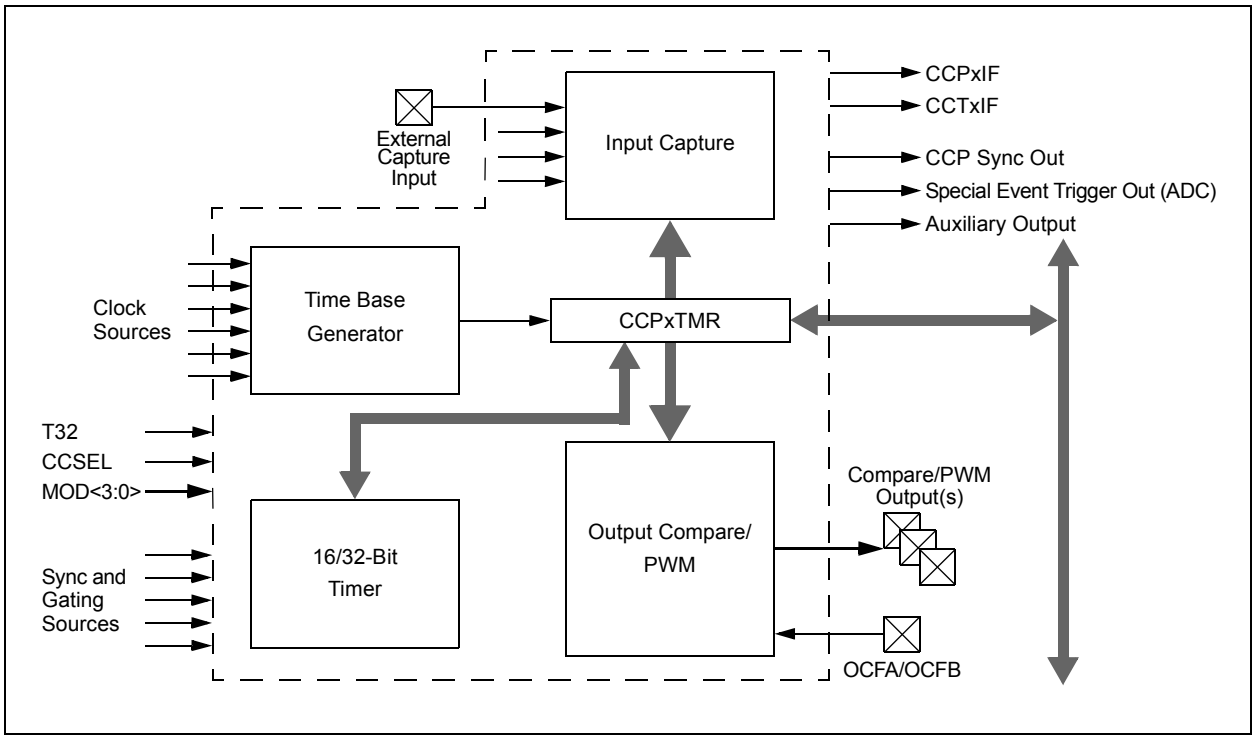
Note 1: Support circuitry for crystal is not shown.
2: In Retention mode, the maximum peripheral output frequency to an I/O pin must be limited to 33 kHz or less.

TABLE 10-3: REMAPPABLE INPUT SOURCES PIN ASSIGNMENTS(1)

Value	RPn Pins	Pin Assignment
00001	RP1	RA0 Pin
00010	RP2	RA1 Pin
00011	RP3	RA2 Pin
00100	RP4	RA3 Pin
00101	RP5	RA4 Pin
00110	RP6	RB0 Pin
00111	RP7	RB1 Pin
01000	RP8	RB2 Pin
01001	RP9	RB3 Pin
01010	RP10	RB4 Pin
01011	RP11	RB5 Pin
01100	RP12	RB7 Pin
01101	RP13	RB8 Pin
01110	RP14	RB9 Pin
01111	RP15	RB13 Pin
10000	RP16	RB14 Pin
10001	RP17	RB15 Pin
10010	RP18	RC9 Pin
10011	RP19	RC2 Pin
10100	RP20	RC7 Pin
10101	RP21	RA7 Pin
10110	RP22	RA10 Pin
10111	RP23	RC6 Pin
11000	RP24	RA9 Pin
11001-11111	Reserved	

Note 1: All RPx pins are not available on all packages.

FIGURE 14-1: MCCP/SCCP CONCEPTUAL BLOCK DIAGRAM



14.2 Registers

Each MCCP/SCCP module has up to seven control and status registers:

- CCPxCON1 (Register 14-1) controls many of the features common to all modes, including input clock selection, time base prescaling, timer synchronization, Trigger mode operations and postscaler selection for all modes. The module is also enabled and the operational mode is selected from this register.
- CCPxCON2 (Register 14-2) controls auto-shutdown and restart operation, primarily for PWM operations, and also configures other input capture and output compare features, and configures auxiliary output operation.
- CCPxCON3 (Register 14-3) controls multiple output PWM dead time, controls the output of the output compare and PWM modes, and configures the PWM Output mode for the MCCP modules.
- CCPxSTAT (Register 14-4) contains read-only status bits showing the state of module operations.

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMR is the 32-Bit Timer/Counter register
- CCPxPR is the 32-Bit Timer Period register
- CCPxR is the 32-bit primary data buffer for output compare operations
- CCPxBUF(H/L) is the 32-Bit Buffer register pair, which is used in input capture FIFO operations

REGISTER 18-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

REGISTER 20-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	EXTSAM	—	SAMC<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from the Fast RC (FRC) oscillator
0 = Clock derived from the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS4<2:0>			—	DS3<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS2<2:0>			—	DS1<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = MCCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = MCCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

REGISTER 22-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1, 2 AND 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	ON	COE	CPOL	—	—	—	CEVT	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Enable bit
- 1 = Comparator is enabled
- 0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is present on the CxOUT pin
- 0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
- 1 = Comparator output is inverted
- 0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
- 1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
- 0 = Comparator event has not occurred

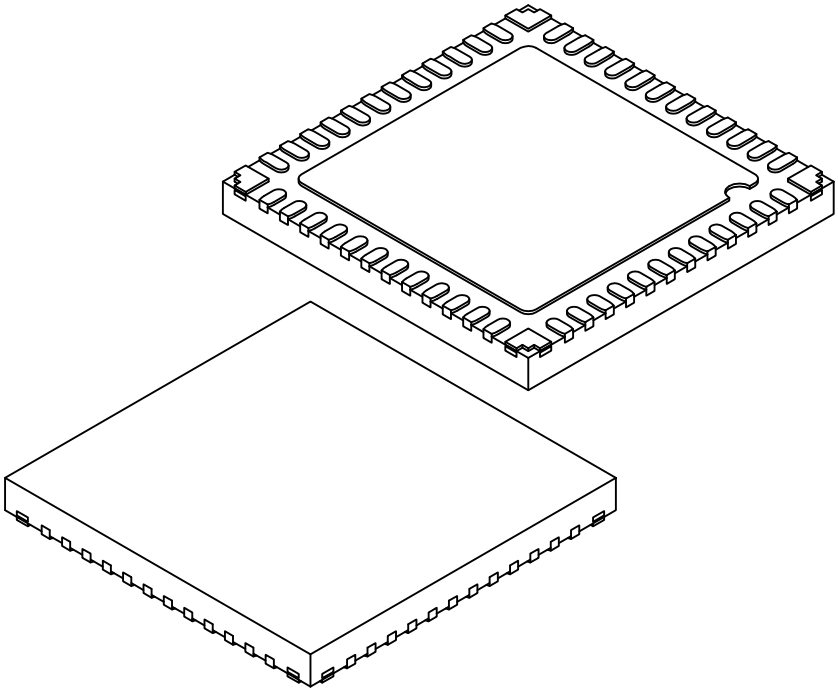
bit 8 **COUT:** Comparator Output bit

When CPOL = 0:
- 1 = $V_{IN+} > V_{IN-}$
- 0 = $V_{IN+} < V_{IN-}$

When CPOL = 1:
- 1 = $V_{IN+} < V_{IN-}$
- 0 = $V_{IN+} > V_{IN-}$

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.15 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.50	4.60	4.70
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.50	4.60	4.70
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1		0.45 REF	
Corner Anchor Pad, Metal-free Zone	b2		0.23 REF	
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-442A-M4 Sheet 2 of 2

NOTES: