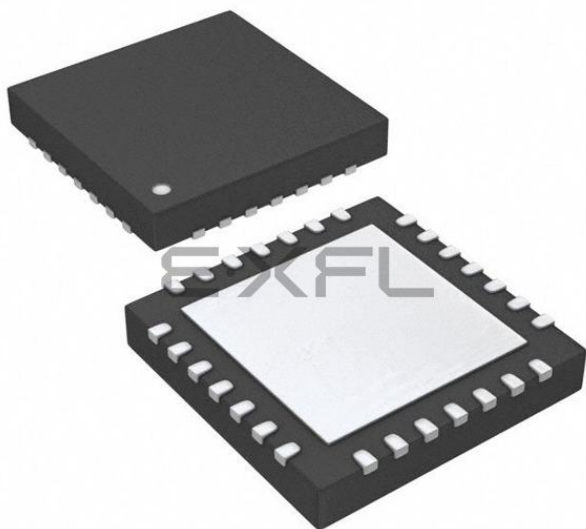




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm028t-i-ml

PIC32MM0256GPM064 FAMILY

Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
 - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)

- 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
- Sleep mode operation
- Low-voltage boost for input
- Band gap reference input feature
- Windowed threshold compare feature
- Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I ² C	USB	Packages
							Dedicated 16-Bit Timers	UART ⁽¹⁾ /LIN/J2602	MCCP ⁽⁴⁾	SCCP ⁽³⁾	CLC	SPI ⁽²⁾ /I ² S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

- Note**
- 1: UART1 has assigned pins. UART2 and UART3 are remappable.
 - 2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.
 - 3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.
 - 4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

PIC32MM0256GPM064 FAMILY

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RA0	2	27	33	36	21	11	I/O	ST/DIG	PORTA digital I/Os
RA1	3	28	34	37	22	12	I/O	ST/DIG	
RA2	9	6	7	7	32	25	I/O	ST/DIG	
RA3	10	7	8	8	33	26	I/O	ST/DIG	
RA4	12	9	10	10	36	29	I/O	ST/DIG	
RA5	—	—	—	—	—	54	I/O	ST/DIG	
RA6	—	—	—	—	20	10	I/O	ST/DIG	
RA7	—	—	—	—	14	1	I/O	ST/DIG	
RA8	—	—	—	—	34	27	I/O	ST/DIG	
RA9	—	—	11	11	37	30	I/O	ST/DIG	
RA10	—	—	—	—	13	64	I/O	ST/DIG	
RA11	—	—	—	—	—	8	I/O	ST/DIG	
RA12	—	—	—	—	—	7	I/O	ST/DIG	
RA13	—	—	—	—	—	6	I/O	ST/DIG	
RA14	—	—	—	—	—	59	I/O	ST/DIG	
RA15	—	—	—	—	8	58	I/O	ST/DIG	
RB0	4	1	35	38	23	13	I/O	ST/DIG	PORTB digital I/Os
RB1	5	2	36	39	24	14	I/O	ST/DIG	
RB2	6	3	1	1	25	15	I/O	ST/DIG	
RB3	7	4	2	2	26	16	I/O	ST/DIG	
RB4	11	8	9	9	35	28	I/O	ST/DIG	
RB5	14	11	15	15	45	43	I/O	ST/DIG	
RB6	15	12	16	16	46	44	I/O	ST/DIG	
RB7	16	13	17	17	47	46	I/O	ST/DIG	
RB8	17	14	18	18	48	48	I/O	ST/DIG	
RB9	18	15	19	20	1	49	I/O	ST/DIG	
RB10	21	18	24	27	9	60	I/O	ST/DIG	
RB11	22	19	25	28	10	61	I/O	ST/DIG	
RB13	24	21	27	30	12	63	I/O	ST/DIG	
RB14	25	22	28	31	15	2	I/O	ST/DIG	
RB15	26	23	29	32	16	3	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer
I²C = I²C/SMBus input buffer

DIG = Digital input/output
ANA = Analog level input/output

P = Power

PIC32MM0256GPM064 FAMILY

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

PIC32MM0256GPM064 FAMILY

NOTES:

9.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. “Oscillators with DCO”** (DS60001329) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0256GPM064 family oscillator system has the following modules and features:

- A Total of Five External and Internal Oscillator Options as Clock Sources
- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- On-Chip User-Selectable Divisor Postscaler on Select Oscillator Sources
- Software-Controllable Switching between Various Clock Sources
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output

A block diagram of the oscillator system is provided in Figure 9-1.

9.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0256GPM064 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

9.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switching process.

Note: The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in FOSC must be programmed to '0'. (Refer to **Section 26.1 “Configuration Bits”** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSC<2:0> control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register.
3. Write the appropriate value to the NOSC<2:0> bits (OSCCON<10:8>) for the new oscillator source.
4. Set the OSWEN bit to initiate the oscillator switch.

TABLE 16-1: I2C1, I2C2 AND I2C3 REGISTER MAP (CONTINUED)

Virtual Address (BF80 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1700	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	r	r	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
1710	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
1720	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Register										0000
1730	I2C3MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Mask Register										0000
1740	I2C3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
1750	I2C3TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Transmit Register								0000
1760	I2C3RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000

Legend: — = unimplemented, read as '0'; r = reserved bit. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except I2CxRCV, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

17.1 UART Control Registers

TABLE 17-1: UART1, UART2 AND UART3 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
1800	U1MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
1810	U1STA ⁽¹⁾	31:16	UART1 MASK<7:0>								UART1 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
1820	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART1 Transmit Register								0000
1830	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART1 Receive Register								0000
1840	U1BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler															0000	
1900	U2MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
1910	U2STA ⁽¹⁾	31:16	UART2 MASK<7:0>								UART2 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
1920	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART2 Transmit Register								0000
1930	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART2 Receive Register								0000
1940	U2BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler															0000	
2000	U3MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2010	U3STA ⁽¹⁾	31:16	UART2 MASK<7:0>								UART2 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2020	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART2 Transmit Register								0000
2030	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART2 Receive Register								0000
2040	U3BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler															0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

PIC32MM0256GPM064 FAMILY

REGISTER 19-4: RTCTIME/ALMTIME: RTCC TIME/ALARM REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	HRTEN<2:0>			HRTONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SECTEN<3:0>				SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.

bit 27-24 **HRTONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.

bit 15-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

20.0 12-BIT ADC CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 25. “12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect”** (DS60001359) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

20.1 Introduction

The 12-bit ADC Converter with Threshold Detect includes the following features:

- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 300 ksp/s
- User-Selectable Resolution of 10 or 12 bits
- Up to 24 Analog Inputs (internal and external)
- External Voltage Reference Input Pins

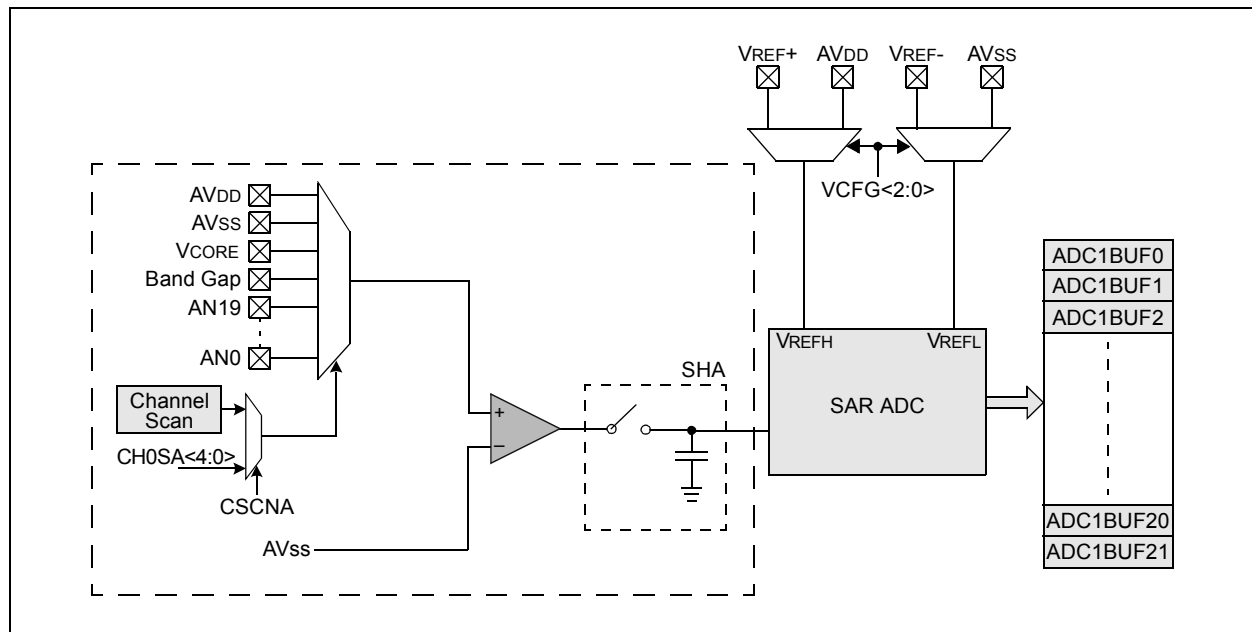
- Unipolar Differential Sample-and-Hold Amplifier (SHA)
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length Configurable Conversion Result Buffer
- Eight Options for Result Alignment and Encoding
- Configurable Interrupt Generation
- Operation during CPU Sleep and Idle modes

Figure 20-1 illustrates a block diagram of the 12-bit ADC. The 12-bit ADC has external analog inputs, AN0 through AN19, and 4 internal analog inputs connected to VDD, VSS, V_{CORE} and band gap. In addition, there are two analog input pins for external voltage reference connections.

The analog inputs are connected through a multiplexer to the SHA. Unipolar differential conversions are possible on all inputs (see Figure 20-1).

The Automatic Input Scan mode sequentially converts multiple analog inputs. A special control register specifies which inputs will be included in the scanning sequence. The 12-bit ADC is connected to a 22-word result buffer. The 12-bit result is converted to one of eight output formats in either 32-bit or 16-bit word widths.

FIGURE 20-1: ADC BLOCK DIAGRAM



REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 2-0 **DS1<2:0>**: Data Selection MUX 1 Signal Selection bits

For CLC1:

111 = SCCP5 OCMP compare match event
110 = M CCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:

111 = SCCP5 OCMP compare match event
110 = M CCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:

111 = SCCP7 OCMP compare match event
110 = M CCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:

111 = SCCP7 OCMP compare match event
110 = M CCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

PIC32MM0256GPM064 FAMILY

NOTES:

PIC32MM0256GPM064 FAMILY

REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

- bit 6-5 **FWDTWINSZ<1:0>**: Watchdog Timer Window Size bits
- 11 = Watchdog Timer window size is 25%
 - 10 = Watchdog Timer window size is 37.5%
 - 01 = Watchdog Timer window size is 50%
 - 00 = Watchdog Timer window size is 75%
- bit 4-0 **SWDTPS<4:0>**: Sleep Mode Watchdog Timer Postscale Select bits
- From 10100 to 11111 = 1:1048576.
- 10011 = 1:524288
 - 10010 = 1:262144
 - 10001 = 1:131072
 - 10000 = 1:65536
 - 01111 = 1:32768
 - 01110 = 1:16384
 - 01101 = 1:8192
 - 01100 = 1:4096
 - 01011 = 1:2048
 - 01010 = 1:1024
 - 01001 = 1:512
 - 01000 = 1:256
 - 00111 = 1:128
 - 00110 = 1:64
 - 00101 = 1:32
 - 00100 = 1:16
 - 00011 = 1:8
 - 00010 = 1:4
 - 00001 = 1:2
 - 00000 = 1:1

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REGISTER 26-10: ANCFG: BAND GAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS, HC	R/W-0, HS, HC	U-0
	—	—	—	—	—	VBGADC	VBGCMP	—

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **VBGADC:** ADC Band Gap Enable bit

1 = ADC band gap is enabled

0 = ADC band gap is disabled

bit 1 **VBGCMP:** Comparator Band Gap Enable bit

1 = Comparator band gap is enabled

0 = Comparator band gap is disabled

bit 0 **Unimplemented:** Read as '0'

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

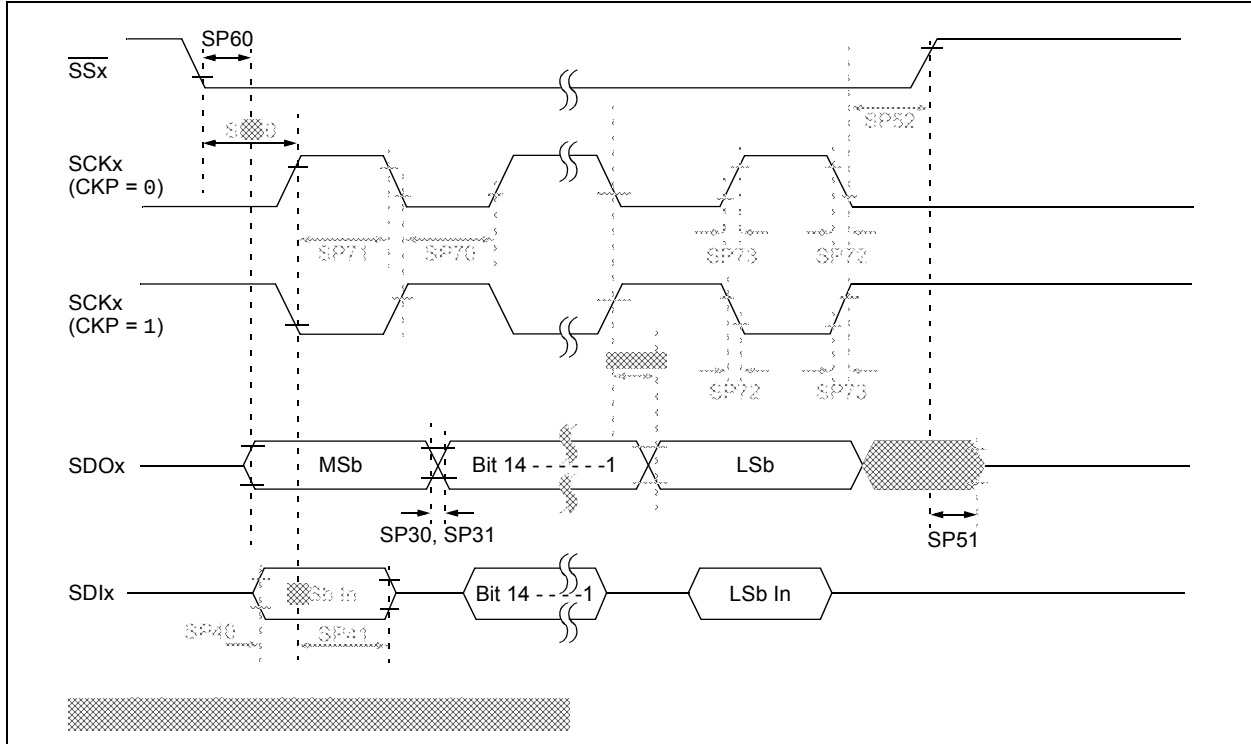
Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

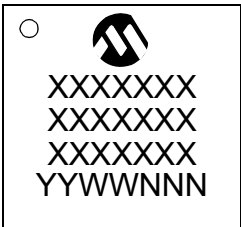
FIGURE 29-12: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



PIC32MM0256GPM064 FAMILY

30.1 Package Marking Information (Continued)

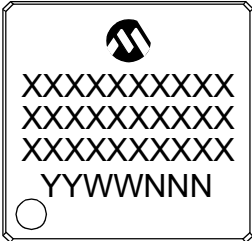
40-Lead UQFN (5x5x0.5 mm)



Example



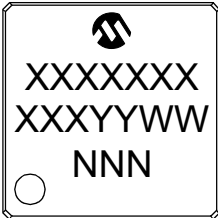
48-Lead UQFN (6x6 mm)



Example



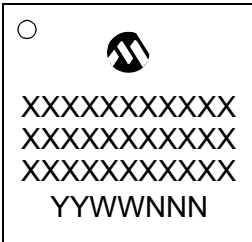
48-Lead TQFP (7x7x1.0 mm)



Example



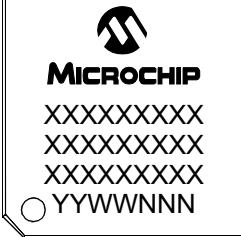
64-Lead QFN (9x9x0.9 mm)



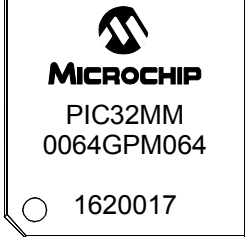
Example



64-Lead TQFP (10x10x1 mm)



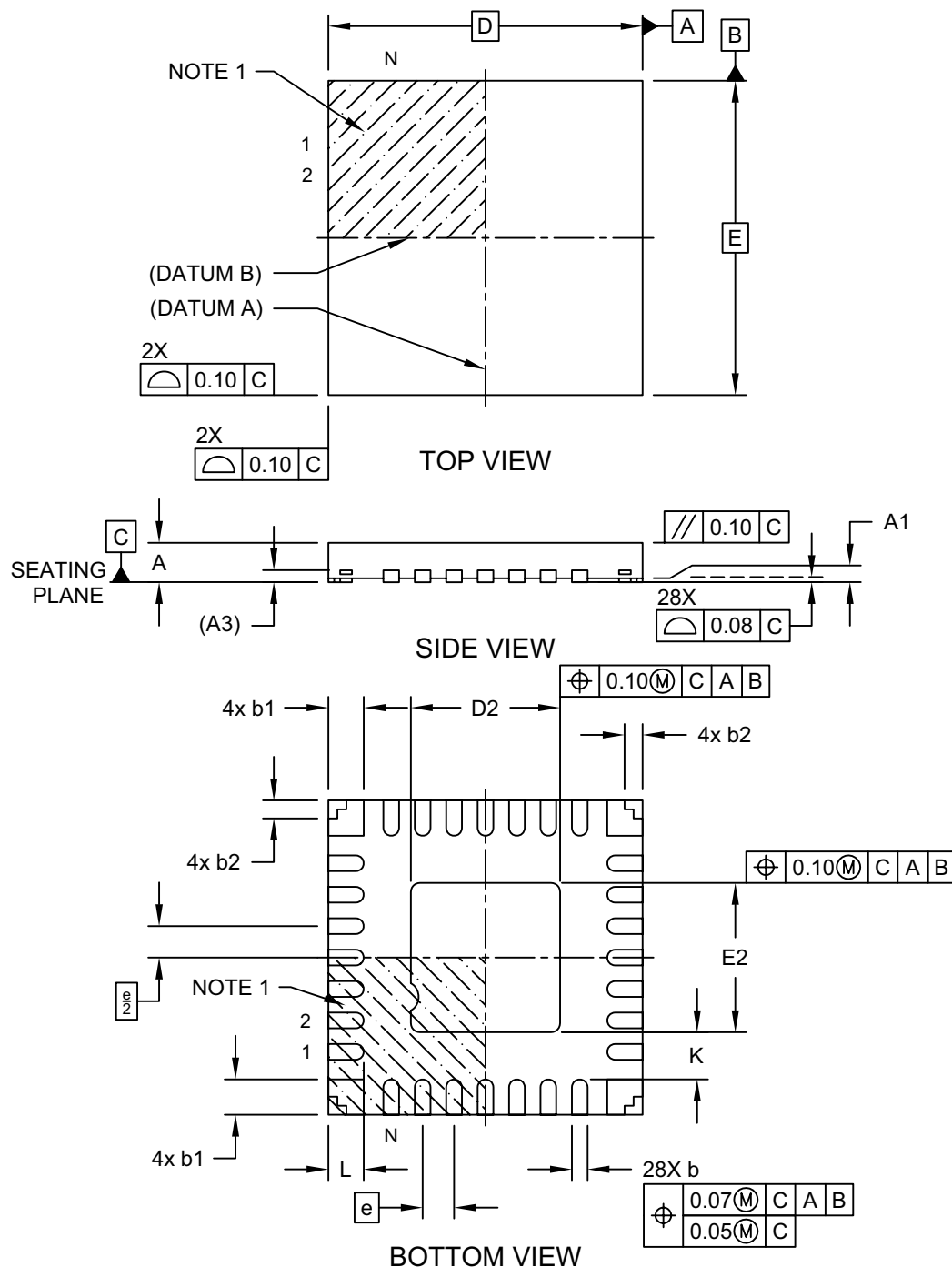
Example



PIC32MM0256GPM064 FAMILY

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

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