Microchip Technology - PIC32MM0256GPM036-I/M2 Datasheet

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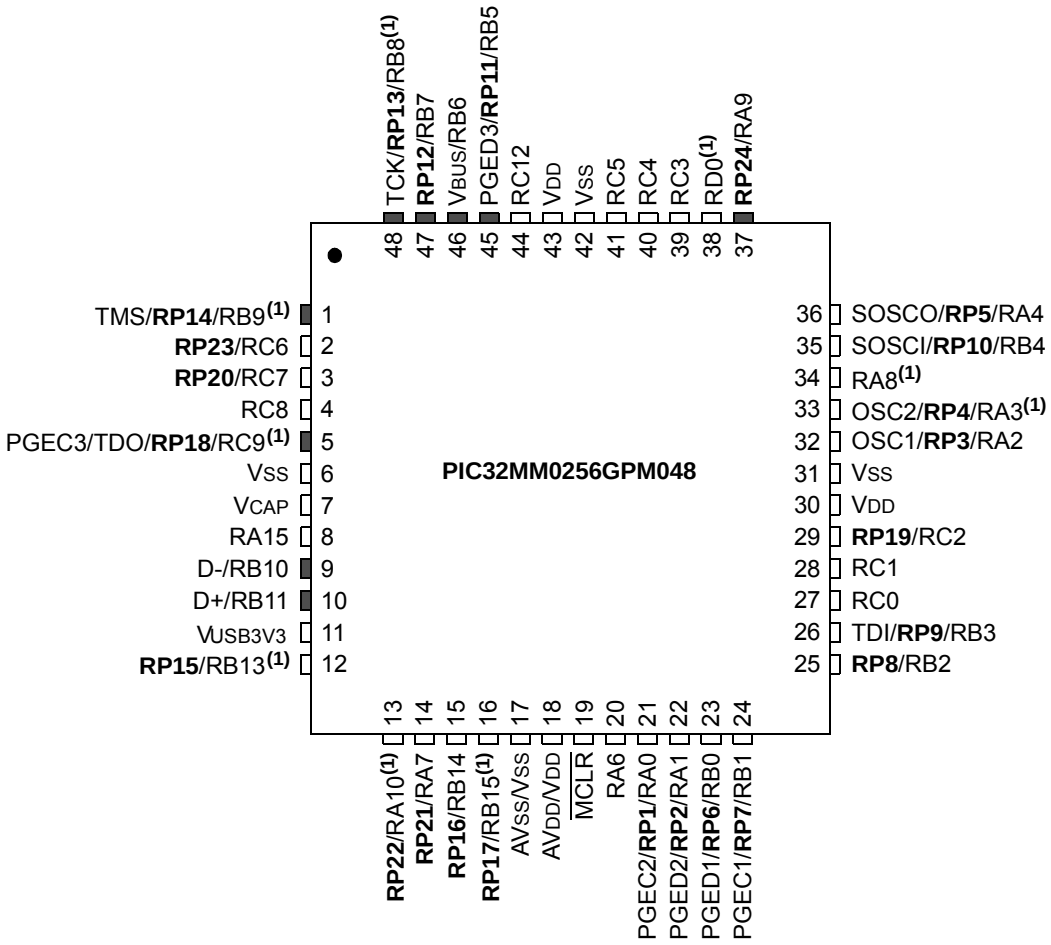
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-SQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm036-i-m2

Pin Diagrams (Continued)

48-Pin UQFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

REGISTER 6-4: PWRCON: POWER CONTROL REGISTER(2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SBOREN	RETEN(1)	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **SBOREN:** BOR Enable bit

Enables the BOR for select BOREN Configuration bit settings.
1 = Writing a '1' to this bit enables the BOR for select BOREN configuration values
0 = Writing a '0' to this bit enables the BOR for select BOREN configuration values

bit 1 **RETEN:** Output Level of the Regulator During Sleep Selection bit(1)

1 = Writing a '1' to this bit will cause the main regulator to be put in a low-power state during Sleep mode(3)
0 = Writing a '0' to this bit will have no effect

bit 0 **VREGS:** Voltage Regulator Standby Enable bit

1 = Voltage regulator will remain active during Sleep mode
0 = Voltage regulator will go into Standby mode during Sleep mode

Note 1: Refer to **Section 25.0 "Power-Saving Features"** for details.
2: The SYSKEY register is used to unlock this register.
3: The RETEN bit in the device configuration must also be set to enable this mode.

TABLE 10-3: REMAPPABLE INPUT SOURCES PIN ASSIGNMENTS(1)

Value	RPn Pins	Pin Assignment
00001	RP1	RA0 Pin
00010	RP2	RA1 Pin
00011	RP3	RA2 Pin
00100	RP4	RA3 Pin
00101	RP5	RA4 Pin
00110	RP6	RB0 Pin
00111	RP7	RB1 Pin
01000	RP8	RB2 Pin
01001	RP9	RB3 Pin
01010	RP10	RB4 Pin
01011	RP11	RB5 Pin
01100	RP12	RB7 Pin
01101	RP13	RB8 Pin
01110	RP14	RB9 Pin
01111	RP15	RB13 Pin
10000	RP16	RB14 Pin
10001	RP17	RB15 Pin
10010	RP18	RC9 Pin
10011	RP19	RC2 Pin
10100	RP20	RC7 Pin
10101	RP21	RA7 Pin
10110	RP22	RA10 Pin
10111	RP23	RC6 Pin
11000	RP24	RA9 Pin
11001-11111	Reserved	

Note 1: All RPx pins are not available on all packages.

13.0 WATCHDOG TIMER (WDT)

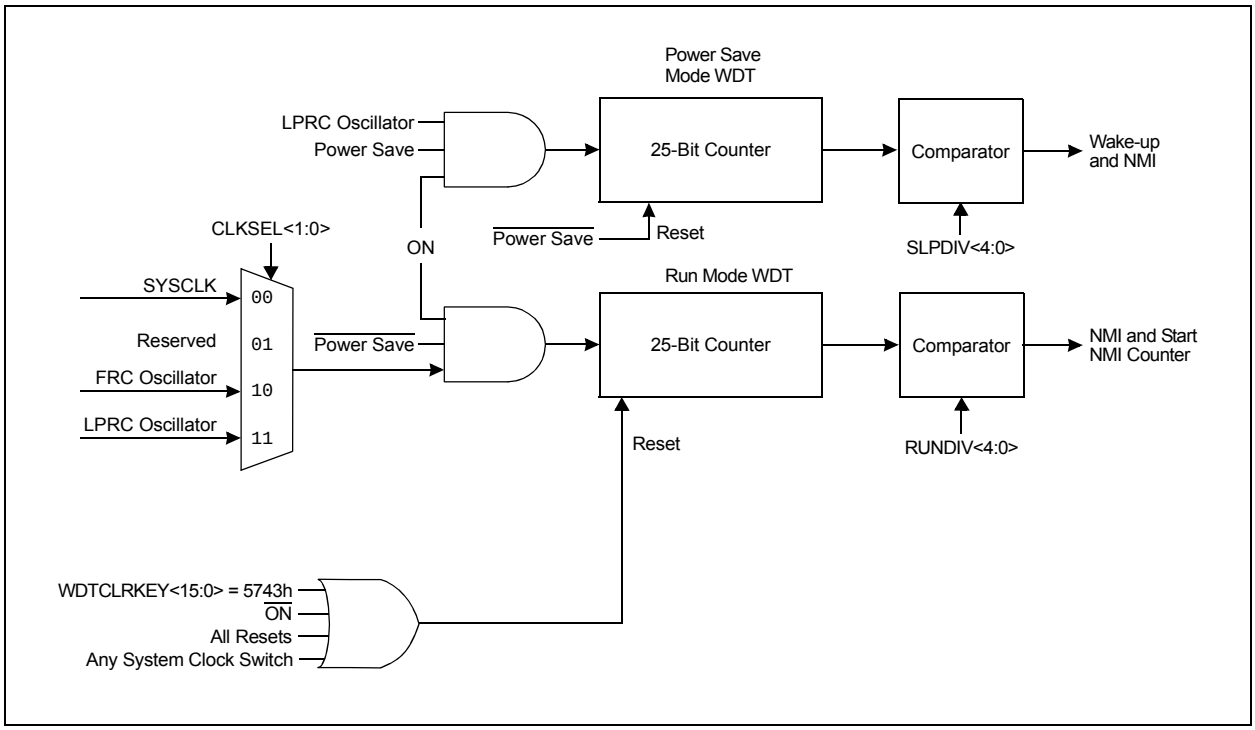
Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 13-1: WATCHDOG TIMER BLOCK DIAGRAM



18.5 Control Registers

REGISTER 18-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to Clear bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = Change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input was detected
- 0 = No change on the session valid input was detected

REGISTER 18-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

REGISTER 19-2: RTCCON2: RTCC CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	PS<1:0>		—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter for the seconds output.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **PS<1:0>:** Prescale Select bits
Sets the prescaler for the seconds output.
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

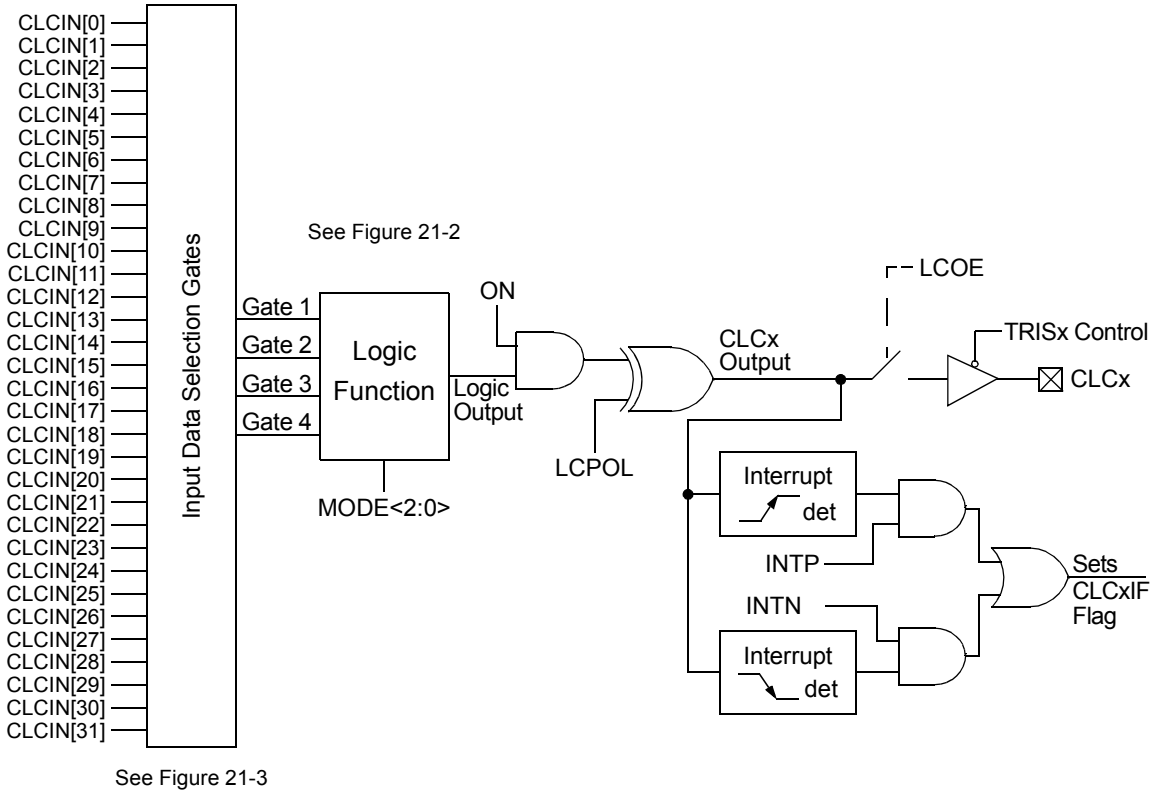
21.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. "Configurable Logic Cell"** (DS60001363) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 21-1 shows an overview of the module. Figure 21-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 21-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCON register.

TABLE 21-1: CLC1, CLC2 AND CLC3 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2480	CLC1CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2490	CLC1SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
24A0	CLC1GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2500	CLC2CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2510	CLC2SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2520	CLC2GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2580	CLC3CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2590	CLC3SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
25A0	CLC3GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2600	CLC4CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2610	CLC4SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2620	CLC4GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

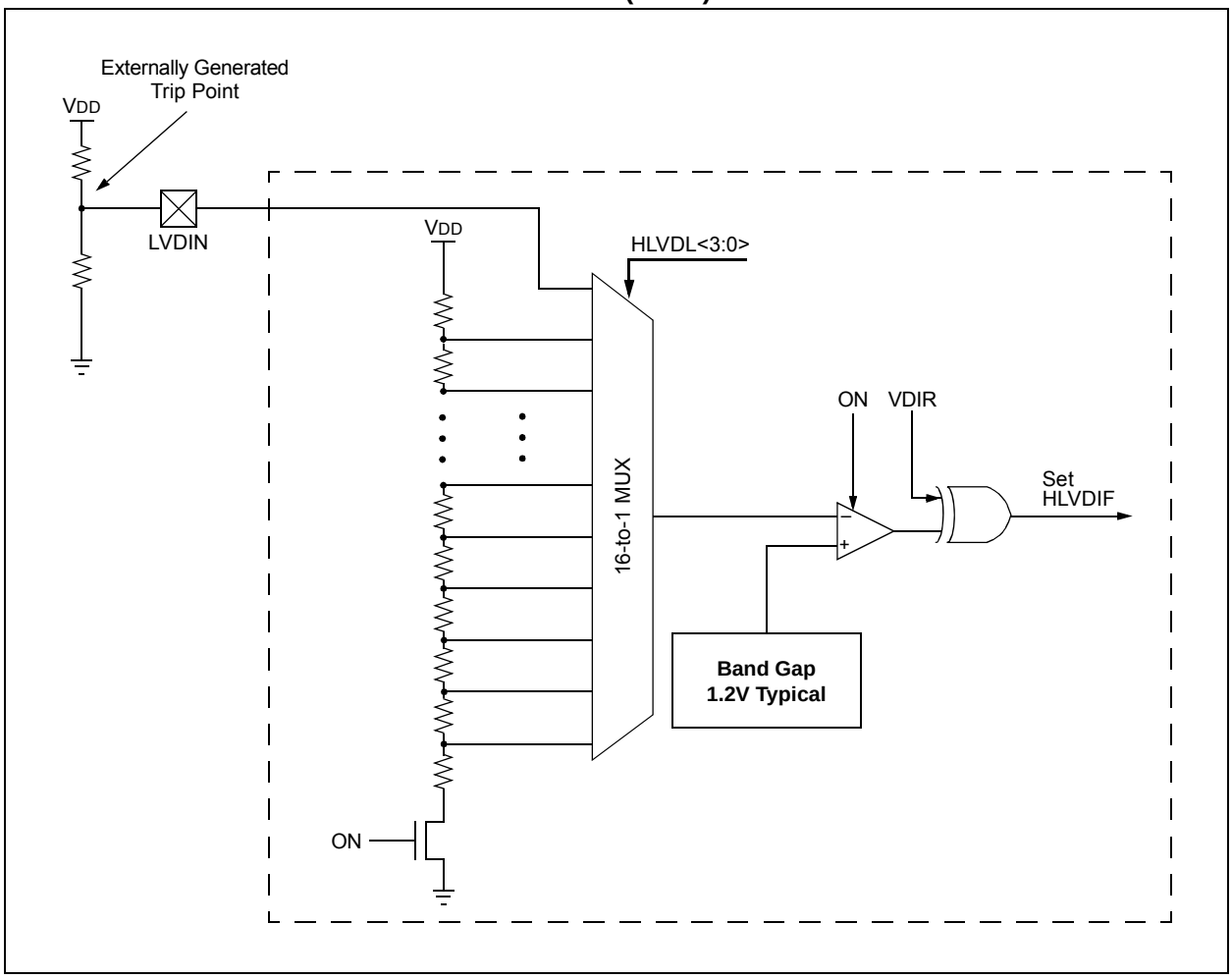
24.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 24-1) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

FIGURE 24-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER (CONTINUED)

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin and compared with 1.2V band gap)
1110 = VDD trip point is between 2.00V and 2.22V
1101 = VDD trip point is between 2.08V and 2.33V
1100 = VDD trip point is between 2.15V and 2.44V
1011 = VDD trip point is between 2.25V and 2.55V
1010 = VDD trip point is between 2.35V and 2.69V
1001 = VDD trip point is between 2.45V and 2.80V
1000 = VDD trip point is between 2.65V and 2.98V
0111 = VDD trip point is between 2.75V and 3.09V
0110 = VDD trip point is between 2.95V and 3.30V
0101 = VDD trip point is between 3.25V and 3.63V
0100-0000 = Reserved; do not use.

28.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

28.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

28.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MM0256GPM064 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MM0256GPM064 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any general purpose digital or analog pin (not 5.5V tolerant) with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any general purpose digital or analog pin (5.5V tolerant) with respect to V_{SS}:
When V_{DD} = 0V: ..... -0.3V to +4.0V
When $V_{DD} \geq$ 2.0V: ..... -0.3V to +6.0V
Voltage on AV_{DD} with respect to V_{DD} ..... (V_{DD} – 0.3V) to (lesser of: 4.0V or (V_{DD} + 0.3V))
Voltage on AV_{SS} with respect to V_{SS} ..... -0.3V to +0.3V
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin(1) ..... 300 mA
Maximum output current sunk by I/O pin ..... 11 mA
Maximum output current sourced by I/O pin ..... 16 mA
Maximum output current sunk by I/O pin with increased current drive strength
(RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) ..... 17 mA
Maximum output current sourced by I/O pin with increased current drive strength
(RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) ..... 24 mA
Maximum current sunk by all ports ..... 300 mA
Maximum current sourced by all ports(1) ..... 300 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 29-1).

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 29-11: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

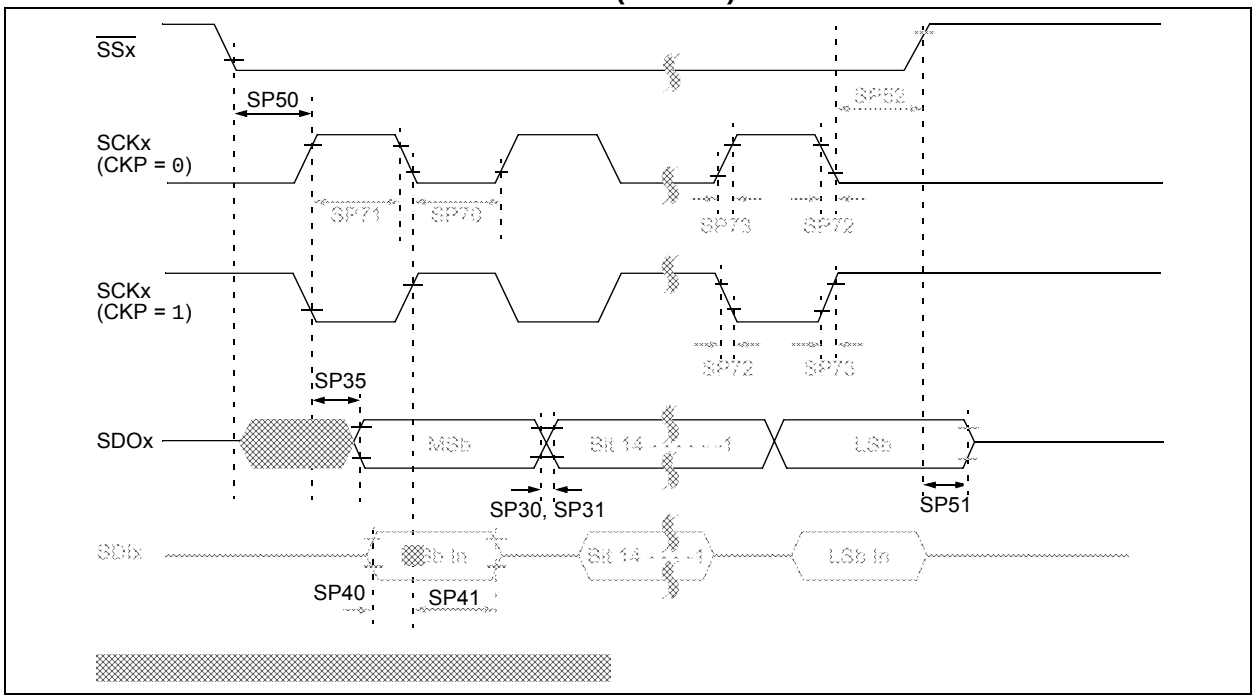


TABLE 29-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.0V
			—	—	10	ns	VDD < 2.0V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(4)	2.5	—	12	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 10 pF load on all SPIx pins.

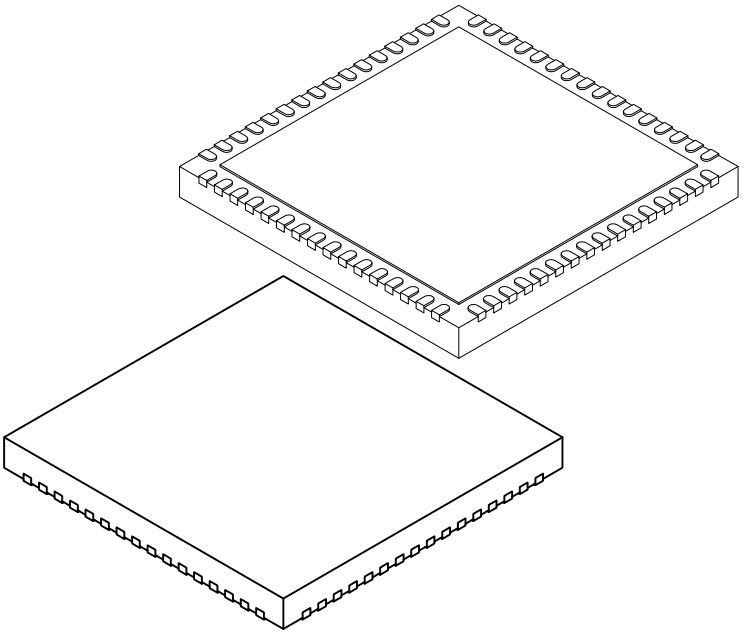
TABLE 29-38: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common-Mode Range	0.8	—	2.5	V	
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	14.25 kΩ load connected to 3.6V
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.60	7.70	7.80
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.60	7.70	7.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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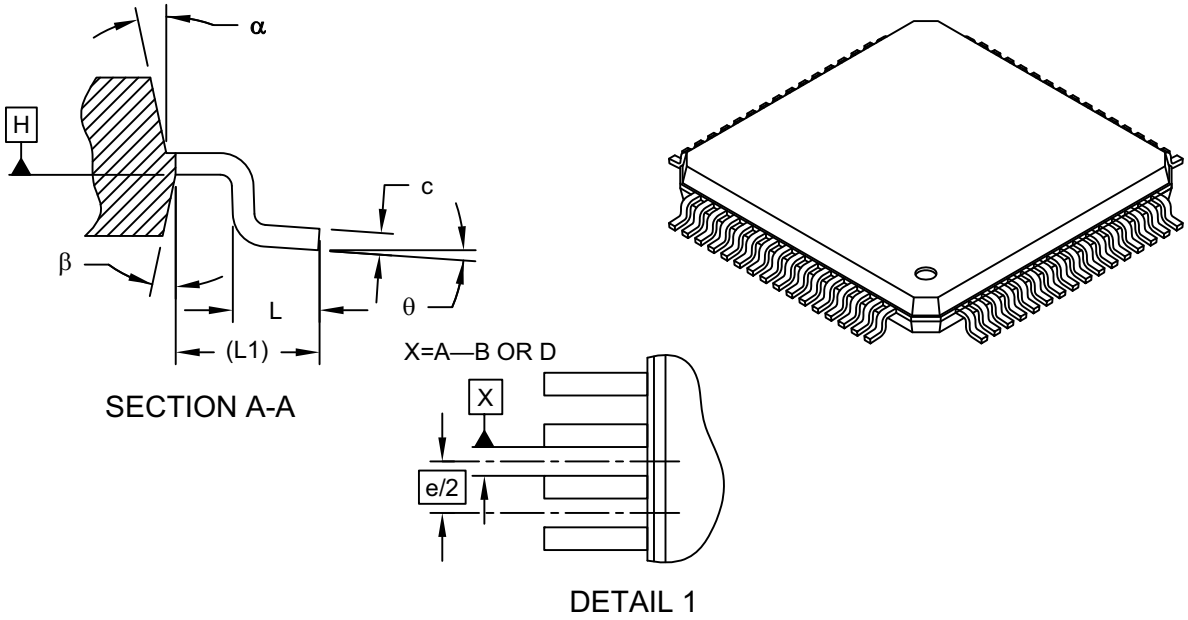
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision A (January 2016)

This is the initial version of the document.

Revision B (March 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Low-Power Modes"**, **"Peripheral Features"**, **"Microcontroller Features"** and **"Analog Features"** sections.
  - Changed program row size to 128 32-bit words in **Section 5.0 "Flash Program Memory"**.
  - Updated **Section 4.2 "Bus Matrix (BMX)"**, **Section 8.0 "Direct Memory Access (DMA) Controller"**, **Section 9.0 "Oscillator Configuration"**, **Section 9.2 "Clock Switching Operation"**, **Section 9.3 "FRC Active Clock Tuning"**, **Section 10.1 "CLR, SET and INV Registers"**, **Section 10.5 "I/O Port Write/Read Timing"**, **Section 10.6 "GPIO Port Merging"**, **Section 20.1 "Introduction"**, **Section 26.5 "Band Gap Voltage Reference"** and **Section 26.7 "Unique Device Identifier (UDID)"**.
  - Added the 36-Lead VQFN (M2) and 48-Lead UQFN (M4) packaging diagrams to **Section 30.0 "Packaging Information"**.
- Tables:
  - Updated Table 1-1, Table 7-2, Table 7-3, Table 9-1, Table 10-5, Table 10-6, Table 10-7, Table 10-8, Table 20-1, Table 26-3, Table 26-4, Table 26-6, Table 26-8, Table 29-2, Table 29-3, Table 29-4, Table 29-5, Table 29-6, Table 29-7, Table 29-8, Table 29-11, Table 29-14, Table 29-20 and Table 29-21.
  - Replaced Table 29-34 with Table 29-34, Table 29-35 and Table 29-36.
  - Removed previously numbered Table 29-35.
- Examples:
  - Updated Example 9-1.
- Figures:
  - Updated Figure 1-1, Figure 8-1, Figure 9-1, Figure 9-2 and Figure 22-1.
  - Added Figure 9-2.
- Registers:
  - Updated Register 6-4, Register 9-1, Register 9-2, Register 9-3, Register 9-5, Register 14-1, Register 19-1, Register 19-2, Register 26-1,Register 26-5 and Register 26-10.
  - Removed Register 9-7.

Revision C (May 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Peripheral Features"** section.
  - Updated **Section 2.3 "Master Clear (MCLR) Pin"** and **Section 25.3 "Retention Sleep Mode"**.
- Tables:
  - Updated Table 29-4, Table 29-5, Table 29-6 and Table 29-7.
- Registers:
  - Updated Register 13-1.

NOTES: