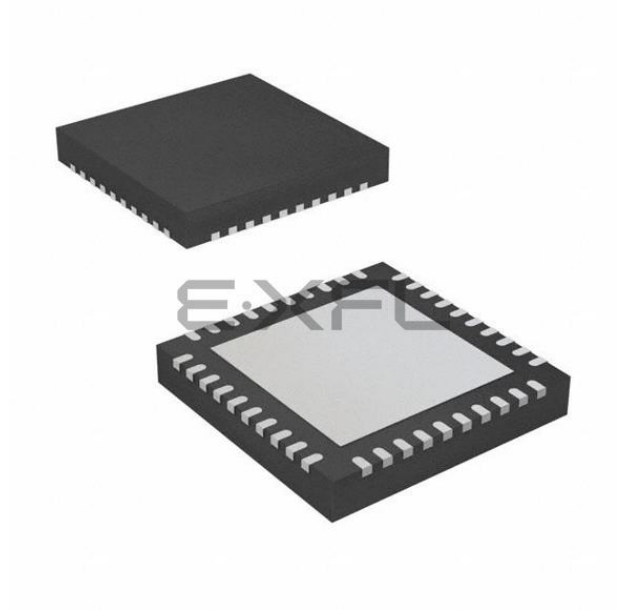
Microchip Technology - PIC32MM0256GPM036-I/MV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm036-i-mv

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0256GPM064 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0256GPM064 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0256GPM064 FAMILY BLOCK DIAGRAM

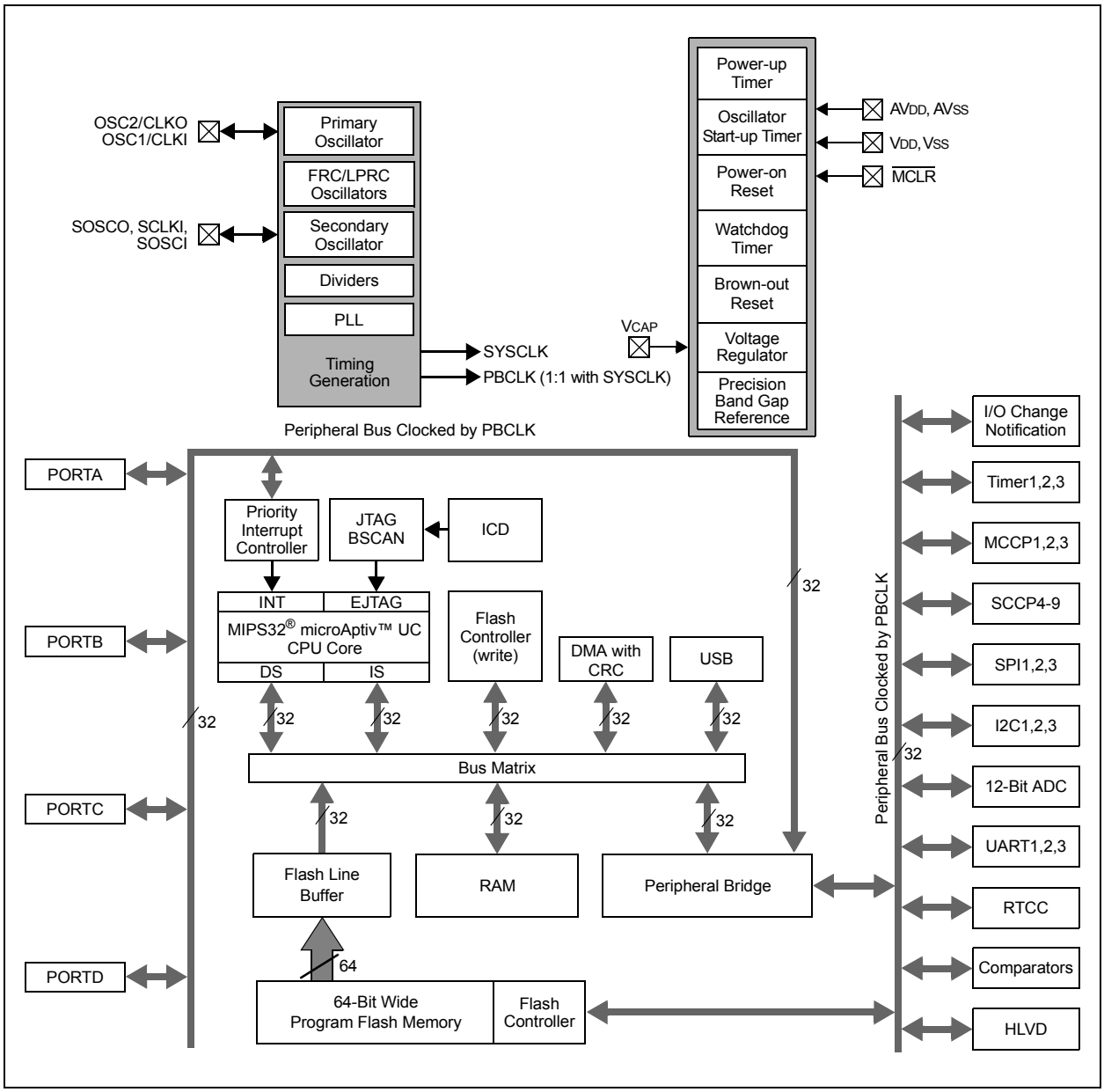


TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
AN0	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter input channels
AN1	3	28	34	37	22	12	I	ANA	
AN2	4	1	35	38	23	13	I	ANA	
AN3	5	2	36	39	24	14	I	ANA	
AN4	6	3	1	1	25	15	I	ANA	
AN5	9	6	7	7	32	25	I	ANA	
AN6	10	7	8	8	33	26	I	ANA	
AN7	11	8	9	9	35	28	I	ANA	
AN8	24	21	27	30	12	63	I	ANA	
AN9	25	22	28	31	15	2	I	ANA	
AN10	26	23	29	32	16	3	I	ANA	
AN11	7	4	2	2	26	16	I	ANA	
AN12	—	—	3	3	27	19	I	ANA	
AN13	—	—	4	4	28	20	I	ANA	
AN14	—	—	20	21	4	52	I	ANA	
AN15	—	—	—	—	41	37	I	ANA	
AN16	—	—	—	—	—	6	I	ANA	
AN17	—	—	—	—	—	7	I	ANA	
AN18	—	—	—	—	—	8	I	ANA	
AN19	—	—	—	—	—	10	I	ANA	
AVDD	28	25	31	34	18	5	P	—	Analog modules power supply
AVSS	27	24	30	33	17	4	P	—	Analog modules ground
C1INA	7	4	2	2	26	16	I	ANA	Comparator 1 Input A
C1INB	6	3	1	1	25	15	I	ANA	Comparator 1 Input B
C1INC	5	2	36	39	24	14	I	ANA	Comparator 1 Input C
C1IND	4	1	35	38	23	13	I	ANA	Comparator 1 Input D
C2INA	5	2	36	39	24	14	I	ANA	Comparator 2 Input A
C2INB	4	1	35	38	23	13	I	ANA	Comparator 2 Input B
C2INC	—	—	20	21	4	52	I	ANA	Comparator 2 Input C
C2IND	—	—	3	3	27	19	I	ANA	Comparator 2 Input D
C3INA	26	23	29	32	16	3	I	ANA	Comparator 3 Input A
C3INB	25	22	28	31	15	2	I	ANA	Comparator 3 Input B
C3INC	4	1	35	38	23	13	I	ANA	Comparator 3 Input C
C3IND	10	7	8	8	33	26	I	ANA	Comparator 3 Input D
CLKI	9	6	7	7	32	25	I	ST	External Clock source input (EC mode)
CLKO	10	7	8	8	33	26	O	DIG	System clock output
CVREF	25	22	28	31	15	2	O	ANA	Comparator voltage reference output
CVREF+	2	27	33	36	21	11	I	ANA	Positive comparator voltage reference input
D+	22	19	25	28	10	61	I/O	—	USB transceiver differential plus line
D-	21	18	24	27	9	60	I/O	—	USB transceiver differential minus line
FSYNC1	26	23	29	32	16	32	I/O	ST/DIG	SPI1 frame signal input or output
FSYNC3	14	11	15	15	45	22	I/O	ST/DIG	SPI3 frame signal input or output

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{\text{MCLR}}$.	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-Maskable Interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	_general_exception_handler
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	_general_exception_handler
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	_general_exception_handler

REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
	TGATE	TCKPS<2:0>			—	—	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer3 On bit
1 = Timer3 is enabled
0 = Timer3 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer3 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer3 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer3 Input Clock Prescale Select bits
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer3 Clock Source Select bit
1 = External clock is from the T3CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

14.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. "Capture/Compare/PWM/ Timer (MCCP and SCCP)"** (DS60001381) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

14.1 Introduction

PIC32MM0256GPM064 family devices include nine Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
  - Backward compatible with previous input capture peripherals of the PIC32 family
  - 16-bit or 32-bit capture of time base on external event
  - Up to four-level deep FIFO capture buffer
  - Capture source input multiplexer
  - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
  - Backward compatible with previous output compare peripherals of the PIC32 family
  - Single Edge and Dual Edge Compare modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
  - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 14-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

TABLE 14-1: MCCP/SCCP REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	CCP1CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0110	CCP1CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0120	CCP1CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0130	CCP1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0140	CCP1TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0150	CCP1PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0160	CCP1RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0170	CCP1RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0180	CCP1BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0200	CCP2CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0210	CCP2CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0220	CCP2CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0230	CCP2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0240	CCP2TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0250	CCP2PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	r-0	r-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	r = Reserved bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>) only if the RBF bit (I2CxSTAT<1>) = 0
0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 18 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 17-16 **Reserved:** Maintain as '0'

bit 15 **ON:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I^2C pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^2C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware is clear at the beginning of slave transmission. Hardware is clear at the end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware is clear at the beginning of slave transmission.

REGISTER 18-15: U1TOK: USB TOKEN REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0>(1)				EP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)

1101 = SETUP (TX) token type transaction
1001 = IN (RX) token type transaction
0001 = OUT (TX) token type transaction

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits

The 4-bit value must specify a valid endpoint.

Note 1: All other values not listed are reserved and must not be used.

REGISTER 18-16: U1SOF: USB SOF THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical Values of the Threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

NOTES:

REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half-second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = MCCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = MCCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

REGISTER 22-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1, 2 AND 3) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in CMSTAT register
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of the comparator connects to the band gap reference voltage
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

REGISTER 23-1: DAC1CON: VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **DACDAT<4:0>:** Voltage Reference Selection bits

11111 = (DACDAT<4:0> * CVREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** Voltage Reference Output Enable bit

1 = Voltage level is output on the CVREF pin
0 = Voltage level is disconnected from the CVREF pin

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the CVREF+ input pin voltage
00 = No reference is selected – output is AVSS

TABLE 26-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1840	UDID1	31:16	UDID Word 1<31:0>																xxxx
		15:0																	xxxx
1844	UDID2	31:16	UDID Word 2<31:0>																xxxx
		15:0																	xxxx
1848	UDID3	31:16	UDID Word 3<31:0>																xxxx
		15:0																	xxxx
184C	UDID4	31:16	UDID Word 4<31:0>																xxxx
		15:0																	xxxx
1850	UDID5	31:16	UDID Word 5<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 26-8: RESERVED REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2900	RESERVED1	31:16	Reserved Register 1<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 29-3: OPERATING VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DC10	VDD	**Supply Voltage**	2.0	—	3.6	V	
DC16	VPOR(1)	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	100	mV	
DC17A	SVDD(1)	**Recommended VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 66 ms, 0-2.0V in 40 ms
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	—	2.083	V	

Note 1: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

TABLE 29-4: OPERATING CURRENT (IDD)(2)

DC CHARACTERISTICS						
Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC19	.72	.96	mA	-40°C to +85°C	2.0V	FSYS = 1 MHz
	—	.96	mA	-40°C to +85°C	3.3V	
DC23	2.5	3.7	mA	-40°C to +85°C	2.0V	FSYS = 8 MHz
	2.5	3.7	mA	-40°C to +85°C	3.3V	
DC24	7.9	10.2	mA	-40°C to +85°C	2.0V	FSYS = 25 MHz
	7.9	10.2	mA	-40°C to +85°C	3.3V	
DC25	.4	.8	μA	-40°C to +85°C	2.0V	LPRC, FSYS = 32 kHz
	.4	.8	μA	-40°C to +85°C	3.3V	

Note 1: Typical parameters are for design guidance only and are not tested.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}}$ = VDD; WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing:

```
while(1)
 {
 NOP();
 }
```

3: JTAG is disabled

TABLE 29-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

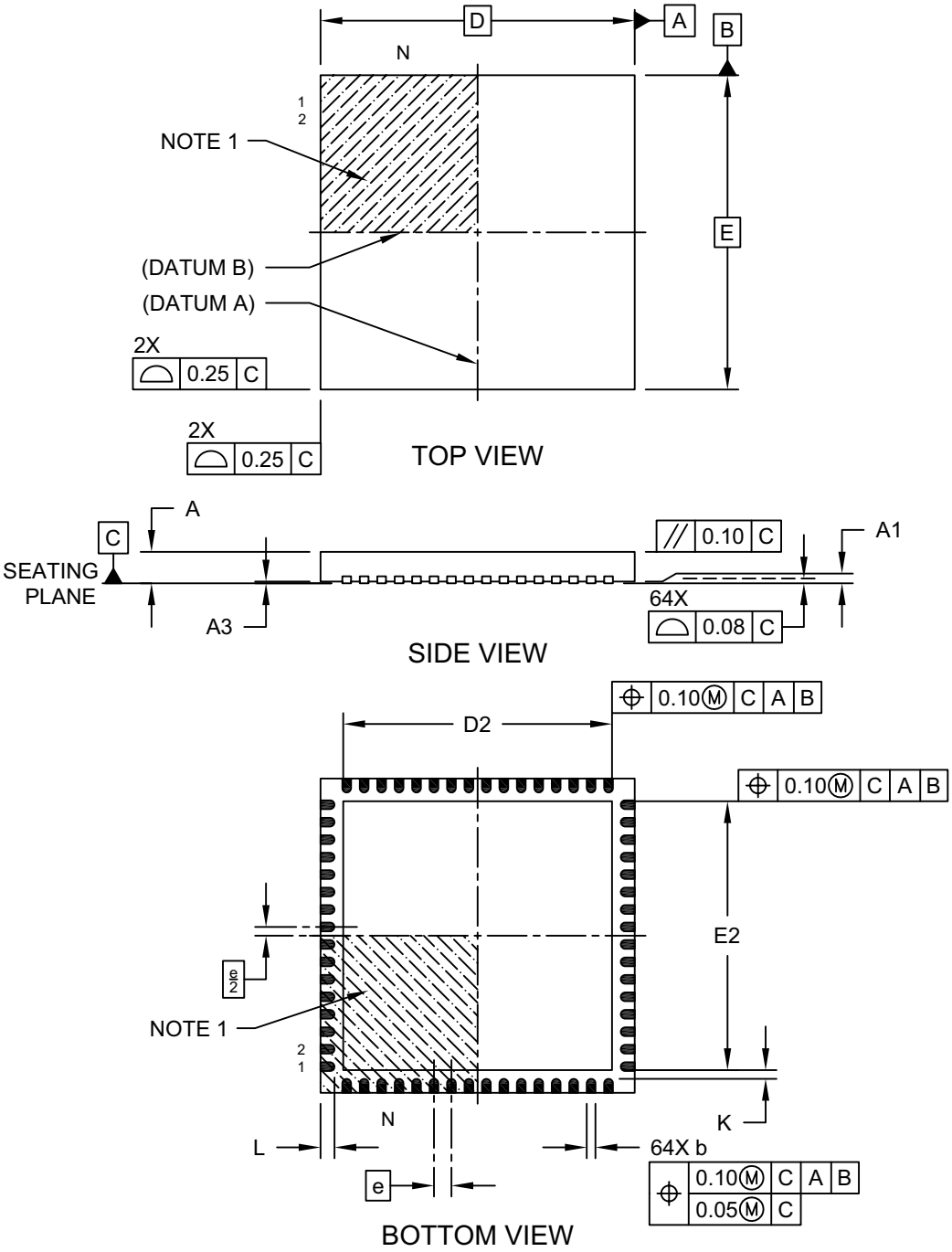
Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	VBG	Internal Band Gap Reference	—	1.2	—	V	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 1.9V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Series Resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, RETVR (FPOR<2>) = 0

TABLE 29-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0101	3.25	—	3.63	V	
			HLVDL<3:0> = 0110	2.95	—	3.30	V	
			HLVDL<3:0> = 0111	2.75	—	3.09	V	
			HLVDL<3:0> = 1000	2.65	—	2.98	V	
			HLVDL<3:0> = 1001	2.45	—	2.80	V	
			HLVDL<3:0> = 1010	2.35	—	2.69	V	
			HLVDL<3:0> = 1011	2.25	—	2.55	V	
			HLVDL<3:0> = 1100	2.15	—	2.44	V	
			HLVDL<3:0> = 1101	2.08	—	2.33	V	
			HLVDL<3:0> = 1110	2.00	—	2.22	V	
DC101	VTHL	HLVD Voltage on LVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.2	—	V	

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2