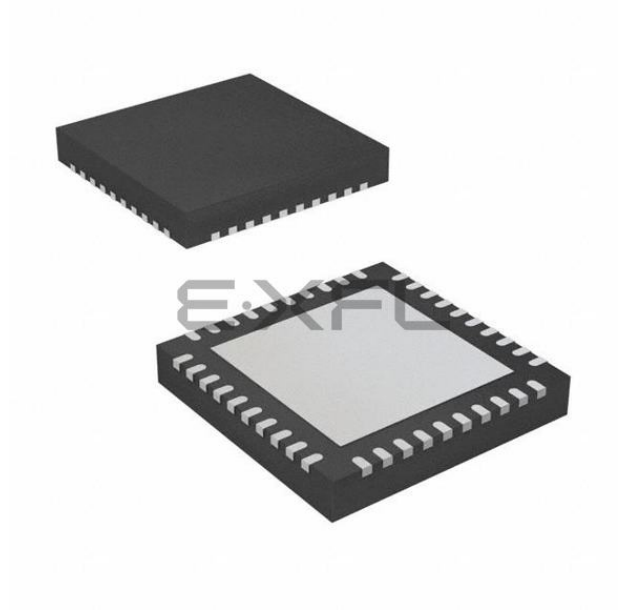
Microchip Technology - PIC32MM0256GPM036T-I/MV Datasheet



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Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm036t-i-mv

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
INT0	26	23	29	32	16	32	I	ST	External Interrupt 0
INT1	25	22	28	31	15	31	I	ST	External Interrupt 1
INT2	18	15	19	20	1	49	I	ST	External Interrupt 2
INT3	2	27	33	36	40	36	I	ST	External Interrupt 3
LVDIN	24	21	20	21	4	52	I	ANA	High/Low-Voltage Detect input
$\overline{\text{MCLR}}$	1	26	32	35	19	9	I	ST	Master Clear (device Reset)
OCM1A	17	14	18	18	48	7	O	DIG	MCCP1 Output A
OCM1B	18	15	19	20	1	53	O	DIG	MCCP1 Output B
OCM1C	9	6	7	7	32	25	O	DIG	MCCP1 Output C
OCM1D	10	7	8	8	41	37	O	DIG	MCCP1 Output D
OCM1E	2	27	33	36	40	36	O	DIG	MCCP1 Output E
OCM1F	3	28	34	37	22	12	O	DIG	MCCP1 Output F
OCM2A	19	16	5	5	29	21	O	DIG	MCCP2 Output A
OCM2B	26	23	29	32	39	35	O	DIG	MCCP2 Output B
OCM2C	4	1	35	38	23	13	O	DIG	MCCP2 Output C
OCM2D	5	2	36	39	24	14	O	DIG	MCCP2 Output D
OCM2E	6	3	1	1	25	15	O	DIG	MCCP2 Output E
OCM2F	7	4	2	2	26	16	O	DIG	MCCP2 Output F
OCM3A	24	21	11	11	37	54	O	DIG	MCCP3 Output A
OCM3B	25	22	28	31	15	33	O	DIG	MCCP3 Output B
OCM3C	11	8	9	9	35	59	O	DIG	MCCP3 Output C
OCM3D	12	9	10	10	36	41	O	DIG	MCCP3 Output D
OCM3E	14	11	15	15	45	42	O	DIG	MCCP3 Output E
OCM3F	16	13	17	17	47	45	O	DIG	MCCP3 Output F
OSC1	9	6	7	7	32	25	—	—	Primary Oscillator crystal
OSC2	10	7	8	8	33	26	—	—	Primary Oscillator crystal
PGEC1	5	2	36	39	24	14	I	ST	ICSP™ Port 1 programming clock input
PGEC2	2	27	33	36	21	11	I	ST	ICSP Port 2 programming clock input
PGEC3	19	16	21	22	5	55	I	ST	ICSP Port 3 programming clock input
PGED1	4	1	35	38	23	13	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	3	28	34	37	22	12	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	14	11	15	15	45	43	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	12	9	10	10	36	29	I	ST	Real-Time Clock 50/60 Hz clock input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0256GPM064 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)
- VUSB3V3 pin, this pin must be powered for USB operation (see **Section 18.4 "Powering the USB Transceiver"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information are available by accessing the CP0 registers listed in Table 3-2.

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	INTCON	31:16	—	—	—	—	—	—	—	—	—	VS<6:0>							0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
F010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
F020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
F030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
F040	IFS0	31:16	—	USBIF	—	—	—	—	CMP3IF	CMP2IF	CMP1IF	—	—	—	T3IF	T2IF	T1IF	—	0000
		15:0	—	—	—	—	CNDIF	CNCIF	CNBIF	CNAIF	INT4IF	INT3IF	INT2IF	INT1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
F050	IFS1	31:16	—	—	U3EIF	U3TXIF	U3RXIF	U2EIF	U2TXIF	U2RXIF	U1EIF	U1TXIF	U1RXIF	—	—	—	SPI3RXIF	SPI3TXIF	0000
		15:0	SPI3EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	LVDIF	—	—	AD1IF	RTCCIF	0000
F060	IFS2	31:16	CPCIF	NVMIF	—	FSTIF	CCT9IF	CCP9IF	CCT8IF	CCP8IF	CCT7IF	CCP7IF	CCT6IF	CCP6IF	CCT5IF	CCP5IF	CCT4IF	CCP4IF	0000
		15:0	CCT3IF	CCP3IF	CCT2IF	CCP2IF	CCT1IF	CCP1IF	I2C3BCIF	I2C3MIF	I2C3SIF	I2C2BCIF	I2C2MIF	I2C2SIF	I2C1BCIF	I2C1MIF	I2C1SIF	—	0000
F070	IFS3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	ECCBEIF	—	0000
F080	IEC0	31:16	—	USBIE	—	—	—	—	CMP3IE	CMP2IE	CMP1IE	—	—	—	T3IE	T2IE	T1IE	—	0000
		15:0	—	—	—	—	CNDIE	CNCIE	CNBIE	CNAIE	INT4IE	INT3IE	INT2IE	INT1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
F090	IEC1	31:16	—	—	U3EIE	U3TXIE	U3RXIE	U2EIE	U2TXIE	U2RXIE	U1EIE	U1TXIE	U1RXIE	—	—	—	SPI3RXIE	SPI3TXIE	0000
		15:0	SPI3EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	LVDIE	—	—	AD1IE	RTCCIE	0000
F0A0	IEC2	31:16	CPCIE	NVMIE	—	FSTIE	CCT9IE	CCP9IE	CCT8IE	CCP8IE	CCT7IE	CCP7IE	CCT6IE	CCP6IE	CCT5IE	CCP5IE	CCT4IE	CCP4IE	0000
		15:0	CCT3IE	CCP3IE	CCT2IE	CCP2IE	CCT1IE	CCP1IE	I2C3BCIE	I2C3MIE	I2C3SIE	I2C2BCIE	I2C2MIE	I2C2SIE	I2C1BCIE	I2C1MIE	I2C1SIE	—	0000
F0B0	IEC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	ECCBEIE	—	0000
F0C0	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
F0D0	IPC1	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
F0E0	IPC2	31:16	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
F0F0	IPC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

NOTES:

REGISTER 8-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON(1)	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: The user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 8-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTRx = CHSSIZx)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTRx = CHSSIZx/2)
0 = No interrupt is pending

REGISTER 9-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
0111 = System PLL VCO output (not divided)
0110 = Reserved
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = Reserved
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 9-6: OSCTUN: FRC TUNING REGISTER (CONTINUED)

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency – 1.50%
100001 =
•
•
•
111111 =
000000 = Center frequency; oscillator runs at a nominal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency + 1.453%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note:	Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0930	CCP9STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0940	CCP9TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0950	CCP9PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0960	CCP9RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0970	CCP9RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0980	CCP9BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half-second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

REGISTER 21-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 1
0 = The Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 1
0 = The Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

23.0 VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference"** (DS61109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The CVREF module is a 32-TAP DAC that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently from them.

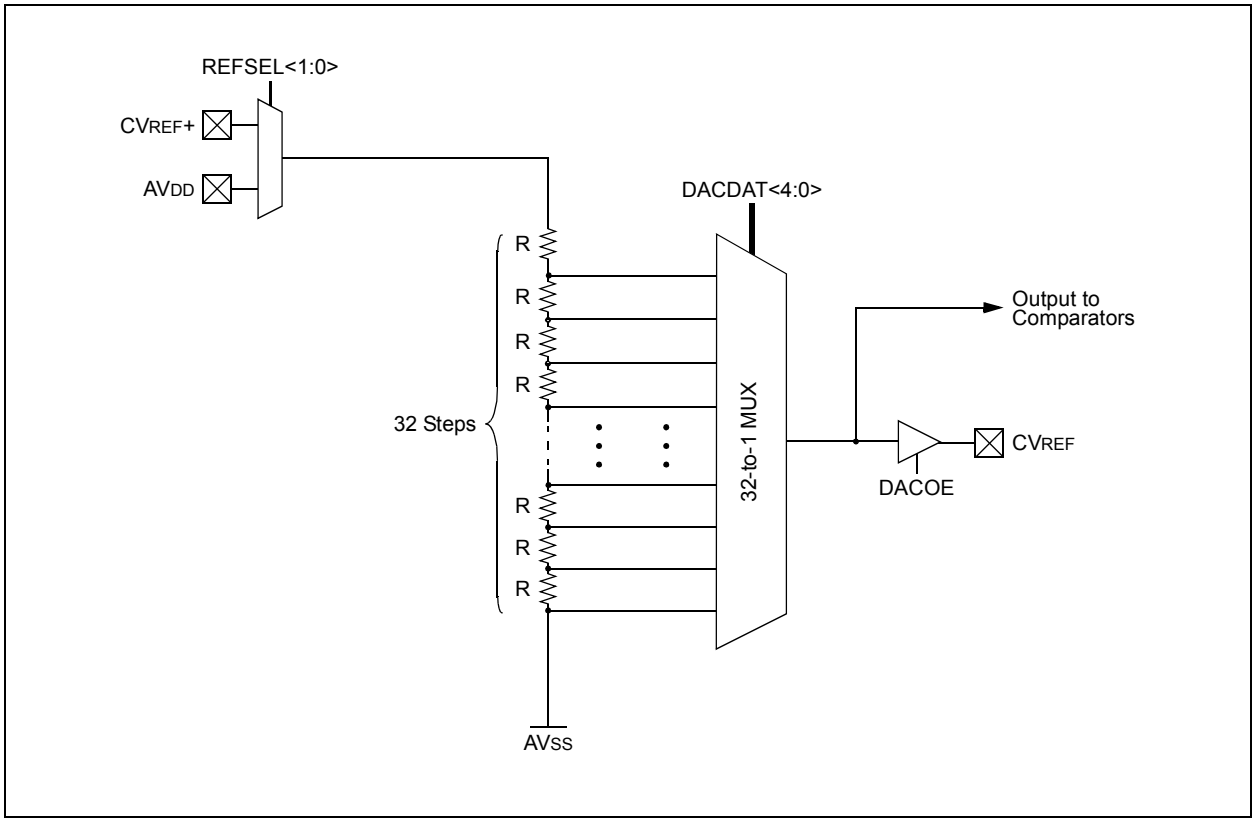
The module's supply reference can be provided from either the device VDD/VSS or an external voltage reference pin. The CVREF output is available for the comparators and for pin output.

The voltage reference has the following features:

- 32 Output Levels are Available
- Internally Connected to Comparators to Conserve Device Pins
- Output can be Connected to a Pin

A block diagram of the CVREF module is illustrated in Figure 23-1.

FIGURE 23-1: VOLTAGE REFERENCE BLOCK DIAGRAM



REGISTER 26-1: FDEVOPT/AFDEVOPT: DEVICE OPTIONS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							
15:8	R/P	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	FVBUSIO	FUSBIDIO	—	—	—	—	—	—
7:0	r-1	r-1	r-1	R/P	R/P	r-1	r-1	r-1
	—	—	—	ALTI2C	SOSCHP	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **USERID<15:0>:** User ID bits (2 bytes which can programmed to any value)

bit 15 **FVBUSIO:** USB VBUS_ON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 14 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 13-5 **Reserved:** Program as '1'

bit 4 **ALTI2C:** Alternate I2C1 Location Select bit
1 = SDA1 and SCL1 are on pins, RB8 and RB9
0 = SDA1 and SCL1 are moved to alternate I^2C locations, RB5 and RC9

bit 3 **SOSCHP:** Secondary Oscillator (SOSC) High-Power Enable bit
1 = SOSC operates in normal power mode
0 = SOSC operates in High-Power mode

bit 2-0 **Reserved:** Program as '1'

TABLE 29-5: IDLE CURRENT (I_{IDLE})(2)

DC CHARACTERISTICS						
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**V_{DD}**	**Conditions**
DC40	.69	.8	μA	-40°C to +85°C	2.0V	F_{SYS} = 1 MHz
	.69	.8	μA	-40°C to +85°C	3.3V	
DC41	.98	1.7	mA	-40°C to +85°C	2.0V	F_{SYS} = 8 MHz
	.98	1.7	mA	-40°C to +85°C	3.3V	
DC42	2.9	3.7	mA	-40°C to +85°C	2.0V	F_{SYS} = 25 MHz
	2.9	3.7	mA	-40°C to +85°C	3.3V	
DC44	.36	.7	μA	-40°C to +85°C	2.0V	F_{SYS} = 32 kHz
	.36	.7	μA	-40°C to +85°C	3.3V	

Note 1: Parameters are for design guidance only and are not tested.

2: Base I_{IDLE} current is measured with the core in Idle, the clock on and all modules turned off. OSC1 driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required). Peripheral Module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to V_{SS}.

TABLE 29-14: COMPARATOR DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	-20	—	+20	mV	**(Note 1)**
D301	VICM	Input Common-Mode Voltage	VSS – 0.3V	—	VDD + 0.3V	V	**(Note 1)**
D307	TRESP	Response Time	—	150	—	ns	**(Note 2)**

Note 1: Parameters are characterized but not tested.

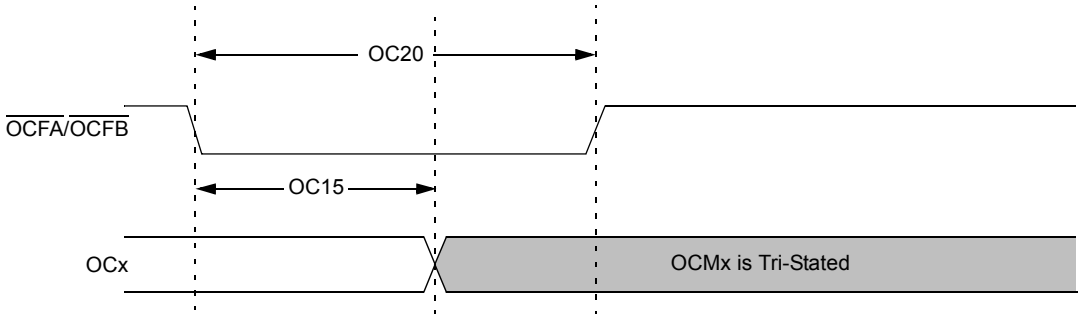
2: Measured with one input at VDD/2 and the other transitioning from VSS to VDD, 40 mV step, 15 mV overdrive.

TABLE 29-15: VOLTAGE REFERENCE DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VRD310	TSET	Settling Time	—	—	10	µs	**(Note 1)**
VRD311	VRAA	Absolute Accuracy	-1	—	1	LSb	
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ	

Note 1: Measures the interval while DACDAT<4:0> transitions from '11111' to '00000'.

FIGURE 29-8: MCCP AND SCCP PWM MODE TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

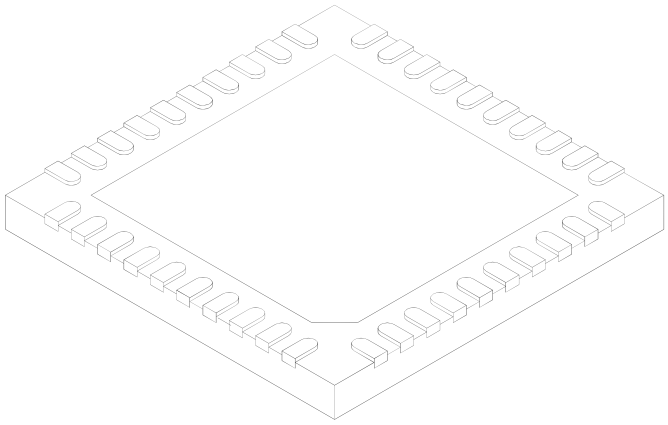
TABLE 29-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	10	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2