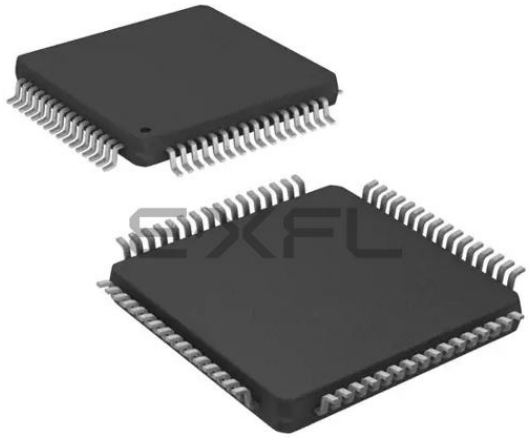
Microchip Technology - PIC32MM0256GPM064-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	IrDA, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 20x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mm0256gpm064-i-pt

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority 3 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority 3 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority 2 bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority 2 bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8A50	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8A60	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8A70	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
8A80	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
8A90	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
8AA0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
8AB0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8AC0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8AD0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
8AE0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8AF0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8B00	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
8B10	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8B20	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8B30	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

REGISTER 8-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON(1)	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

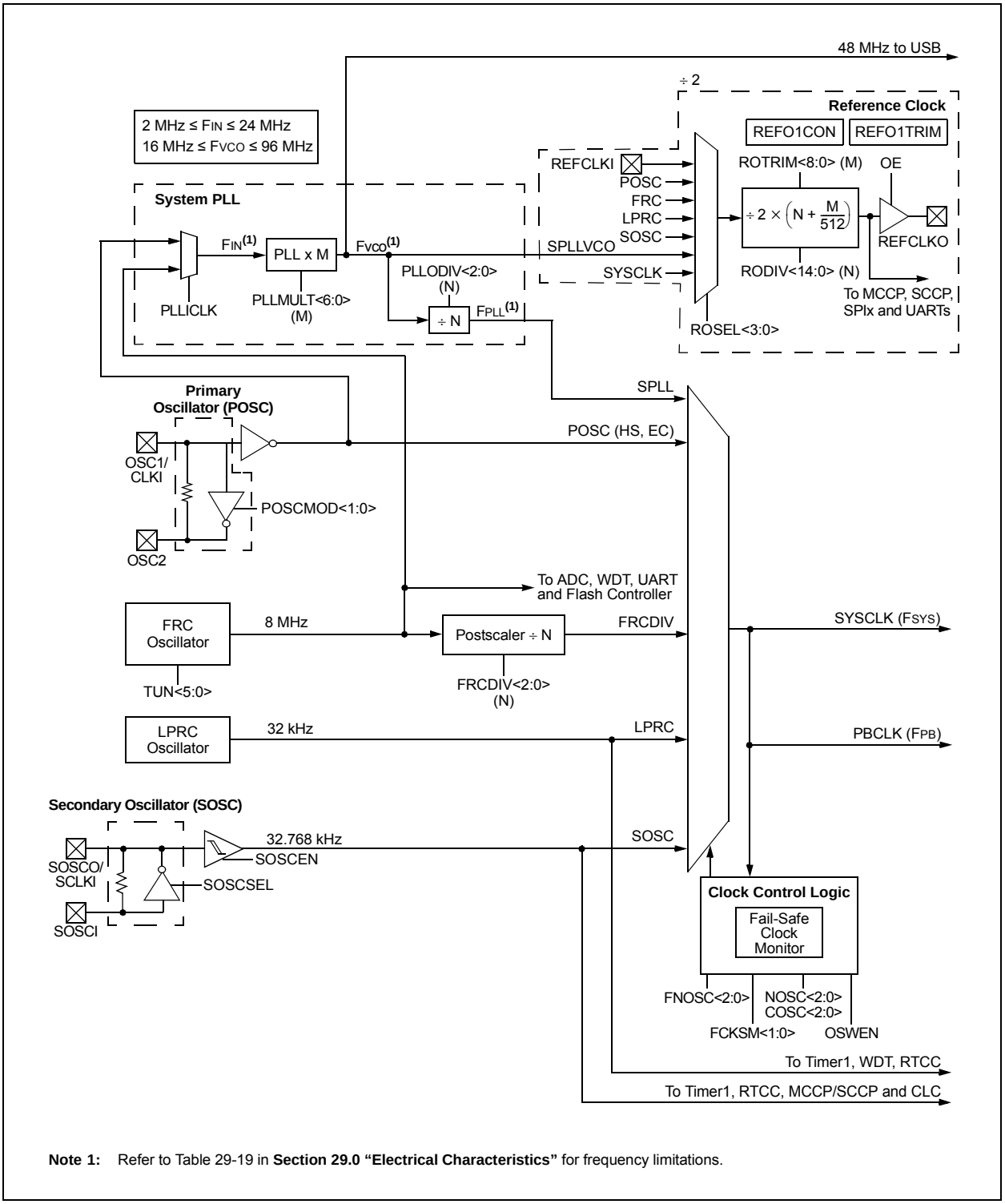
bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: The user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

FIGURE 9-1: PIC32MM0256GPM064 FAMILY OSCILLATOR DIAGRAM(1)



Note 1: Refer to Table 29-19 in **Section 29.0 "Electrical Characteristics"** for frequency limitations.

REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from T2CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: The user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only available on even numbered timers (Timer2).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0430	CCP4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0440	CCP4TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0450	CCP4PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0460	CCP4RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0470	CCP4RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0480	CCP4BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0500	CCP5CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0510	CCP5CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0520	CCP5CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0530	CCP5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0540	CCP5TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0550	CCP5PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0560	CCP5RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0570	CCP5RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0580	CCP5BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event

bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as '0'. A write of '1' will initiate the hardware event.

REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 11 **STRICT:** Strict I^2C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced; device does not respond to reserved address space or generates addresses in reserved address space
0 = Strict I^2C reserved address rule is not enabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with the SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^2C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on the SDAx and SCLx pins and transmits the ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

TABLE 18-1: USB OTG REGISTER MAP (CONTINUED)

Virtual Address (BF88_ #)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8770	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8780	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8790	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

REGISTER 18-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

bit 11 **WRLOCK:** RTCC Registers Write Lock bit
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
• • •
011 = Reserved
010 = RTCC input clock source (user-defined divided output based on the combination of the RTCCON2 bits, DIV<15:0> and PS<1:0>)
001 = Seconds clock
000 = Alarm event

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

REGISTER 19-2: RTCCON2: RTCC CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	PS<1:0>		—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter for the seconds output.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **PS<1:0>:** Prescale Select bits
Sets the prescaler for the seconds output.
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

20.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- **AD1CON1: ADC Control Register 1**
- **AD1CON2: ADC Control Register 2**
- **AD1CON3: ADC Control Register 3**
- **AD1CON5: ADC Control Register 5**

  The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.
- **AD1CHS: ADC Input Select Register**

  The AD1CHS register selects the input pins to be connected to the SHA.
- **AD1CSS: ADC Input Scan Select Register**

  The AD1CSS register selects inputs to be sequentially scanned.
- **AD1CHIT: ADC Compare Hit Register**

  The AD1CHIT register indicates the channels meeting specified comparison requirements.

Table 20-1 provides a summary of all ADC related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

REGISTER 20-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	EXTSAM	—	SAMC<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from the Fast RC (FRC) oscillator
0 = Clock derived from the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

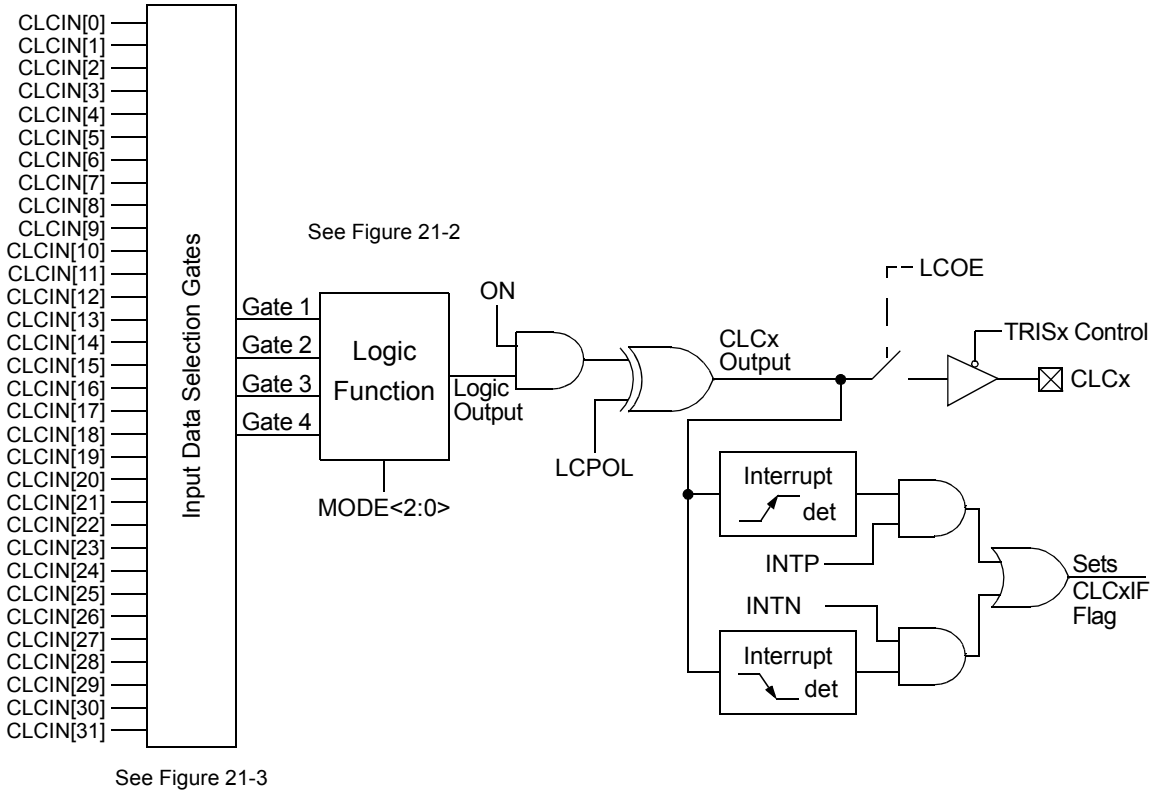
21.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. "Configurable Logic Cell"** (DS60001363) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 21-1 shows an overview of the module. Figure 21-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 21-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCON register.

REGISTER 26-3: FPOR/AFPOR: POWER-UP SETTINGS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	LPBOREN	RETVR	BOREN<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

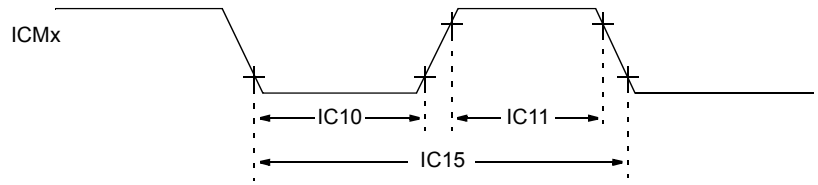
bit 31-4 **Reserved:** Program as '1'

bit 3 **LPBOREN:** Low-Power BOR Enable bit
1 = Low-Power BOR is enabled when main BOR is disabled
0 = Low-Power BOR is disabled

bit 2 **RETVR:** Retention Voltage Regulator Enable bit
1 = Retention regulator is disabled
0 = Retention regulator is enabled and controlled by the RETEN bit during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

FIGURE 29-6: MCCP AND SCCP INPUT CAPTURE MODE TIMING CHARACTERISTICS



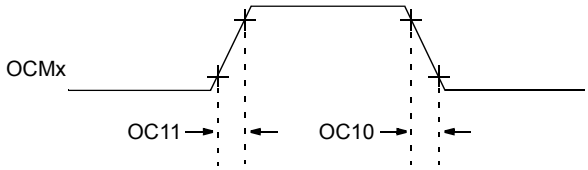
Note: Refer to Figure 29-2 for load conditions.

TABLE 29-25: MCCP AND SCCP INPUT CAPTURE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**
IC10	TccL	ICMx Input Low Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC11	TccH	ICMx Input High Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC15	TccP	ICMx Input Period	[(25 ns or 2 TPBCLK)/N] + 50 ns	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 29-7: MCCP AND SCCP OUTPUT COMPARE MODE TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-26: MCCP AND SCCP OUTPUT COMPARE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCMx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCMx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

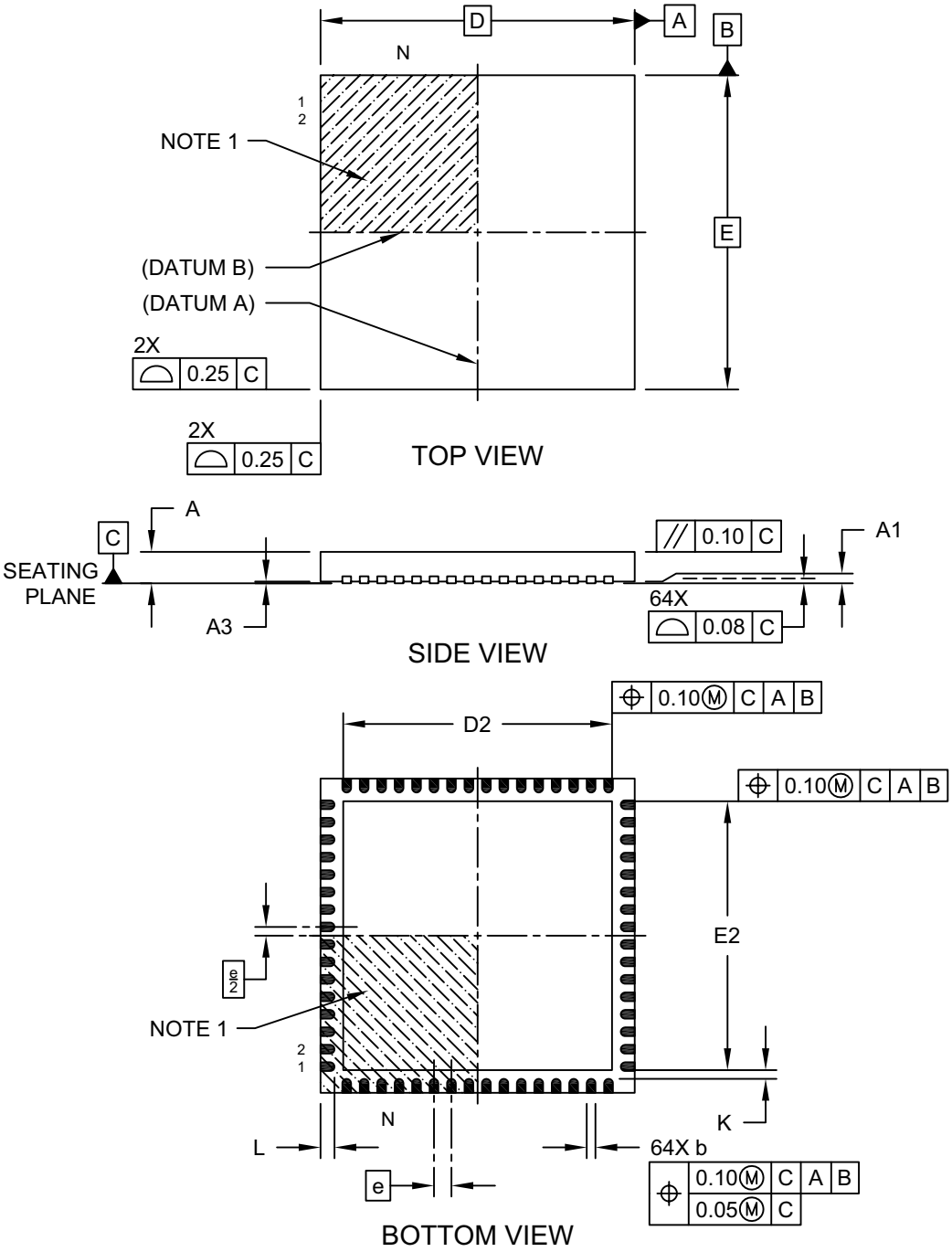
TABLE 29-38: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common-Mode Range	0.8	—	2.5	V	
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	14.25 kΩ load connected to 3.6V
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2