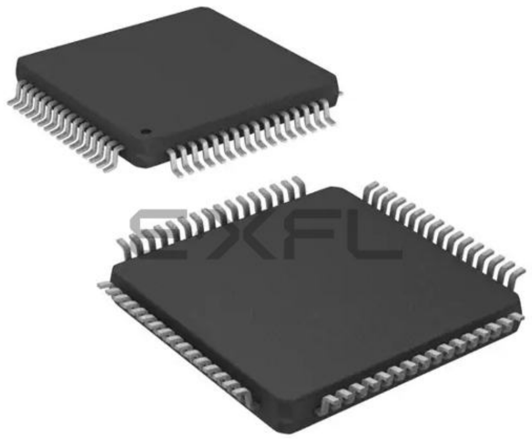

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Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18c601t-i-pt

TABLE 1-2: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	PIC18C601		PIC18C801				
	TQFP	PLCC	TQFP	PLCC			
							PORTF is a bi-directional I/O port.
RF0/AN5	18	28	24	36			
RF0					I/O	ST	Digital I/O.
AN5					I	Analog	Analog input 5.
RF1/AN6	17	27	23	35			
RF1					I/O	ST	Digital I/O.
AN6					I	Analog	Analog input 6.
RF2/AN7	16	26	18	30			
RF2					I/O	ST	Digital I/O.
AN7					I	Analog	Analog input 7.
RF3/$\overline{CSIO}$	15	25	17	29			
RF3					I/O	ST	Digital I/O.
$\overline{CSIO}$					I/O	ST	System bus chip select I/O.
RF4/A16	14	24	—	—			
RF4/$\overline{CS2}$	—	—	16	28			
RF4					I/O	ST	Digital I/O.
A16					I/O	TTL	External memory address 16.
$\overline{CS2}$					O	TTL	Chip select 2.
RF5/$\overline{CS1}$	13	23	15	27			
RF5					I/O	ST	Digital I/O.
$\overline{CS1}$					O	TTL	Chip select 1.
RF6/$\overline{LB}$	12	22	14	26			
RF6					I/O	ST	Digital I/O.
$\overline{LB}$					O	TTL	Low byte select signal for external memory interface.
RF7/$\overline{UB}$	11	21	13	25			
RF7					I/O	ST	Digital I/O.
$\overline{UB}$					O	TTL	High byte select signal for external memory interface.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open Drain (no P diode to V_{DD})

6.3.4 16-BIT EXTERNAL TABLE WRITE (BYTE SELECT MODE)

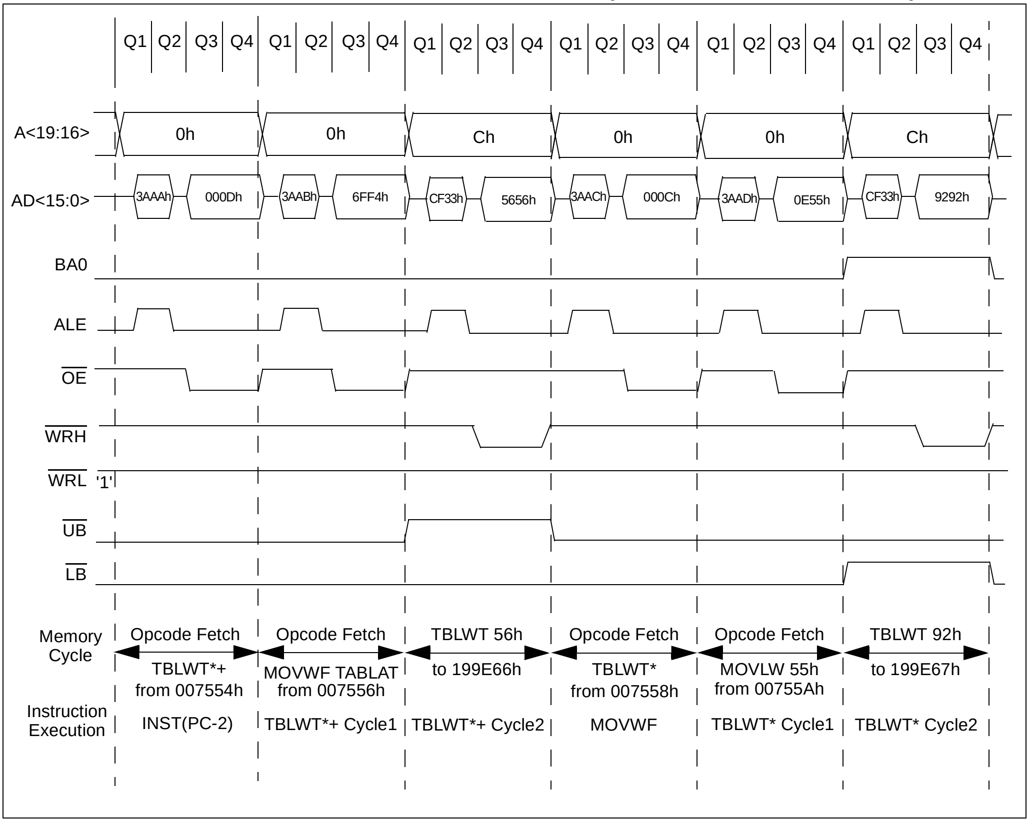
This mode allows Table Writes to word-wide external memories that have byte selection capabilities. This generally includes word-wide FLASH devices and word-wide static RAM devices.

During a `TBLWT` cycle, the TABLAT data is presented on the upper and lower byte of the AD<15:0> bus. The WRH line is strobed for each write cycle and the WRL line is unused. The BA0 or UB or UL lines are used to select the byte to be written, based on the LSb of the TBLPTR.

JEDEC standard flash memories will require a I/O port line to become a BYTE/WORD input signal and will use the BA0 signal as a byte address. JEDEC standard static RAM memories will use the UB or UL signals to select the byte.

Figure 6-10 shows the timing associated with this mode.

FIGURE 6-10: `TBLWT` EXTERNAL INTERFACE TIMING (16-BIT BYTE SELECT MODE)



 Advance Information

TABLE 9-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/AD0/A0(2)	bit0	ST/TTL(1)	Input/output port pin or system bus bit 0
RD1/AD1/A1(2)	bit1	ST/TTL(1)	Input/output port pin or system bus bit 1
RD2/AD2/A2(2)	bit2	ST/TTL(1)	Input/output port pin or system bus bit 2
RD3/AD3/A3(2)	bit3	ST/TTL(1)	Input/output port pin or system bus bit 3
RD4/AD4/A4(3)	bit4	ST/TTL(1)	Input/output port pin or system bus bit 4
RD5/AD5/A5(2)	bit5	ST/TTL(1)	Input/output port pin or system bus bit 5
RD6/AD6/A6(2)	bit6	ST/TTL(1)	Input/output port pin or system bus bit 6
RD7/AD7/A7(2)	bit7	ST/TTL(1)	Input/output port pin or system bus bit 7

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in System Bus mode.

2: RDx is used as a multiplexed address/data bus for PIC18C601 and PIC18C801 in 16-bit mode, and as an address only for PIC18C801 in 8-bit mode.

TABLE 9-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
LATD	LATD Data Output Register								xxxx xxxx	uuuu uuuu
TRISD	PORTD Data Direction Register								1111 1111	1111 1111
MEMCON	EBDIS	PGRM	WAIT1	WAIT0	—	—	WM1	WM0	0000 --00	0000 --00

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

9.7 PORTG, LATG, and TRISG Registers

PORTG is a 5-bit wide, bi-directional port. The corresponding data direction register is TRISG. Setting a TRISG bit (= 1) will make the corresponding PORTG pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISG bit (= 0) will make the corresponding PORTG pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATG register read and write the latched output value for PORTG.

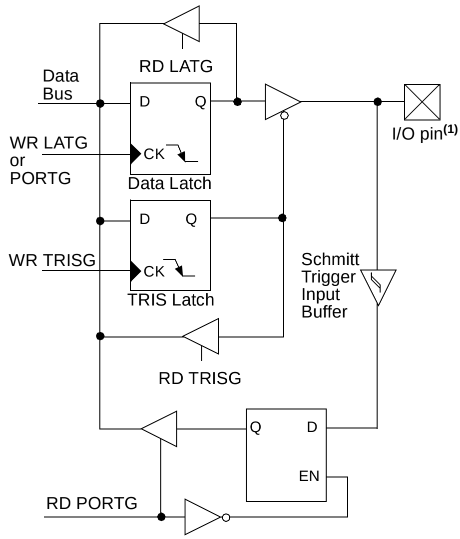
PORTG is multiplexed with system bus control signals ALE, $\overline{OE}$, $\overline{WRH}$, $\overline{WRL}$ and BA0. The $\overline{WRH}$ signal is the only signal that is disabled and configured as a port pin (RG3) during external program execution in 8-bit mode. All other pins are by default, system bus control signals. PORTG can be configured as an I/O port by setting EBDIS bit in the MEMCON register and when execution is taking place in internal program RAM.

Note:	On Power-on Reset, PORTG defaults to system bus signals.

EXAMPLE 9-8: INITIALIZING PORTG

```
CLRF    PORTG      ; Initialize PORTG by
                   ; clearing output
                   ; data latches
CLRF    LATG       ; Alternate method
                   ; to clear output
                   ; data latches
MOVLW   04h        ; Value used to
                   ; initialize data
                   ; direction
MOVWF   TRISG      ; Set RG1:RG0 as outputs
                   ; RG2 as input
                   ; RG4:RG3 as outputs
```

FIGURE 9-14: PORTG BLOCK DIAGRAM IN I/O MODE



Note 1: I/O pins have diode protection to VDD and VSS.

9.9 PORTJ, LATJ, and TRISJ Registers

Note:	PORTJ is available only on PIC18C801 devices.

PORTJ is an 8-bit wide, bi-directional I/O port. The corresponding data direction register is TRISJ. Setting a TRISJ bit (= 1) will make the corresponding PORTJ pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISJ bit (= 0) will make the corresponding PORTJ pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATJ register read and write the latched output value for PORTJ.

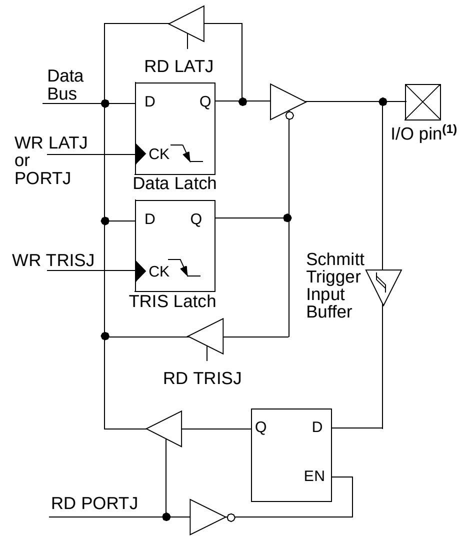
PORTJ is multiplexed with de-multiplexed system data bus D7:D0, when device is configured in 8-bit execution mode. Register MEMCON configures PORTJ as I/O or system bus pins.

Note:	On Power-on Reset, PORTJ defaults to system bus signals.

EXAMPLE 9-10: INITIALIZING PORTJ

```
CLRF    PORTJ    ; Initialize PORTJ by
                 ; clearing output
                 ; data latches
CLRF    LATJ     ; Alternate method
                 ; to clear output
                 ; data latches
MOVLW   0CFh     ; Value used to
                 ; initialize data
                 ; direction
MOVWF   TRISJ    ; Set RJ3:RJ0 as inputs
                 ; RJ5:RJ4 as outputs
                 ; RJ7:RJ6 as inputs
```

FIGURE 9-19: PORTJ BLOCK DIAGRAM IN I/O MODE



Note 1: I/O pins have diode protection to VDD and VSS.

 Advance Information

TABLE 9-17: PORTJ FUNCTIONS

Name	Bit#	Buffer Type	Function
RJ0/D0(1)	bit0	ST/TTL	Input/output port pin or Data bit 0 for external memory interface
RJ1/D1(1)	bit1	ST/TTL	Input/output port pin or Data bit 1 for external memory interface
RJ2/D2(1)	bit2	ST/TTL	Input/output port pin or Data bit 2 for external memory interface
RJ3/D3(1)	bit3	ST/TTL	Input/output port pin or Data bit 3 for external memory interface
RJ4/D4(1)	bit4	ST/TTL	Input/output port pin or Data bit 4 for external memory interface
RJ5/D5(1)	bit5	ST/TTL	Input/output port pin or Data bit 5 for external memory interface
RJ6/D6(1)	bit6	ST/TTL	Input/output port pin or Data bit 6 for external memory interface
RJ7/D7(1)	bit7	ST/TTL	Input/output port pin or Data bit 7 for external memory interface

Legend: ST = Schmitt Trigger input, TTL = TTL input
Note 1: PORTJ is available only on PIC18C801 devices.

TABLE 9-18: SUMMARY OF REGISTERS ASSOCIATED WITH PORTJ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
TRISJ	PORTJ Data Direction Control Register								1111 1111	1111 1111
PORTJ	Read PORTJ pin/Write PORTJ Data Latch								xxxx xxxx	uuuu uuuu
LATJ	Read PORTJ Data Latch/Write PORTJ Data Latch								xxxx xxxx	uuuu uuuu
MEMCON	EBDIS	PGRM	WAIT1	WAIT0	—	—	WM1	WM0	0000 --00	0000 --00

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTJ.

11.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter (Two 8-bit registers: TMR1H and TMR1L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- RESET from CCP module special event trigger

Register 11-1 shows the Timer1 Control register. This register controls the operating mode of the Timer1 module as well as contains the Timer1 oscillator enable bit (T1OSCEN). Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON register).

Figure 11-1 is a simplified block diagram of the Timer1 module.

Note:	Timer1 is disabled on POR.

REGISTER 11-1: T1CON REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **RD16:** 16-bit Read/Write Mode Enable bit
1 = Enables register Read/Write of TImer1 in one 16-bit operation
0 = Enables register Read/Write of Timer1 in two 8-bit operations

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable bit
1 = Timer1 Oscillator is enabled
0 = Timer1 Oscillator is shut-off
The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Select bit
When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T13CKI (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 15-3: SSPCON2 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

bit 7 **GCEN:** General Call Enable bit (In I^2C Slave mode only)
1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (In I^2C Master mode only)
In Master Transmit mode:
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5 **ACKDT:** Acknowledge Data bit (In I^2C Master mode only)
In Master Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (In I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3 **RCEN:** Receive Enable bit (In I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2 **PEN:** STOP Condition Enable bit (In I^2C Master mode only)
SCK release control
1 = Initiate STOP condition on SDA and SCL pins. Automatically cleared by hardware.
0 = STOP condition idle

bit 1 **RSEN:** Repeated START Condition Enabled bit (In I^2C Master mode only)
1 = Initiate Repeated START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated START condition idle

bit 0 **SEN:** START Condition Enabled bit (In I^2C Master mode only)
1 = Initiate START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = START condition idle

Note: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the IDLE mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

FIGURE 16-2: ASYNCHRONOUS TRANSMISSION

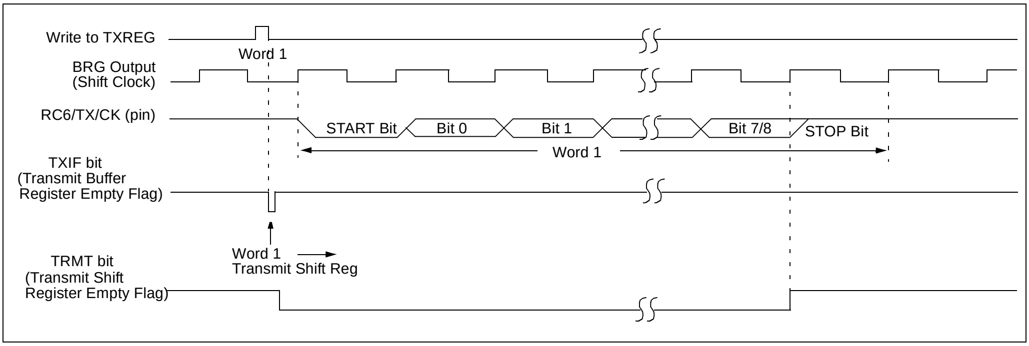
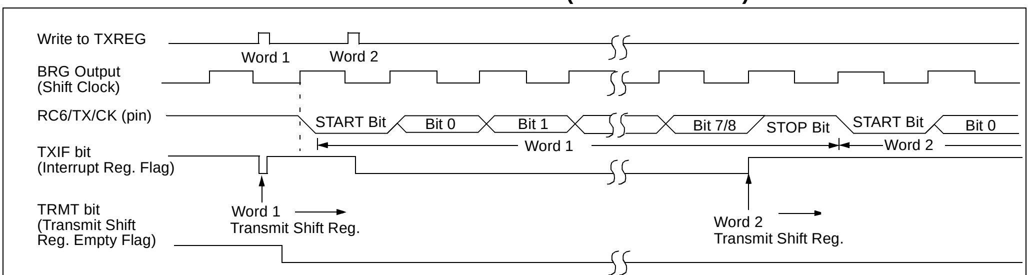


FIGURE 16-3: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 16-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
IPR1	—	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	-000 0000	-000 0000
RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART Transmit Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	ADDEN	BRGH	TRMT	TX9D	0000 0010	0000 0010
SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'.
Shaded cells are not used for Asynchronous Transmission.

 Advance Information

REGISTER 17-2: ADCON1 REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **VCFG1:VCFG0:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O
Shaded cells = Additional A/D channels available on PIC18C801 devices.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

17.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2TOSC
- 4TOSC
- 8TOSC
- 16TOSC
- 32TOSC
- 64TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μs.

Table 17-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

17.3 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

2: Analog levels on any pin defined as a digital input may cause the input buffer to consume current out of the device's specification limits.

TABLE 17-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency	
Operation	**ADCS2:ADCS0**	**PIC18C601/801**	**PIC18LC601/801(5)**
2TOSC	`000`	1.25 MHz	666 kHz
4TOSC	`100`	2.50 MHz	1.33 MHz
8TOSC	`001`	5.00 MHz	2.67 MHz
16TOSC	`101`	10.0 MHz	5.33 MHz
32TOSC	`010`	20.0 MHz	10.67 MHz
64TOSC	`110`	—	—
RC	`x11`	—	—

Note 1: The RC source has a typical TAD time of 4 μs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion or the A/D accuracy may be out of specification.
5: This column is for the **LC** devices only.

19.0 SPECIAL FEATURES OF THE CPU

There are several features intended to maximize system reliability, minimize cost through elimination of external components and provide power saving operating modes:

- OSC Selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- ID Locations

PIC18C601/801 devices have a Watchdog Timer, which can be permanently enabled/disabled via the configuration bits, or it can be software controlled. By default, the Watchdog Timer is disabled to allow software control. It runs off its own RC oscillator for cost reduction. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. By default, HS oscillator mode is selected. There are two main modes of operations for external memory interface: 8-bit and 16-bit (default). A set of configuration bits are used to select various options.

19.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 300000h.

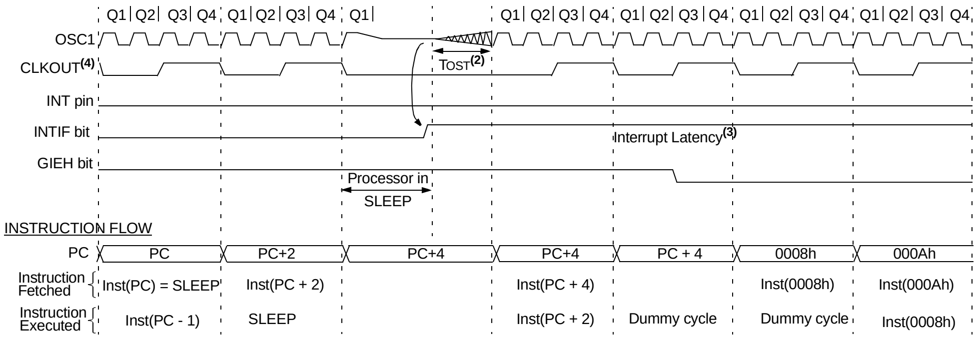
The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h - 3FFFFFh), which can only be accessed using table reads and table writes.

TABLE 19-1: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	—	—	—	—	—	—	FOSC1	FOSC0	`---- --11`
300002h	CONFIG2L	—	BW	—	—	—	—	—	$\overline{\text{PWRTEN}}$	`-1-- ---1`
300003h	CONFIG2H	—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN	`---- 1110`
300006h	CONFIG4L	r	—	—	—	—	—	—	STVREN	`1--- ---1`
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	`0000 0000`
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	`0000 0000`

Legend: `x` = unknown, `u` = unchanged, - = unimplemented, `q` = value depends on condition, r = reserved, maintain ‘1’.
Shaded cells are unimplemented, read as ’0’.

FIGURE 19-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT(1,2)



Note 1: HS or LP oscillator mode assumed.
2: GIE set is assumed. In this case, after wake- up, the processor jumps to the interrupt routine. If GIE is cleared, execution will continue in-line.
3: TOST = 1024TOSC (drawing not to scale). This delay will not occur for RC and EC osc modes.
4: CLKOUT is not available in these oscillator modes, but shown here for timing reference.

20.0 INSTRUCTION SET SUMMARY

The PIC18C601/801 instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration path from them.

With few exceptions, instructions are a single program memory word (16-bits). Each single word instruction is divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal** operations
- **Control** operations

The PIC18C601/801 instruction set summary in Table 20-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 20-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The file register (represented by 'f')
2. The destination of the result (represented by 'd')
3. The accessed memory (represented by 'a')

The file register designator 'f' specifies which file register is to be used by the instruction.

The destination designator 'd' specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The file register (represented by 'f')
2. The bit in the file register (represented by 'b')
3. The accessed memory (represented by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator 'f' represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (represented by 'k')
- The desired FSR register to load the literal value into (represented by 'f')
- No operand required (specified by '—')

The **control** instructions may use some of the following operands:

- A program memory address (represented by 'n')
- The mode of the Call or Return instructions (represented by 's')
- The mode of the Table Read and Table Write instructions (represented by 'm')
- No operand required (specified by '—')

All instructions are a single word, except for four double word instructions. These four instructions were made double word instructions so that all the required information is available in these 32 bits. In the second word, the 4 MSbs are 1's. If this second word is executed as an instruction (by itself), it will execute as a `NOP`.

All single word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a `NOP`.The double word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs. Two word branch instructions (if true) would take 3 μs.

Figure 20-1 shows the general formats that the instructions can have. All examples use the format `'nnh'` to represent a hexadecimal number, where `'h'` signifies a hexadecimal digit.

The Instruction Set Summary, shown in Table 20-2, lists the instructions recognized by the Microchip assembler (MPASM™).

Section 20.1 provides a description of each instruction.

BNC **Branch if Not Carry**

Syntax:	[*label*] BNC n
Operands:	-128 ≤ n ≤ 127
Operation:	if carry bit is '0' (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	`1110` `0011` `nnnn` `nnnn`
Description:	If the Carry bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: `HERE BNC Jump`

Before Instruction
PC = address `(HERE)`

After Instruction
If Carry = 0;
PC = address `(Jump)`
If Carry = 1;
PC = address `(HERE+2)`

BNN **Branch if Not Negative**

Syntax:	[*label*] BNN n
Operands:	-128 ≤ n ≤ 127
Operation:	if negative bit is '0' (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	`1110` `0111` `nnnn` `nnnn`
Description:	If the Negative bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: `HERE BNN Jump`

Before Instruction
PC = address `(HERE)`

After Instruction
If Negative = 0;
PC = address `(Jump)`
If Negative = 1;
PC = address `(HERE+2)`

TSTFSZ — Test f, skip if 0

Syntax:	[*label*] TSTFSZ f [,a]
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]
Operation:	skip if f = 0
Status Affected:	None
Encoding:	0110 | 011a | ffff | ffff
Description:	If 'f' = 0, the next instruction, fetched during the current instruction execution, is discarded and a `NOP` is executed, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, the Bank will be selected as per the BSR value.
Words:	1
Cycles:	1(2) **Note:** 3 cycles if skip and followed by a 2-word instruction

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```
HERE    TSTFSZ  CNT
NZERO   :
ZERO    :
```

Before Instruction
PC = Address (`HERE`)

After Instruction
If CNT = 00h,
PC = Address (`ZERO`)
If CNT ≠ 00h,
PC = Address (`NZERO`)

XORLW — Exclusive OR literal with WREG

Syntax:	[*label*] XORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(WREG) .XOR. k → WREG
Status Affected:	N,Z
Encoding:	0000 | 1010 | kkkk | kkkk
Description:	The contents of WREG are XOR'ed with the 8-bit literal 'k'. The result is placed in WREG.
Words:	1
Cycles:	1

Q Cycle Activity:

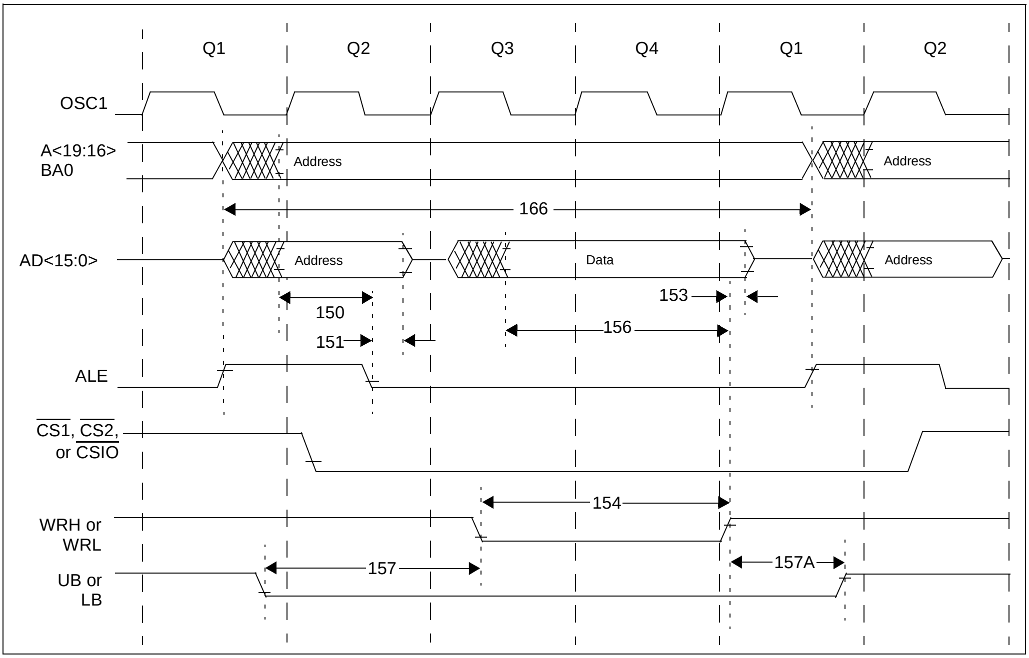
Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to WREG

Example: `XORLW 0AFh`

Before Instruction
WREG = 0B5h
N = ?
Z = ?

After Instruction
WREG = 1Ah
N = 0
Z = 0

FIGURE 22-9: PROGRAM MEMORY WRITE TIMING DIAGRAM



Operating Conditions: 2.0V <VCC <5.5V, -40°C <TA <125°C unless otherwise stated.

TABLE 22-8: PROGRAM MEMORY WRITE TIMING REQUIREMENTS

Param No.	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2alL	Address out valid to ALE↓ (address setup time)	0.25TCY-10	—	—	ns
151	TalL2adl	ALE↓ to address out invalid (address hold time)	5	—	—	ns
153	TwrH2adl	WRn ↑ to data out invalid (data hold time)	5	—	—	ns
154	TwrL	WRn pulse width	0.5TCY-5	0.5TCY	—	ns
156	TadV2wrH	Data valid before WRn ↑ (data setup time)	0.5TCY-10	—	—	ns
157	TbsV2wrL	Byte select valid before WRn ↓ (byte select setup time)	0.25TCY	—	—	ns
157A	TwrH2bsl	WRn ↑ to byte select invalid (byte select hold time)	0.125TCY-5	—	—	ns
166	TalH2alH	ALE↑ to ALE↑ (cycle time)	—	0.25TCY	—	ns
36	TIVRST	Time for Internal Reference Voltage to become stable	—	20	50	µs

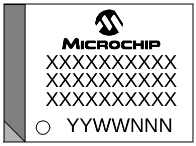
23.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs and Tables are not available at this time.

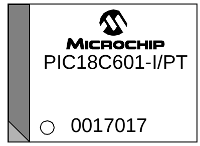
24.0 PACKAGING INFORMATION

24.1 Package Marking Information

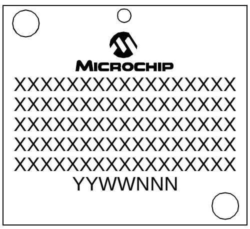
64-Lead TQFP



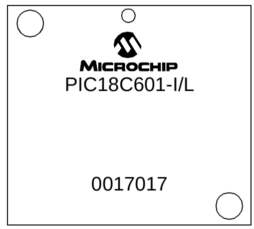
Example



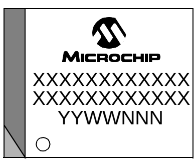
68-Lead PLCC



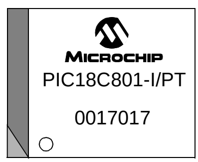
Example



80-Lead TQFP



Example



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

APPENDIX E: DEVELOPMENT TOOL VERSION REQUIREMENTS

This lists the minimum requirements (software/ firmware) of the specified development tool to support the devices listed in this data sheet.

MPLAB® IDE: TBD

MPLAB® SIMULATOR: TBD

MPLAB® ICE 3000:

PIC18C601/801 Processor Module:
Part Number - TBD

PIC18C601/801 Device Adapter:

Socket	Part Number
64-pin TQFP	TBD
68-pin PLCC	TBD
80-pin TQFP	TBD
84-pin PLCC	TBD

MPLAB® ICD: TBD

PRO MATE® II: TBD

PICSTART® Plus: TBD

MPASM™ Assembler: TBD

MPLAB® C18 C Compiler: TBD

Note:	Please read all associated README.TXT files that are supplied with the development tools. These "read me" files will discuss product support and any known limitations.