Renesas Electronics America Inc - R4F20203RDFD#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20203rdfd-v0

4.2.8 Event Link Interrupt Control Status Register (ELCSR)

Address: H'FF0528

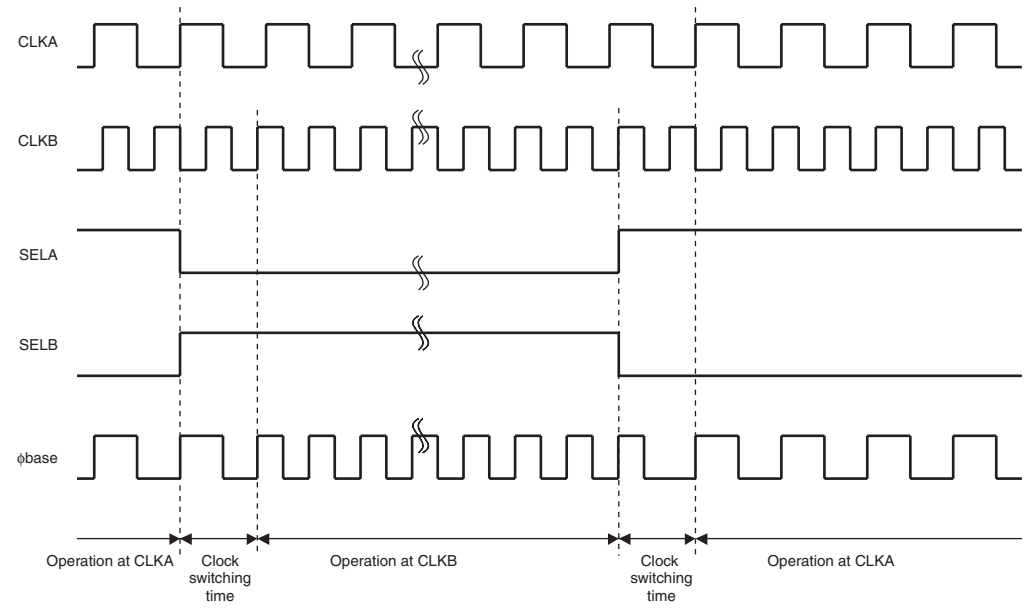
Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ELIE2	ELIE1	ELF2	ELF1
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 4	—	Reserved	These bits are read as 0. The write value should be 0.	—
3	ELIE2	ELC interrupt 2 enable	0: ELF2 interrupts are disabled. 1: ELF2 interrupts are enabled.	R/W
2	ELIE1	ELC interrupt 1 enable	0: ELF1 interrupts are disabled. 1: ELF1 interrupts are enabled.	R/W
1	ELF2	ELC interrupt flag 2	[Setting condition] • When the event selected by ELSR30 occurs*1 [Clearing conditions] • When 1 is read from this bit and then 0 is written to the same bit. • When the DTC is activated by an ELF2 interrupt, and the DISEL bit in MRB of the DTC is 0.*2	R/W
0	ELF1	ELC interrupt flag 1	[Setting condition] • When the event selected by ELSR12 occurs*1 [Clearing conditions] • When 1 is read from this bit and then 0 is written to the same bit. • When the DTC is activated by an ELF1 interrupt, and the DISEL bit in MRB of the DTC is 0.*2	R/W

Notes: 1. For details, see section 12, Event Link Controller.
2. When the DTC is activated by an ELF1 or ELF2 interrupt, the event link source module is not affected.

(2) Switching System Reference Clock Source

Figures 5.8 and 5.9 show clock source switching timing charts for the system reference clock.



[Legend]
CLKA: Clock A
CLKB: Clock B
SELA: CLKA select signal
SELB: CLKB select signal
ϕbase: System reference clock

Note: Clock switching time is a period from the clock select signal change to the second high level of the destination clock.

Figure 5.8 Timing of Clock Source Switching (When the switching destination clock source is active)

10.2.3 Port Data Register 2 (PDR2)

Address: H'FFFFE1

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	PDR27	PDR26	PDR25	PDR24	PDR23	PDR22	PDR21	PDR20
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	PDR27	Port 27 data	0: Low level	R/W
6	PDR26	Port 26 data	1: High level	R/W
5	PDR25	Port 25 data	PDR2 is a register that stores output data for port 2 pins. When PCR2 bits are set to 1, the values stored in PDR2 are output.	R/W
4	PDR24	Port 24 data		R/W
3	PDR23	Port 23 data	When PDR2 is read while PCR2 bits are set to 1, the values stored in PDR2 are read. If PDR2 is read while PCR2 bits are cleared to 0, the pin states are read regardless of the value stored in PDR2.	R/W
2	PDR22	Port 22 data		R/W
1	PDR21	Port 21 data		R/W
0	PDR20	Port 20 data		R/W

10.11.3 Port Pull-Up Control Register B (PUCRB)

Address: H'FF001A

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	PUCRB7	PUCRB6	PUCRB5	PUCRB4	PUCRB3	PUCRB2	PUCRB1	PUCRB0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	PUCRB7	Port B7 pull-up control	0: The pull-up MOS of corresponding pin is disabled.	R/W
6	PUCRB6	Port B6 pull-up control	1: The pull-up MOS of corresponding pin is enabled.	R/W
5	PUCRB5	Port B5 pull-up control	PUCRB is a register that controls the pull-up MOS in bit units of the pins set as the input ports.	R/W
4	PUCRB4	Port B4 pull-up control		R/W
3	PUCRB3	Port B3 pull-up control		R/W
2	PUCRB2	Port B2 pull-up control		R/W
1	PUCRB1	Port B1 pull-up control		R/W
0	PUCRB0	Port B0 pull-up control		R/W

- PUCRB7 bit to PUCRB0 bit (port B7 to B0 pull-up control)

  This function is valid only for the pin set as general input, and for the input pin with a function selected by the PMC. However, this setting is invalid for the analog input pin.

10.11.4 Notes on Using Port B

1. The PB0 pin is initially set as general I/O pin. If using this pin as the analog input pin for the A/D converter, set the PMRA2 bit in PMRA to 1.
2. Pins PB7 and PB6 can be used as analog input pins for the A/D converter or analog output pins for the D/A converter. Do not set these pins as analog input pins and analog output pins at the same time.

11.2.8 DTC Vector Register (DTVECR)

Address: H'FF053D

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	SWDTE	DTC software activation enable	0: Disables the DTC activation by software. 1: Enables the DTC activation by software. Setting this bit to 1 activates DTC. [Clearing conditions] • When the DISEL bit is 0 and the specified number of data transfers has not ended. • When 0 is written to the DISEL bit after a software-activated data transfer end interrupt (SWDTEND) request has been sent to the CPU. When the DISEL bit is 1 and data transfer has ended or when the specified number of data transfers has ended, this bit will not be cleared.	R/W
6	DTVEC6	DTC software activation vector 6 to 0	These bits specify a vector number for DTC activation by software. These bits specify a vector number for DTC software activation. The vector address is expressed as H'0400 + (vector number × 2). For example, when DTVEC6 to DTVEC0 = H'10, the vector address is H'0420. When the bit SWDTE is 0, these bits can be written.	R/W
5	DTVEC5			R/W
4	DTVEC4			R/W
3	DTVEC3			R/W
2	DTVEC2			R/W
1	DTVEC1			R/W
0	DTVEC0			R/W

DTVECR enables or disables DTC activation by software, and sets a vector number for the software activation interrupt.

12.2.12 Event-Generation Timer Interval Setting Register B (ELTMSB)

Address: H'FF06BA

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	C3CLS[3:0]				C2CLS[3:0]			
Value after reset:	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 4	C3CLS[3:0]*	Channel 3 event-generation interval select	0000: Clock source φELC/1	R/W
			0001: Clock source φELC/2	
			0010: Clock source φELC/4	
			0011: Clock source φELC/8	
			0100: Clock source φELC/16	
			0101: Clock source φELC/32	
			0110: Clock source φELC/64	
			0111: Clock source φELC/128	
			1000: Clock source φELC/256 (initial value)	
			1001: Clock source φELC/512	
			1010: Clock source φELC/1024	
			1011: Clock source φELC/2048	
			1100: Clock source φELC/4096	
			1101: Clock source φELC/8192	
			1110: Clock source φELC/16384	
			1111: Clock source φELC/32768	

15.3.6 Function of Changing Output Pins for GR

With the settings of bits IOC3 and IOD3 in TRCIOR1, pins for outputs of compare match signals for GRC and GRD can be changed from the FTIOC and FTIOD pins to the FTIOA and FTIOB pins. This means that the compare match A signal with the compare match C signal can be output on the FTIOA pin. The compare match B with the compare match D signal can be output on the FTIOB pin. Figure 15.24 is a block diagram of this function. Channel 0 and channel 1 can be set independently.

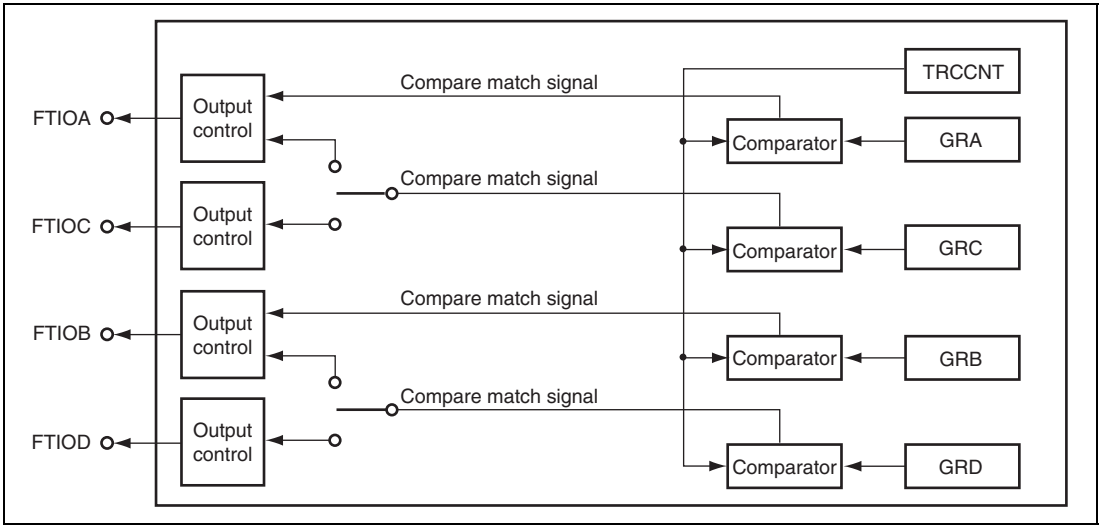


Figure 15.24 Block Diagram of Output Pins for GR

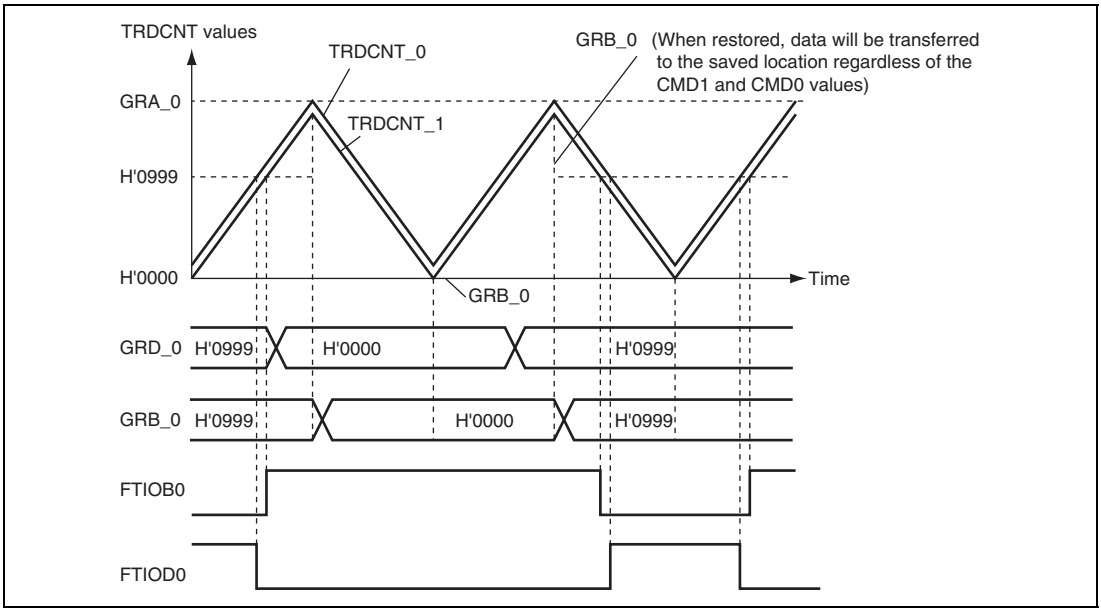


Figure 16.49 Buffer Operation (4)
(Buffer Operation in Complementary PWM Mode CMD1 =1, CMD0 = 0)

16.3.14 Operation through an Event Link

Using the event link controller (ELC), timer RD unit 0 can be made to operate in the following ways in relation to events occurring in other modules. Each channel 0 and 1 can be specified independently.

(1) Staring Counter Operation

The start of counting operations by timer RD can be selected by ELOPA and ELOPB of the ELC. When the event specified by ELSR3 and ELSR4 occur, the STR[1:0] bits in TRDSTR are set to 1, which stars counting by timer RD. However, if the specified event occurs when the STR bit has already been set to 1, the event is not effective.

(2) Counting Event

The counting of events by timer RD can be selected by ELOPA and ELOPB of the ELC. When the event specified in ELSR3 and ELSR4 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of the TPSC[2:0] bits in TRDCR and the STR1, STR0 bits in TRDSTR. When the value of the counter is read, the value read out is the actual number of input events.

(3) Input Capture

Input capture operation of timer RD can be selected by ELOPA and ELOPB of the ELC. When the event specified in ELSR3 and ELSR4 occurs, GRD captures the value of TRDCNT. When input capture operation initiated by an event link is in use, set the IOD[3:0] bits = b'1101 in TRDIORC of timer RD, set the STR bit in TRDSTR to 1, and then start the counter. Since input on the FTIOD pin becomes valid at the same time, fix the input to the FTIOD pin or take other measures such as not allocating the FTIOD pin to the port in the PMC, etc.

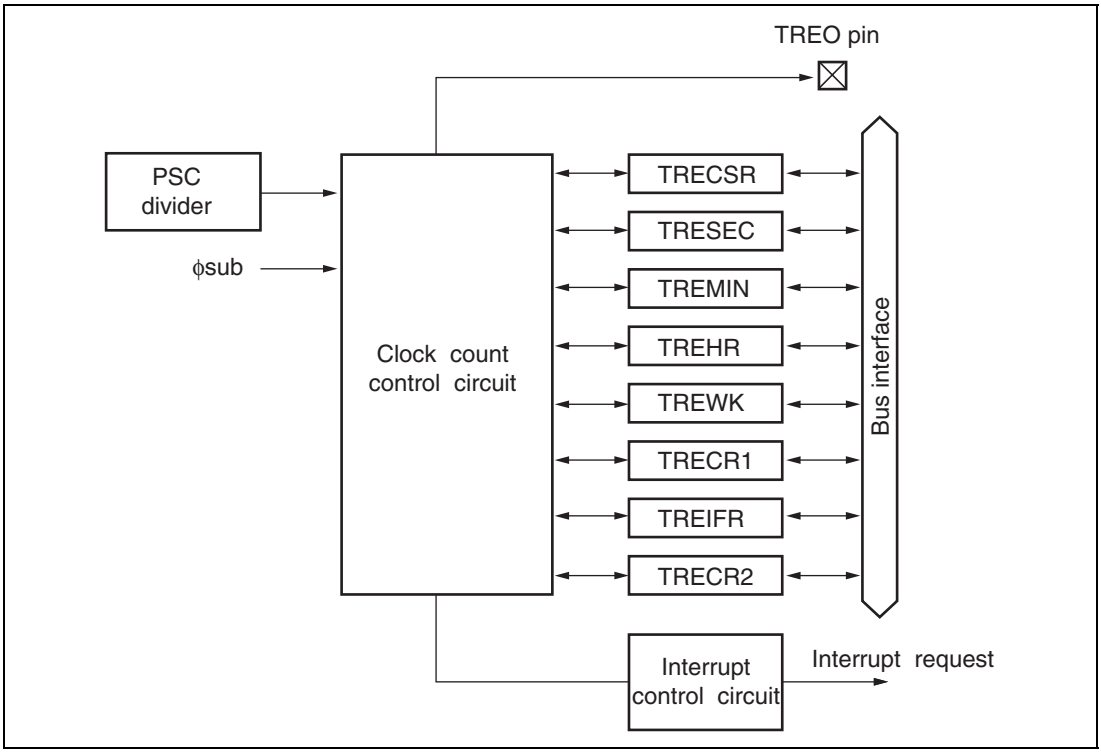


Figure 17.1 Block Diagram of Timer RE

Table 17.1 shows the timer RE input/output pin.

Table 17.1 Pin Configuration

Pin Name	I/O	Function
TREO	Output	Clock or compare-match output

18.3.5 Operation through an Event Link

Using the event link controller (ELC), timer RG can be made to operate in the following ways in relation to events occurring in other modules.

(1) Staring Counter Operation

The start of counting operations by timer RG can be selected by ELOPC of the ELC. When the event specified by ELSR8 occur, the STR bit in TRGMDR is set to 1, which starts counting by timer RG. However, if the specified event occurs when the STR bit has already been set to 1, the event is not effective.

(2) Counting Event

The counting of events by timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of TPSC[2:0] bits in TRGCR and the STR bit in TRGMDR. When the value of the counter is read, the value read out is the actual number of input events.

(3) Input Capture

Input capture operation of timer RG can be selected by ELOPC of the ELC. When the event specified in ELSR8 occurs, GRB captures the value of TRGCNT. When input capture operation initiated by an event link is in use, set IOB[2:0] = b'101 in the TRGIOR register of timer RG, set the STR bit in TRGMDR, and then start the counter. Since input on the TGIOB pin becomes valid at the same time, fix the input to the TGIOB pin or take other measures such as not allocating the TGIOB pin to the port in the PMC, etc.

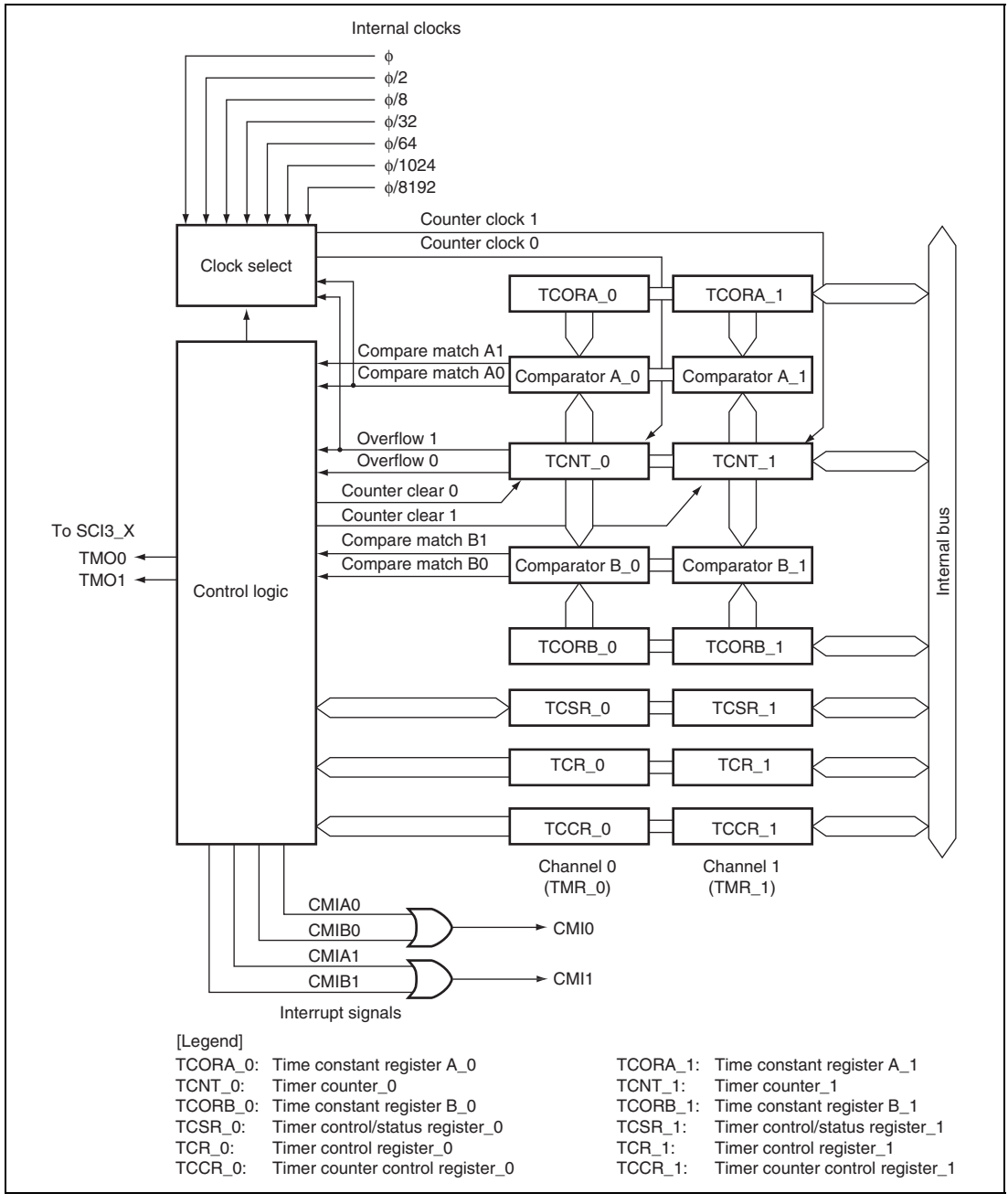


Figure 19.1 Block Diagram of 8-Bit Timer Module

21.2.6 Serial Control Register 3 (SCR3)

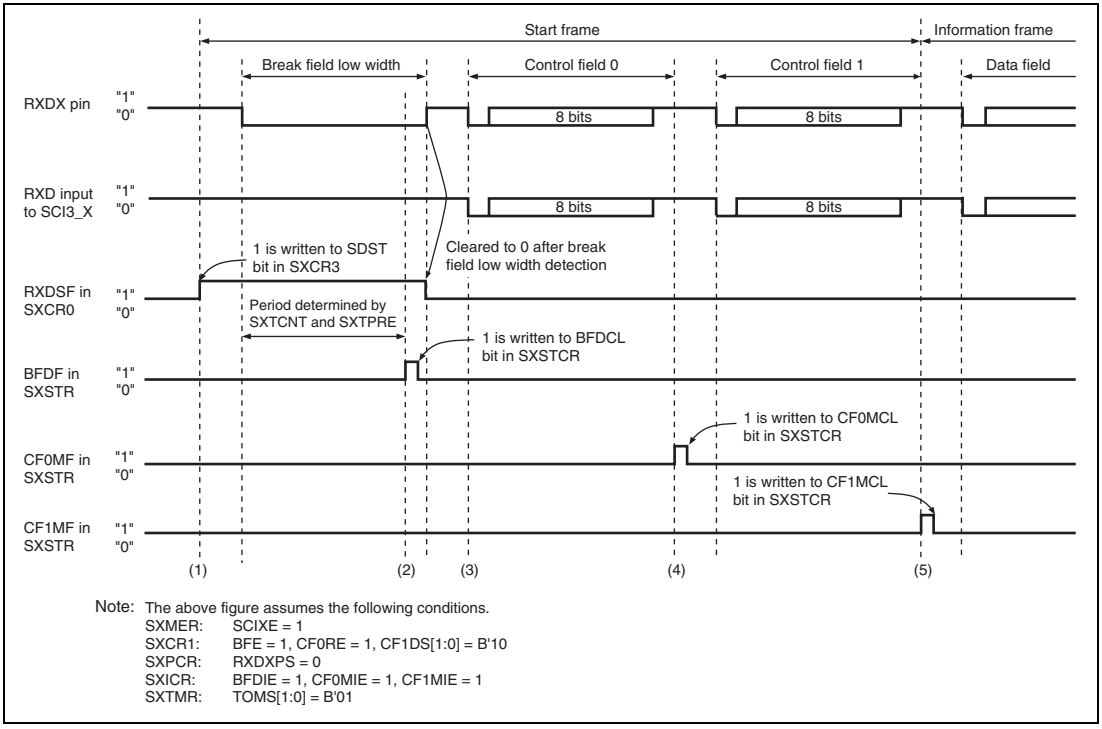
Address: H'FF0552, H'FF055A, H'FF0562

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	TIE	Transmit interrupt enable	0: The TXI interrupt request is disabled. 1: The TXI interrupt request is enabled.	R/W
6	RIE	Receive interrupt enable	0: RXI and ERI interrupt requests are disabled. 1: RXI and ERI interrupt requests are enabled.	R/W
5	TE	Transmit enable	0: Transmission is disabled. 1: Transmission is enabled.	R/W
4	RE	Receive enable	0: Reception is disabled. 1: Reception is enabled.	R/W
3	MPIE	Multiprocessor interrupt enable	(Enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is disabled. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, see section 21.5, Multiprocessor Communication Function.	R/W
2	TEIE	Transmit end interrupt enable	0: The TEI interrupt request is disabled. 1: The TEI interrupt request is enabled.	R/W

4. When the received control field 0 data agrees with the data set to SXCF0DR, the CF0MF bit in SXSTR is set to 1. Here, if the CF0MIE bit in SXICR is 1, an SCIX1 interrupt is generated. Then the control field 1 data begins to be received using the SCI3_X. When the received control field 0 data does not agree with the data set to SXCF0DR, the SCIX returns to the state prior to break field low width detection.
5. When the received control field 1 data agrees with the data set to SXPCF1DR or SXSCF1DR, the CF1MF bit in SXSTR is set to 1. Here, if the CF1MIE bit in SXICR is 1, an SCIX1 interrupt is generated. Then the information frame is transmitted and received using the SCI3_X. When the received control field 1 data does not agree with the data set to SXPCF1DR or SXSCF1DR, the SCIX returns to the state prior to break field low width detection.

The break field and control field 0 data should be omitted according to the start frame configuration.



Note: The above figure assumes the following conditions.
SXMER: SCIXE = 1
SXCR1: BFE = 1, CF0RE = 1, CF1DS[1:0] = B'10
SXPCR: RXDXPS = 0
SXICR: BFDIE = 1, CF0MIE = 1, CF1MIE = 1
SXTMR: TOMS[1:0] = B'01

Figure 22.8 Start Frame Reception Example

(3) Receive Operation

In receive mode, data is latched at the rise of the transfer clock. The transfer clock is output when MST in ICCR1 is 1 and is input when MST is 0. For receive mode operation timing, see figure 24.15. The reception procedure and operations in receive mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MST and CKS[3:0] bits in ICCR1 to 1 (Initial setting).
2. When the transfer clock is output, set MST to 1 to start outputting the receive clock.
3. When the receive operation is completed, data is transferred from ICDRS to ICDRR and RDRF in ICSR is set. When MST = 1, the next byte can be received, so the clock is continually output. The continuous reception is performed by reading ICDRR every time RDRF is set. When the 8th clock is risen while RDRF is set to 1, the overrun is detected and AL/OVE in ICSR is set. At this time, the previous reception data is retained in ICDRR.
4. To stop receiving when MST = 1, read ICDRR after setting RCVD in ICCR1 to 1. Then, SCL is fixed high after receiving the next byte data.

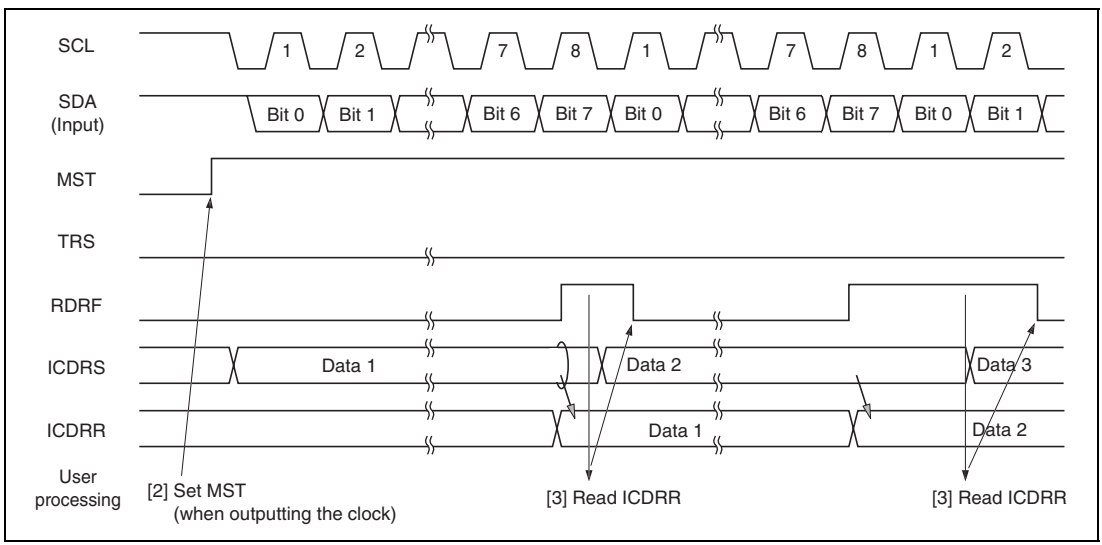


Figure 24.15 Receive Mode Operation Timing

Section 25 Synchronous Serial Communication Unit (SSU)

Note: In this section, the synchronous serial communication unit is abbreviated as SSU for convenience.

The synchronous serial communication unit (SSU) can handle clocked synchronous serial data communication.

Figure 25.1 shows a block diagram of the SSU.

Either the SSU or IIC2 incorporated in this LSI can be used at a time. Accordingly, when the SSU function is used, the IIC2 function is not available.

25.1 Features

- Can be operated in clocked synchronous communication mode or four-line bus communication mode (including bidirectional communication mode)
- Can be operated as a master or a slave device
- Choice of seven internal clocks (φ/256, φ/128, φ/64, φ/32, φ/16, φ/8, φ/4) and an external clock as a clock source
- Clock polarity and phase of SSCK can be selected
- Choice of data transfer direction (MSB-first or LSB-first)
- Receive error detection: overrun error
- Multimaster error detection: conflict error
- Five interrupt sources: transmit-end, transmit-data-empty, receive-data-full, overrun error, and conflict error. The DTC can be activated by the transmit-data-empty and receive-data-full interrupts.
- The transmitter and receiver with buffer structure allow continuous transmission and reception of serial data.

26.3.2 Slave Mode

Figure 26.5 shows the example of hardware LIN interface operation for receiving the header field in slave mode. Figures 26.6 to 26.8 show the flowcharts for header field reception.

The hardware LIN interface operates as follows for header field reception.

1. When 1 is written to the LSTART bit in LINCR register of the hardware LIN interface, Sync Break detection is enabled.
2. When a low level input is longer than the time set in timer RA, it is detected as Sync Break, thus setting the SBDCT flag in the LINST register to 1. In this case, if the SBIE bit in the LINCR register is set to 1, the timer RA/HW-LIN interrupt occurs. The hardware LIN interface then measures the Sync Field.
3. The hardware LIN interface receives the Sync Field (H'55). During reception, the hardware LIN interface measures the time from the start bit through bit 6. Here, the Sync Field input to the SCI3 RXD can be either enabled or disabled depending on the SBE bit setting in the LINCR register.
4. Completion of Sync Field measurement sets the SFDCT flag in the LINST register to 1. In this case, if the SFIE bit in the LINCR register is 1, the timer RA/HW-LIN interrupt occurs.
5. After completing Sync Field measurement, the hardware LIN interface calculates the transfer rate from the timer RA count value and sets the rate in SCI3_1, and also updates the TRAPRE and TRATR registers in timer RA. Then the hardware LIN interface receives the ID field using SCI3_1.
6. After completing ID field reception, the hardware LIN interface performs response field communications.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
High-speed OCO trimming data register 3	HOTRMDR3	8	H'FF062E	Clock oscillator	8	2
High-speed OCO trimming data register 4	HOTRMDR4	8	H'FF062F		8	2
32-MHz high-speed OCO trimming data register 1	HO32TRMDR1	8	H'FF063A		8	2
32-MHz high-speed OCO trimming data register 2	HO32TRMDR2	8	H'FF063B		8	2
32-MHz high-speed OCO trimming data register 3	HO32TRMDR3	8	H'FF063C		8	2
32-MHz high-speed OCO trimming data register 4	HO32TRMDR4	8	H'FF063D		8	2
Timer RG counter	TRGCNT	16	H'FF0640	Timer RG	16*4	2
General register A	GRA	16	H'FF0642	Timer RG	16*4	2
General register B	GRB	16	H'FF0644	Timer RG	16*4	2
Timer RG mode register	TRGMDR	8	H'FF0646	Timer RG	8	2
Timer RG counter control register	TRGCNTCR	8	H'FF0647	Timer RG	8	2
Timer RG control register	TRGCR	8	H'FF0648	Timer RG	8	2
Timer RG I/O control register	TRGIOR	8	H'FF0649	Timer RG	8	2
Timer RG status register	TRGSR	8	H'FF064A	Timer RG	8	2
Timer RG interrupt enable register	TRGIER	8	H'FF064B	Timer RG	8	2
GRA buffer register	BRA	16	H'FF064C	Timer RG	16*4	2
GRB buffer register	BRB	16	H'FF064E	Timer RG	16*4	2
Flash memory control register 1	FLMCR1	8	H'FF0660	FLASH	8	2
Flash memory control register 2	FLMCR2	8	H'FF0661	FLASH	8	2
Flash memory data flash protect register	DFPR	8	H'FF0662	FLASH	8	2
Flash memory status register	FLMSTR	8	H'FF0663	FLASH	8	2
Event link setting register 0	ELSR0	8	H'FF0680	ELC	8	2
Event link setting register 1	ELSR1	8	H'FF0681	ELC	8	2
Event link setting register 2*7	ELSR2	8	H'FF0682	ELC	8	2
Event link setting register 3	ELSR3	8	H'FF0683	ELC	8	2
Event link setting register 4	ELSR4	8	H'FF0684	ELC	8	2

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{NMI}$, $\overline{IRQ0}$ to $\overline{IRQ7}$ TRAIO,TRGB, FTCI, TRGC, FTIOA FTIOB, FTIOC, FTIOD, $\overline{TRCOI}$, FTIOA0, FTIOB0, FTIOC0, FTIOD0, FTIOA1, FTIOB1, FTIOC1, FTIOD1 $\overline{TRDOI\_0}$, FTIOA2 FTIOB2, FTIOC2, FTIOD2 FTIOA3, FTIOB3, FTIOC3, FTIOD3 $\overline{TRDOI\_1}$, TCLKA TCLKB, TGIOA TGIOB, SCK3 SCK3_2, SCK3_X $\overline{ADTRG1}$, $\overline{ADTRG2}$ RXD, RXD_2, RXD_X, RXDX, SCL, SDA SSCK, $\overline{SCS}$ $\overline{SSI}$, SSO, OSC1, $\overline{RES}$	V_{IN} = 0.5 V to (V_{CC} - 0.5 V)	—	—	1.0	µA	
		P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P72 to P77 P80 to P87 P90 to P97 PA0 to PA7 PB0 to PB7 PJ1, PJ0						